Final Exam, ECE 137A

Wednesday March 18, 2015 7:30-10:30 PM

Name: _____

Closed Book Exam: Class Crib-Sheet and 3 pages (6 surfaces) of student notes permitted
Do not open this exam until instructed to do so. Use any and all reasonable approximations (5% accuracy), ***after stating & justifying them***.
Show your work:
Full credit will not be given for correct answers if supporting work is missing.

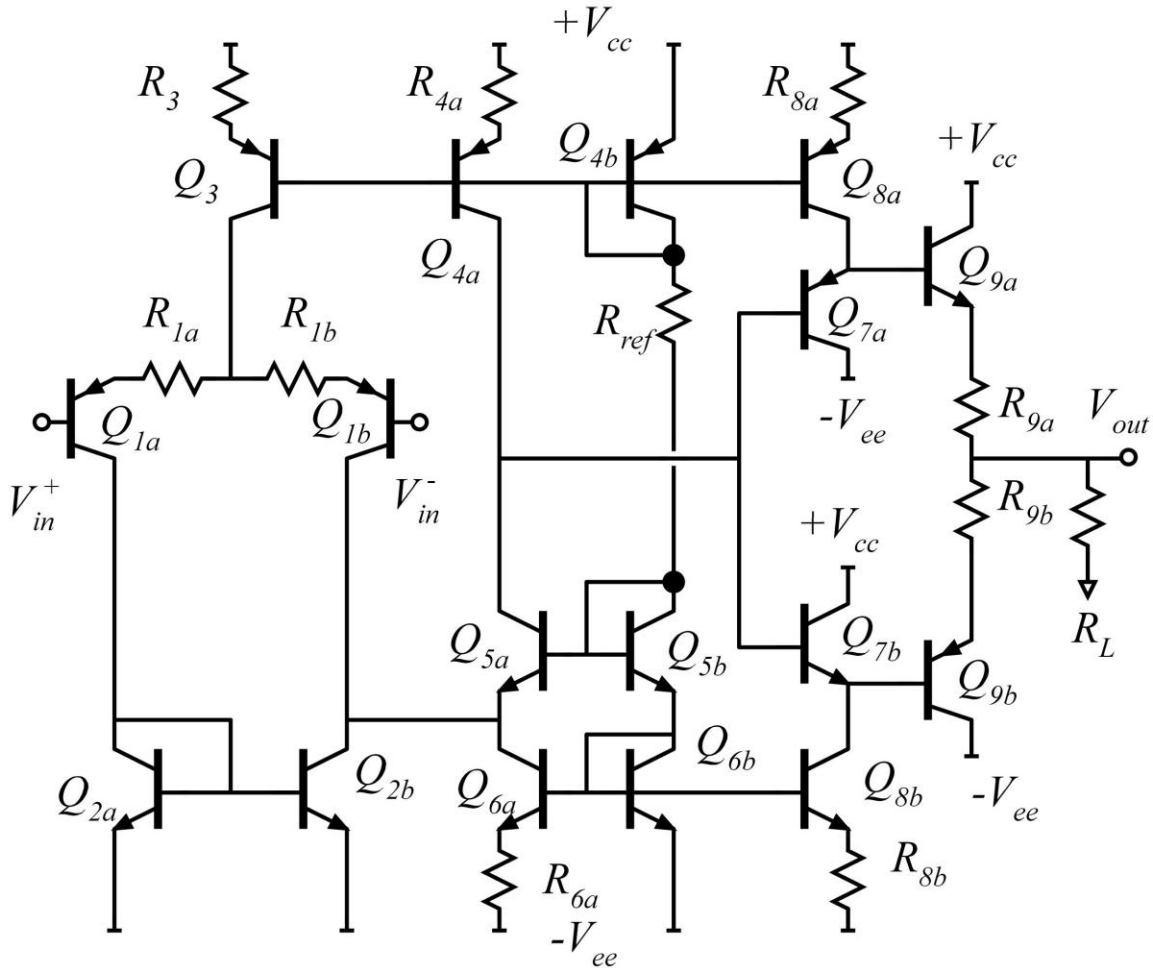
Good luck

Time function	LaPlace Transform
$\delta(t)$ impulse	1
$U(t)$ unit step-function	$1/s$
$e^{-\alpha t}U(t)$	$\frac{1}{s+\alpha}$
$e^{-\alpha t}\cos(\omega_d t)U(t)$	$\frac{s+\alpha}{(s+\alpha)^2+\omega_d^2}$
$e^{-\alpha t}\sin(\omega_d t)U(t)$	$\frac{\omega_d}{(s+\alpha)^2+\omega_d^2}$

Part	Points Received	Points Possible	Part	Points Received	Points Possible
1a		5	2c		15
1b		6	2d		10
1c		4	3a		7
1d		10	3b		8
1e		10	3c		7
2a		10	3d		8
2b		10			
total		100			

Problem 1, 35 points

This is an NOT an Op-Amp: Analyze under the assumption that the differential and common mode input voltages are at zero volts

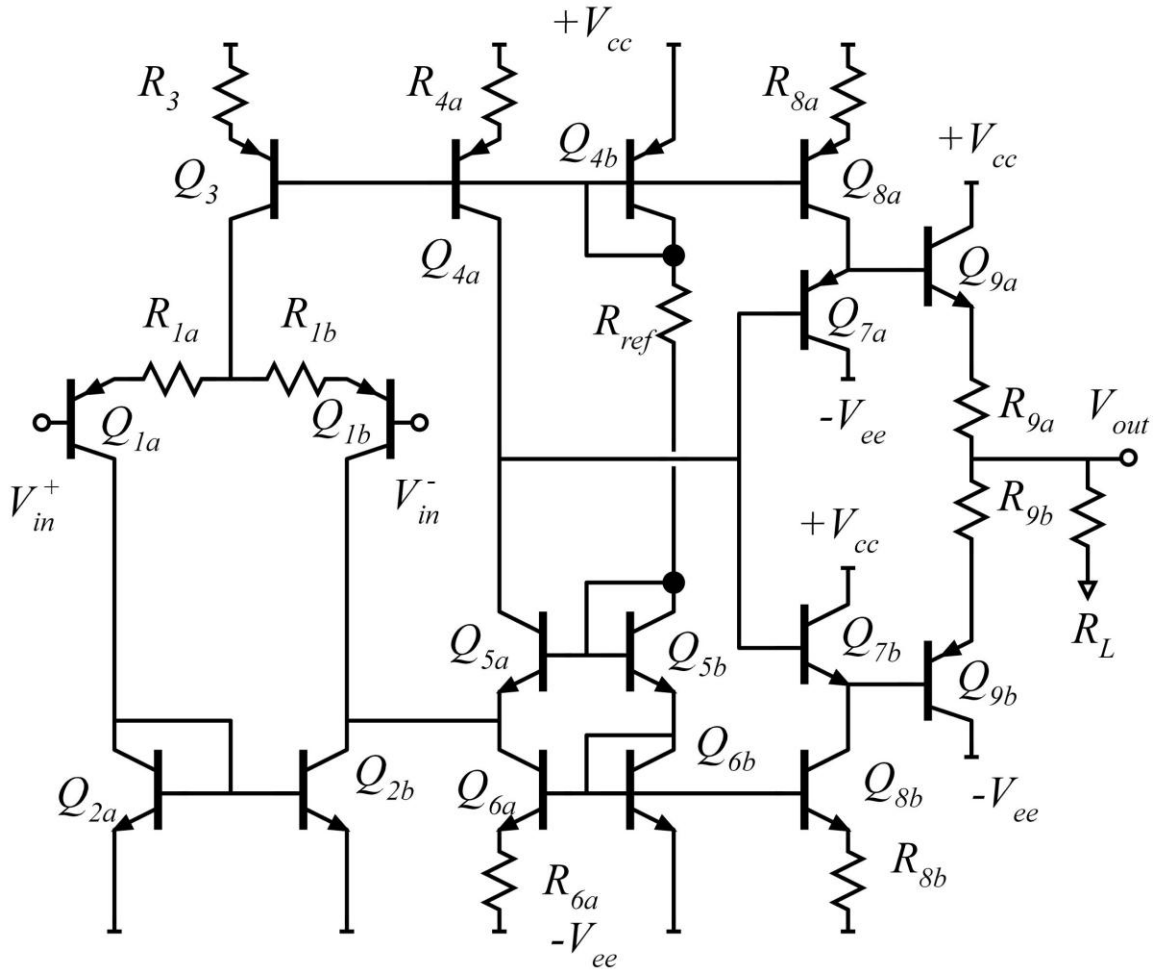


All the transistors have the same (matched) I_S, have $\beta = 100$, and $V_A = \infty$ Volts.
$V_{CE(sat)} = 0.5\text{V}$. V_{be} is roughly 0.7 V, but use $V_{be} = (kT/q)\ln(I_E / I_S)$ when necessary and appropriate. The supplies are +2 Volts and -2 Volts.

Q1ab,2ab,4a,5a,6a are to be biased at 250 μA collector current.
Q4B,5B,6B are to be biased at 1 mA collector current.
Q8ab are to be biased at 500 μA collector current.
Q9ab are to be biased at 250 μA collector current.
$R_L = 250\Omega$ R1a=R1b=500 Ohms

Part a, 5 points

DC bias---to simplify ,assume $\beta = \infty$ ***for the DC analysis only*.**



On the circuit diagram above, label the DC voltages at **ALL nodes**, the DC currents through **ALL resistors,** and the DC collector currents of **all transistors**.

a

Part b, 6 points
DC bias:

Find the value of all resistors.
R3=____ R4ba=____ R6a=____ Rref=____ R8a=____ R8b=____
R9a=____ R9b=____

a

Part c, 4 points

Find the transconductance of the transistors below:
gm1a=_____ gm1b=_____ gm5a=_____ gm7a=_____
gm7b=_____ gm9a=_____ gm9b=_____

a

Part d, 10 points.

Find the following, ***using the actual value of β, i.e. β=100***

	Voltage Gain	Input impedance
Transistor combination Q2a,2b,1a,1b		
Q5a		
Q7a or 7b		
Q9a or 9b		
Overall differential Vout/Vin		

Part e, 10 points

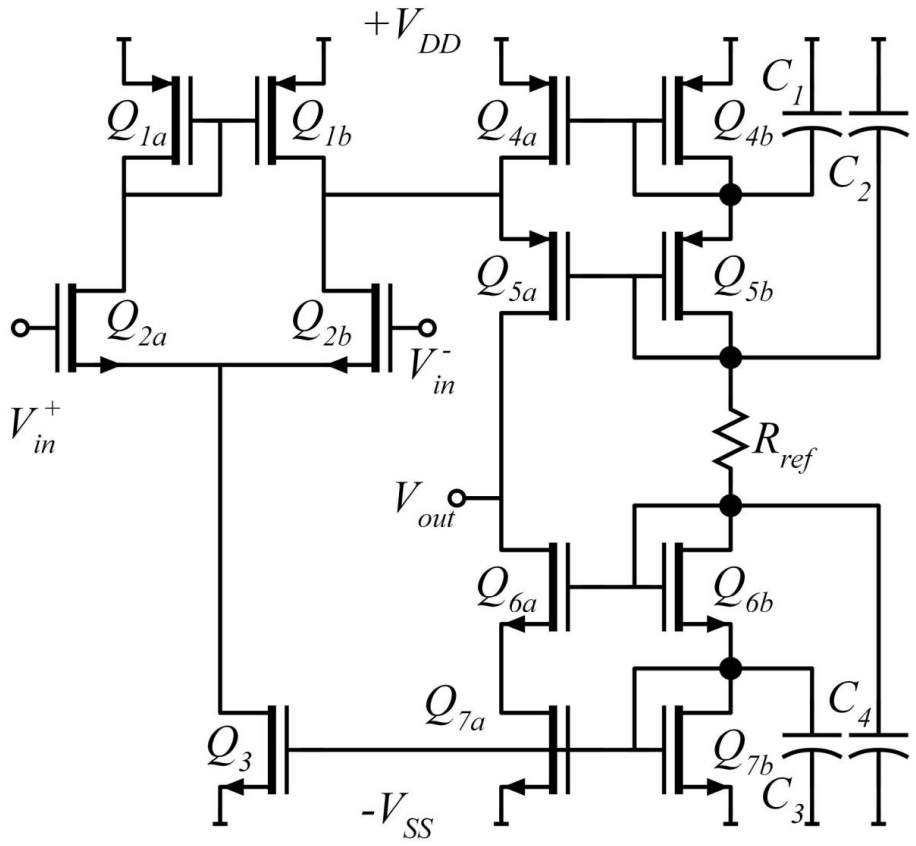
Maximum peak-peak output voltage (***show all your work***)

	magnitude and sign of maximum output signal swing due to ***cutoff***	magnitude and sign of maximum output signal swing due to ***saturation***
Transistor Q4a		
Transistor Q5a		
Transistor Q7a		
Transistor Q7b		
Transistor Q9a		
Transistor Q9b		

Be warned: In some cases a limit is not relevant at all. Mark those answers "not relevant". But, give a 1-sentence statement below as to why it is not relevant. Q7ab and Qab form a push pull stage, so be careful about your answers here.

Problem 2, 35 points

This is an Op-Amp---analyze the bias under the assumption that DC output voltage is zero volts, that the positive input Vi+ is zero volts, and that we must determine the DC value of the negative input voltage (Vi-) necessary to obtain this.



The NMOSFETs and the PMOSFETS have a 0.20 V threshold, a 22nm gate length, 300 cm^2/Vs mobility, a 10^7cm/s saturation drift velocity, and $1/\lambda$ =3 Volts. The gate oxide thickness is 1.0nm and the dielectric constant is 3.8. This gives

$\mu c_{ox} W_g / 2L_g = 15\,\text{mA/V}^2 \cdot (W_g / 1\mu\text{m})$ and

$v_{sat} c_{ox} W_g = 3.36\,\text{mA/V} \cdot (W_g / 1\mu\text{m})$ (both are a bit unrealistic for a real technology).

and $v_{sat} L_g / \mu$ =0.113 V

V_{DD} =+1 V, $-V_{SS}$ = -1 V,

Part a, 10 points

DC bias.

Approximation: ignore the term $(1+\lambda V_{DS})$ ***in DC bias analysis.***

Analyze the bias under the assumption that DC output voltage is zero volts, that the positive input Vi+ is zero volts, and that we must determine the DC value of the negative input voltage (Vi-) necessary to obtain this.

Q1ab,2ab are to be biased at 50 μA drain current.

Q4ab,5ab,6ab,7ab are to be biased at 200 μA drain current

All transistors are to operate with $|V_{gs}|$=0.30V.

Find the gate widths of all transistors.

Find:

Wg1a=_____ Wg1b =_____ Wg2a=_____ Wg2b =_____ Wg3=_____

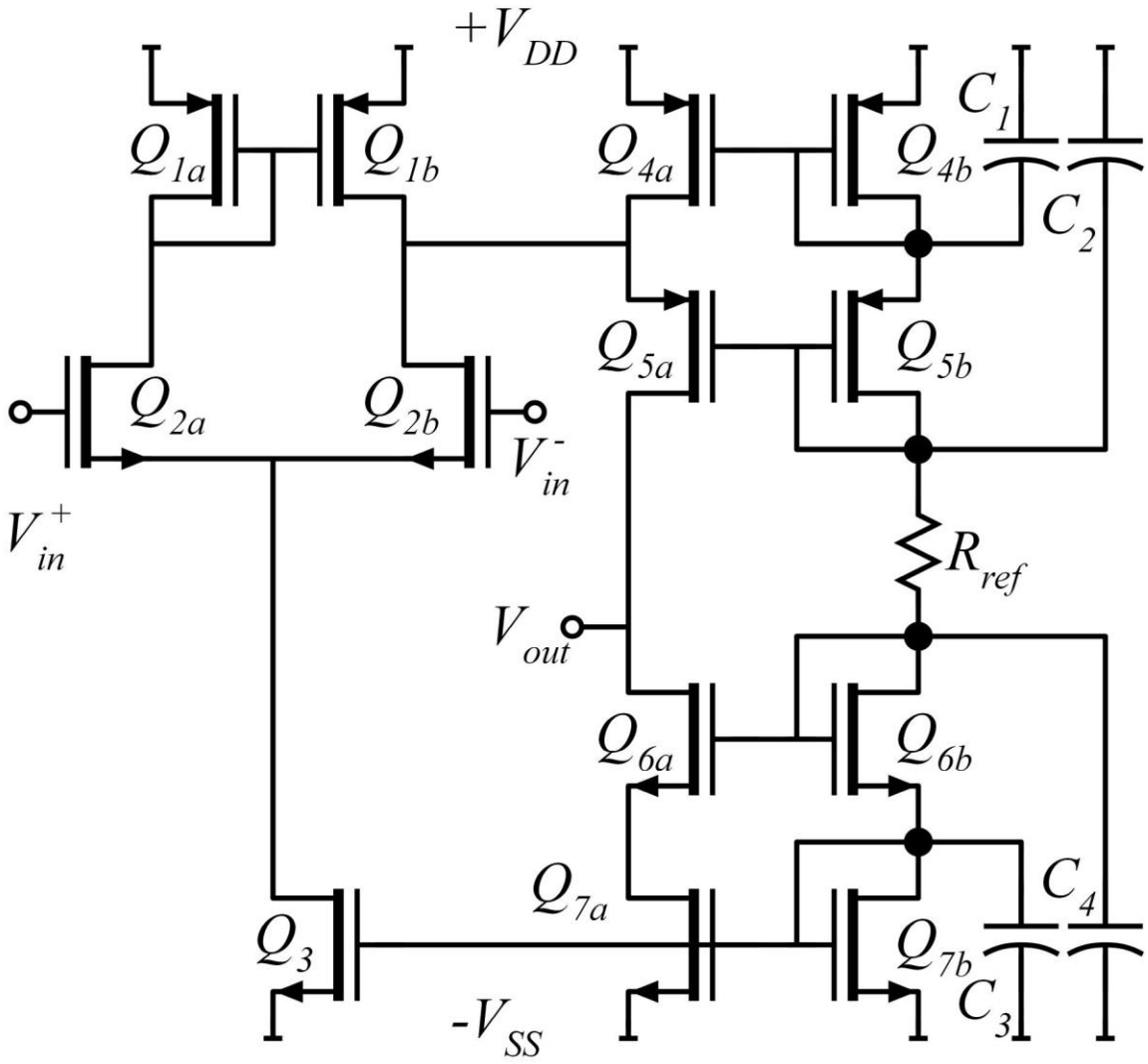
Wg4a=_____ Wg4b =_____ Wg5a=_____ Wg5b =_____

Wg6a=_____ Wg6b =_____ Wg7a=_____ Wg7b =_____

Rref=_____

Part b, 10 points

DC bias



On the circuit diagram above, label the DC voltages at **ALL nodes** the drain currents of **ALL transistors,** and the gate widths of **ALL transistors**

a

a

Part c, 15 points.

You will now compute the op-amp differential gain. ***You must consider the*** $(1+\lambda V_{DS})$ ***term in the FET IV characteristics when you do this.***

The capacitors C1-C4 are all zero Ohms AC impedance. (They would not be present in a real design; they are added here to simplify the exam).

Find the following

	Voltage Gain	Input impedance
Transistor combination Q2a,2b,1a,1b		
Q5a		
Overall differential Vout/Vin		

(Alternative----if you very skilled, you might be able to compute the combined gain of Q2a,2b,1a,1b and Q5a, all together, in a single step using Norton or Thevenin methods. If you do so, first, don't ask for hints on how to do this and, second, do please also calculate the input impedance of Q5a.)

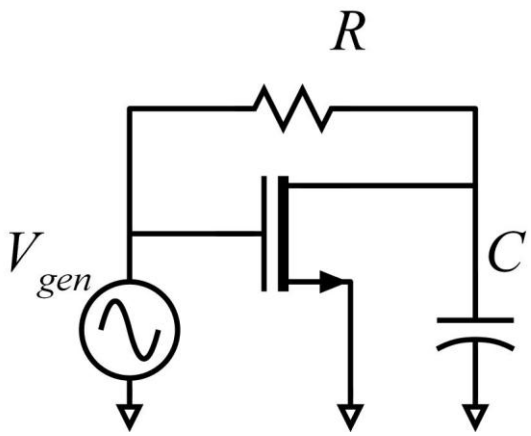
Part d, 10 points

Maximum peak-peak output voltage at the positive output Vo+ (***show all your work***)

	magnitude and sign of maximum output signal swing due to ***cutoff***	magnitude and sign of maximum output signal swing due to: ***knee voltage*** (saturation)
Transistor Q5a		
Transistor Q6a		
Transistor Q2a		
Transistor Q2b		

Be warned: in some cases a limit is not relevant. Mark those answers "not relevant". But, give a 1-sentence statement why below.

Problem 3, 30 points



You will be working on the circuit to the left

Ignore DC bias analysis. You don't need it.

The transistor has transconductance gm.

Its output resistance Rds is infinity...so you don't need to include this element in the circuit diagram !

Part a, 7 points

Draw a small-signal equivalent circuit of the circuit.

Part b, 8 points

gm=20 mS. C=1 μF. R= 1000 Ohms

Find, by nodal analysis, a small-signal expression for Vout/Vin. Be sure to give the answer with **correct units** and in ratio-of-polynomials form, i.e.

$$\frac{V_{out}(s)}{V_{gen}(s)} = K \cdot \frac{1 + b_1 s + b_2 s^2 + \ldots}{1 + a_1 s + a_2 s^2 + \ldots} \text{ or (as appropriate) } \frac{V_{out}(s)}{V_{gen}(s)} = K \cdot (s\tau)^n \cdot \frac{1 + b_1 s + b_2 s^2 + \ldots}{1 + a_1 s + a_2 s^2 + \ldots}$$

Note that an expression like

$\frac{V_{out}(s)}{V_{gen}(s)} = \frac{1}{1 + (3 \cdot 10^{-6})s}$ is dimensionally wrong; $\frac{1}{1 + (3 \cdot 10^{-6}\text{seconds})s}$ is dimensionally correct

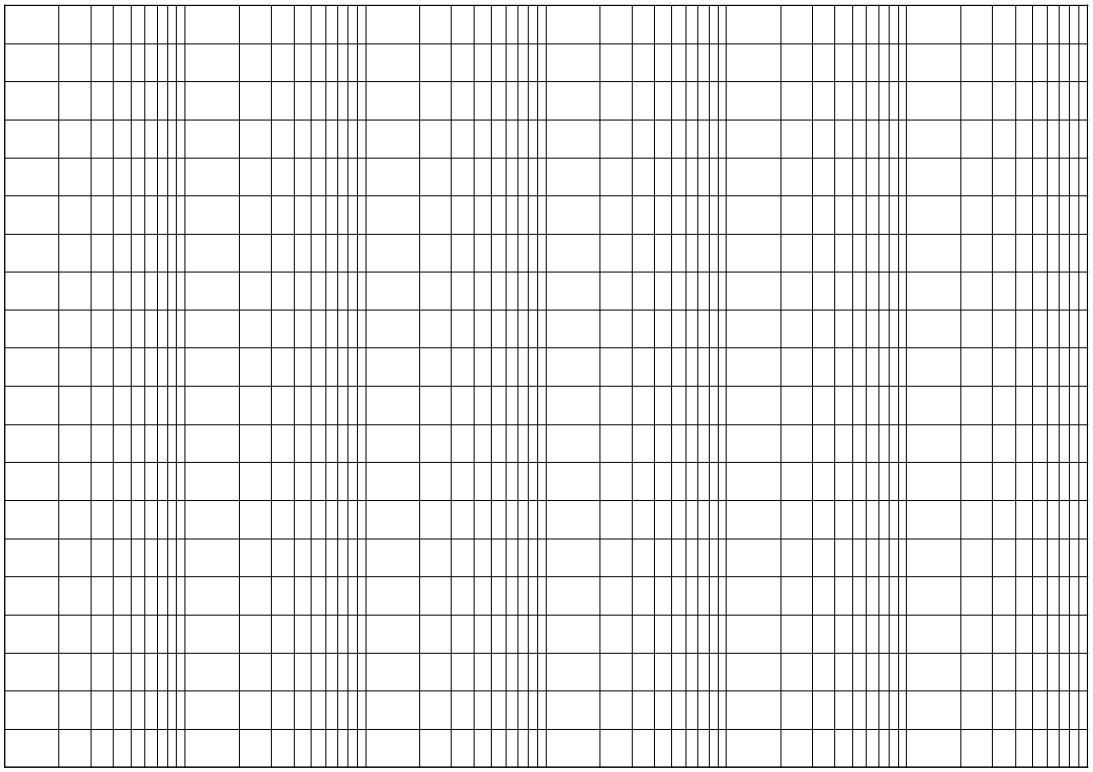
Vout(s)/Vin(s)= _____

Part c, 7 points

Find any/all pole and zero frequencies of the transfer function, in Hz:

_____,_____,_____,_____

Draw a clean Bode Plot of Vout/Vin,
LABEL AXES, LABEL all relevant gains and pole or zero frequencies, Label Slopes



a

Part d, 8 points

Vin(t) is a 0.1 V amplitude step-function.

Find Vout(t)=_____

Plot it below. Label axes, show initial and final values, show time constants.