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ECE137A, Notes Set 10: Multi-stage example: Analog audio power amplifier

These notes should give you some ideas
on how to approach the second lab assignment

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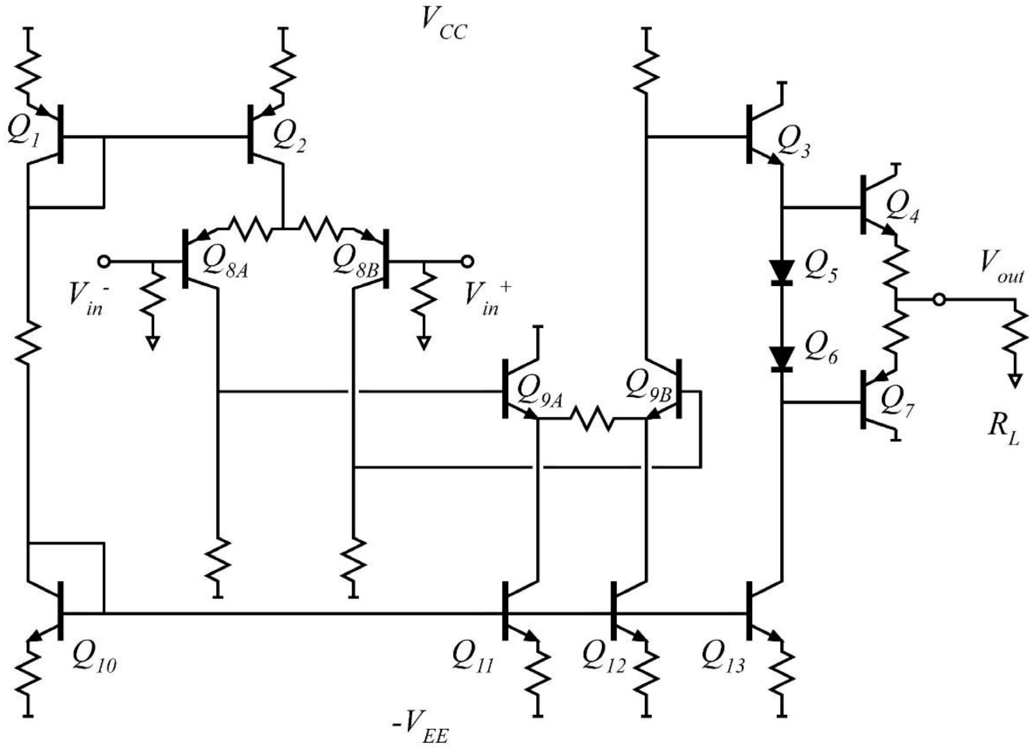
Audio power amplifier example



Q_5 is a diode-connected transistor, and is matched to Q_4.

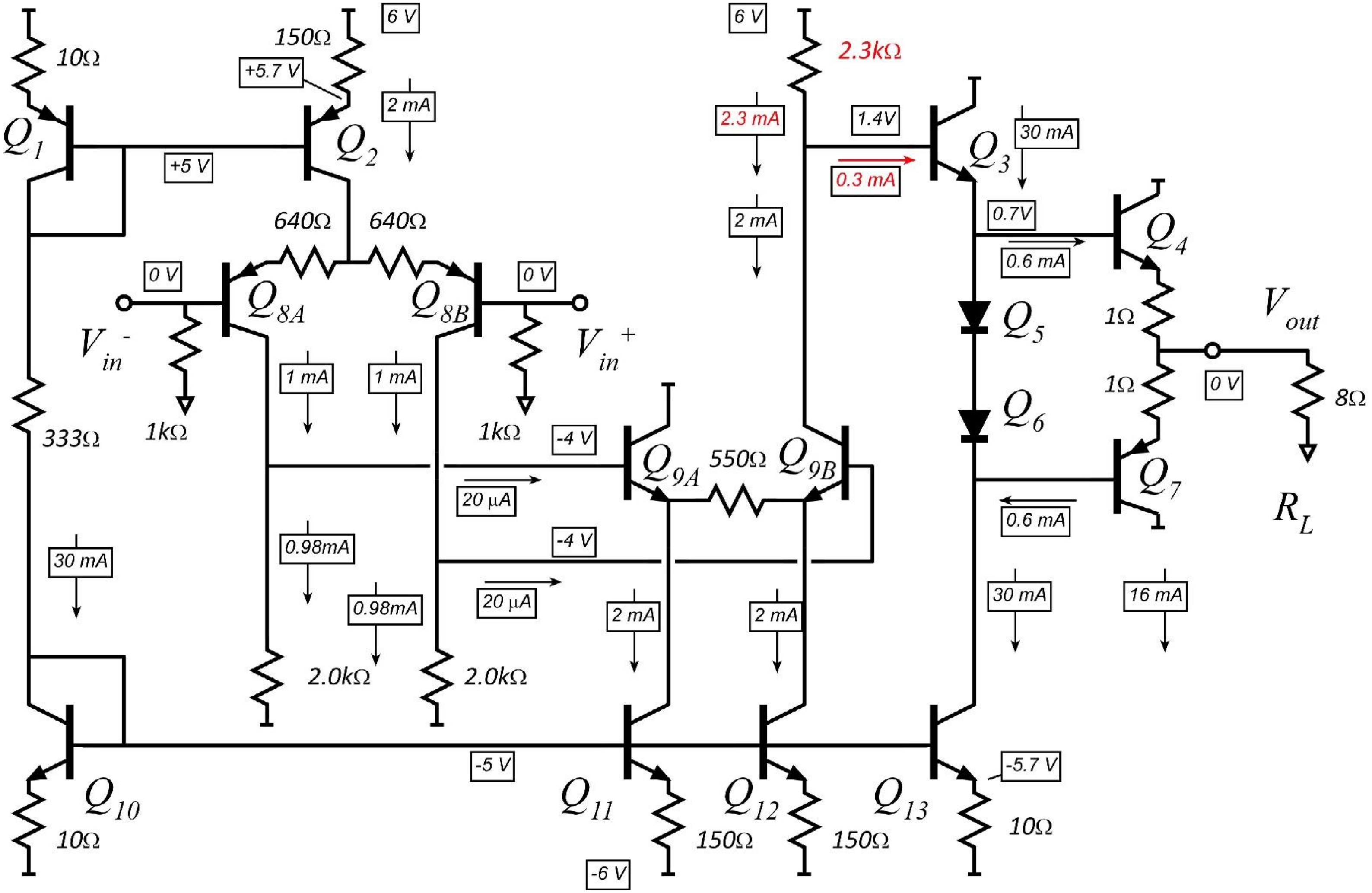
Q_6 is a diode-connected transistor, and is matched to Q_7.

$Q_{4,5,6,7}: \quad \beta_{\min}=25,\ V_A=100\text{V}.$

All other transistors: $\beta_{\min}=100,\ V_A=100\text{V}$

Let us set up DC bias

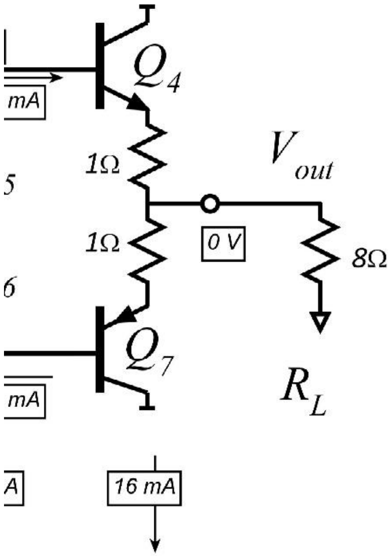
DC bias



Having picked the DC node voltages and DC bias currents,

here are the calculated resistor values... look at previous notes for how to do this.

Small-signal analysis: Q4/Q7



Q_4 and Q_7 are a push-pull stage.

Hand analysis is inherently inaccurate:

over the signal swing, transistor currents vary greatly

g_m and other parameters vary greatly.

effect is real: singal distortion.

Approximate: assume that either Q_4 is Q_7 off. Here, let's pick Q_4 on.

Approximate: use g_m calculated at large output voltage.

At $V_{out}=3\text{V}$, $I_{out}=3\text{V}/8\Omega=0.375\text{A}$. $1/g_m=26\text{mV}/0.375\text{A}=0.07\Omega$

Q_4 : emitter follower.

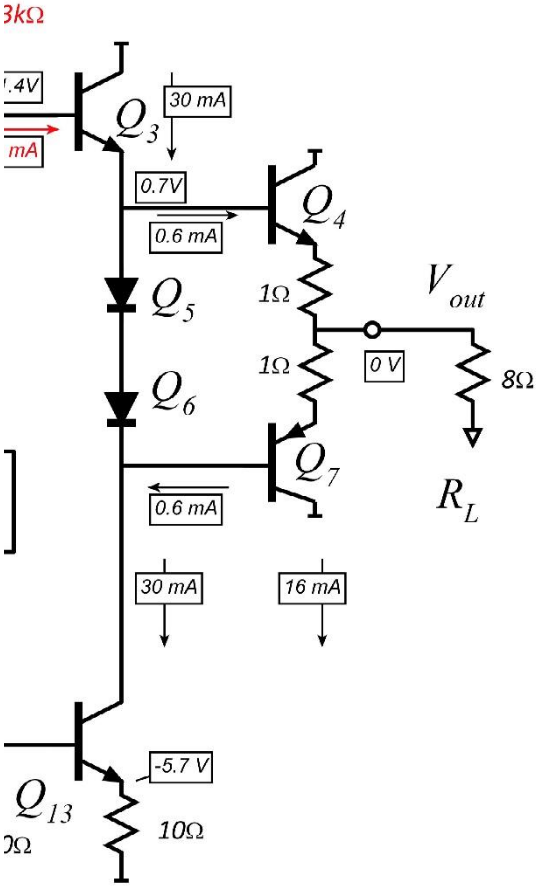
$$R_{Leq}=9\Omega$$

$$A_V=R_{Leq}/(R_{Leq}+1/g_m)=9\Omega/9.07\Omega$$

$$R_{in4}=\beta(R_{Leq}+1/g_m)\geq 25(9.07\Omega)=227\Omega.$$

Including effect of 1Ω resistors: $A_V=(8\Omega/9\Omega)(9\Omega/9.07\Omega)=0.88$

Small-signal analysis: Q3



Q_3 : emitter follower.

$$R_{Leq3} = R_{in4} \parallel R_{CE3} \parallel R_{out13} \parallel R_{in7} \cong R_{in4} = 227\Omega$$

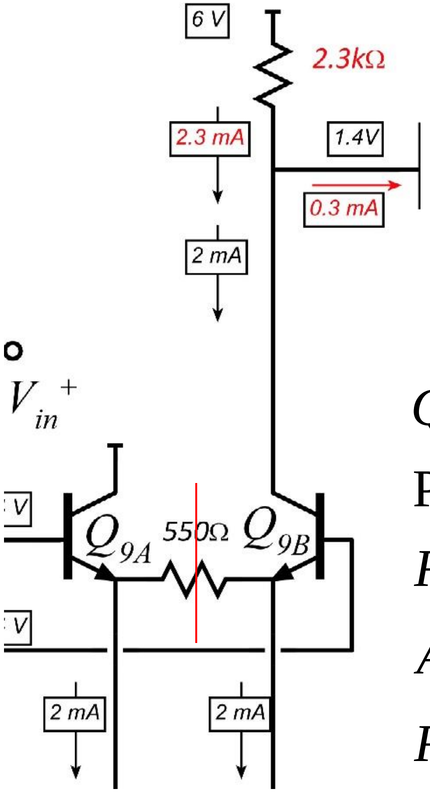
(R_{out13} is very large, and we've assumed Q_7 is off)

$$1/g_{m3} = 26\text{mV}/30\text{mA}=0.866\Omega$$

$$A_V = R_{Leq}/(R_{Leq}+1/g_m) = 227\Omega/227.9\Omega = 0.996$$

$$R_{in3} = \beta(R_{Leq}+1/g_m) \geq 100(228\Omega) = 22.9\text{k}\Omega.$$

Small-signal analysis: Q9A/Q9B



This is a differential pair.

Only one output used → factor of 1/2 is present

Half-circuit: 550Ω/2=275Ω degeneration.

Q_{9B}: Common-emitter with degeneration.

Part of differential pair.

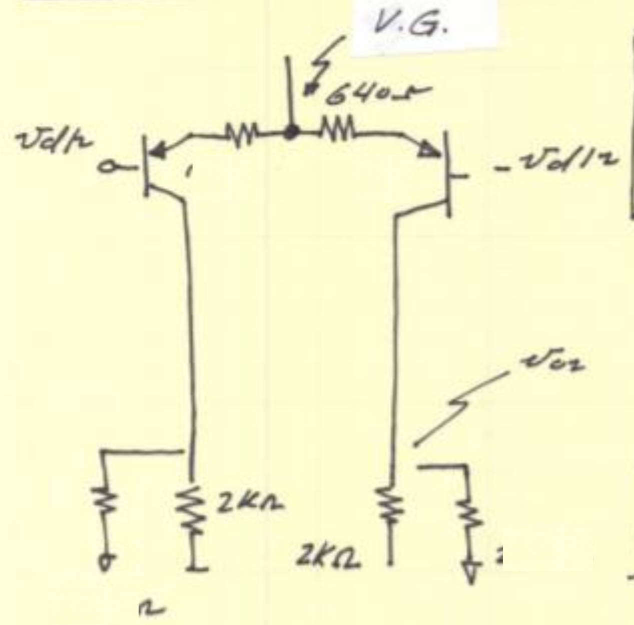
$$R_{Leq} = 2.3\text{k}\Omega \| R_{in3} \,\|\, R_{out9B} \cong 2.3\text{k}\Omega \| R_{in3} = 2.3\text{k}\Omega \| 23\text{k}\Omega = 2.09\text{k}\Omega$$

$$A_{vdiff} = R_{Leq} / 2(1/g_{m9B} + 275\Omega) = 2.09\text{k}\Omega / 2(13\Omega + 275\Omega) = 3.63$$

$$R_{in9B} = \beta(13\Omega + 275\Omega) \geq 100(288\Omega) = 28.8\text{k}\Omega$$

Note that this is the half-circuit input impedance

Small-signal analysis: Q8A/Q8B



If CMRR is large, then differential gain is ≅ single-ended gain

$$R_{Leq} = 2\text{k}\Omega \| R_{in9B} \, \| \, R_{out8B} \cong 2\text{k}\Omega \| R_{in9B}$$

$$= 2\text{k}\Omega \| 29\text{k}\Omega = 1.87\text{k}\Omega$$

Q_{9B}: Common-emitter with degeneration.

Part of differential pair, but both outputs are used

$$A_{vdiff} = R_{Leq} / (1/g_{m9B} + 640\Omega) = 1.87\text{k}\Omega / (26\Omega + 640\Omega) = 2.89$$

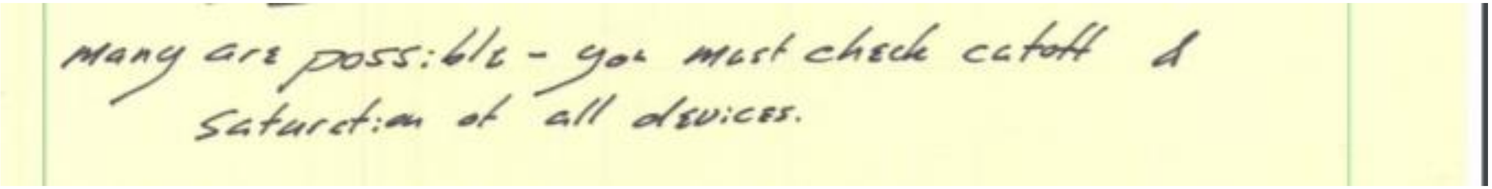
$$R_{in8B} = \beta(26\Omega + 640\Omega) \geq 100(666\Omega) = 66.6\text{k}\Omega$$

$$R_{in,Amp} = 66.6\text{k}\Omega \, \| \, 1\text{k}\Omega = 985\Omega$$

Overall gain: $A_v = 0.88 \cdot 0.966 \cdot 3.63 \cdot 2.89 = 8.91.$

(design target was 10; need to adjust degeneration resistors)

Maximum Signal Swings



many are possible - you must check cutoff & saturation of all devices.

Dominant are:

Saturation of Q_4 and Q_7.

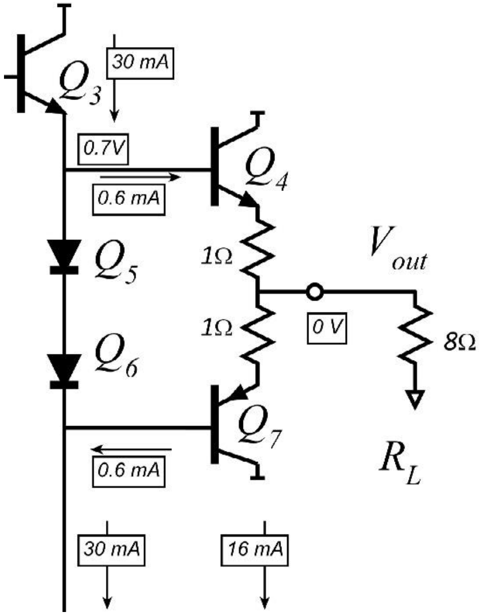
Saturation and cutoff of Q_3.

Saturation of Q_{13}.

Saturation and cutoff of Q_{9B}.

Cutoff of Q_{9A}.

Q4 and Q7 saturation



The maximum positive voltage at the emitter of Q4 is $(V_{CC} - V_{CE,sat})$.

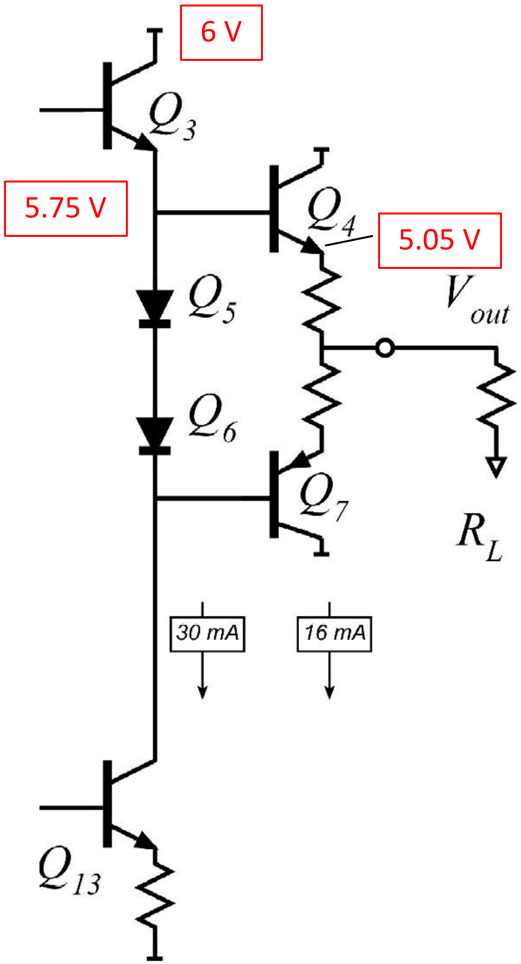
The corresponding output voltage is 8/9 of this.

If $V_{CE,stat} = 0.25\text{V}$, then the maximum output is (8/9)(5.75V)=5.1V.

$\rightarrow$ Maximum 5.1V postive swing due to Q4 saturation.

Q7 saturation similarly limits us to -5.1V negative swing

Q3 saturation



The maximum positive voltage at the emitter of Q3:

$(V_{CC} - V_{CE,sat}) = 6\text{V} - 0.25\text{V}{=}5.75\text{V}.$

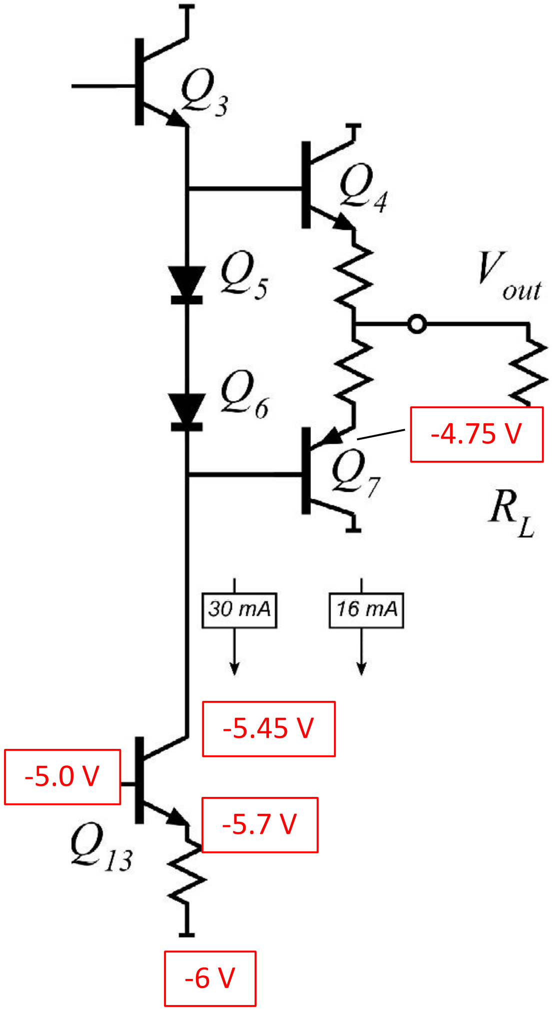
Q_4 emitter voltage=5.75V-0.7V=5.05V

The corresponding output voltage is 8/9 of this.

(8/9)(5.05V)=4.48V.

→ Maximum 4.5V postive swing due to Q3 saturation.

Q13 saturation



The maximum negative voltage at the collector of Q13:

$(-V_{E,Q}+V_{CE,sat})=-5.7\text{V}-0.25\text{V}=-5.45\text{V}.$

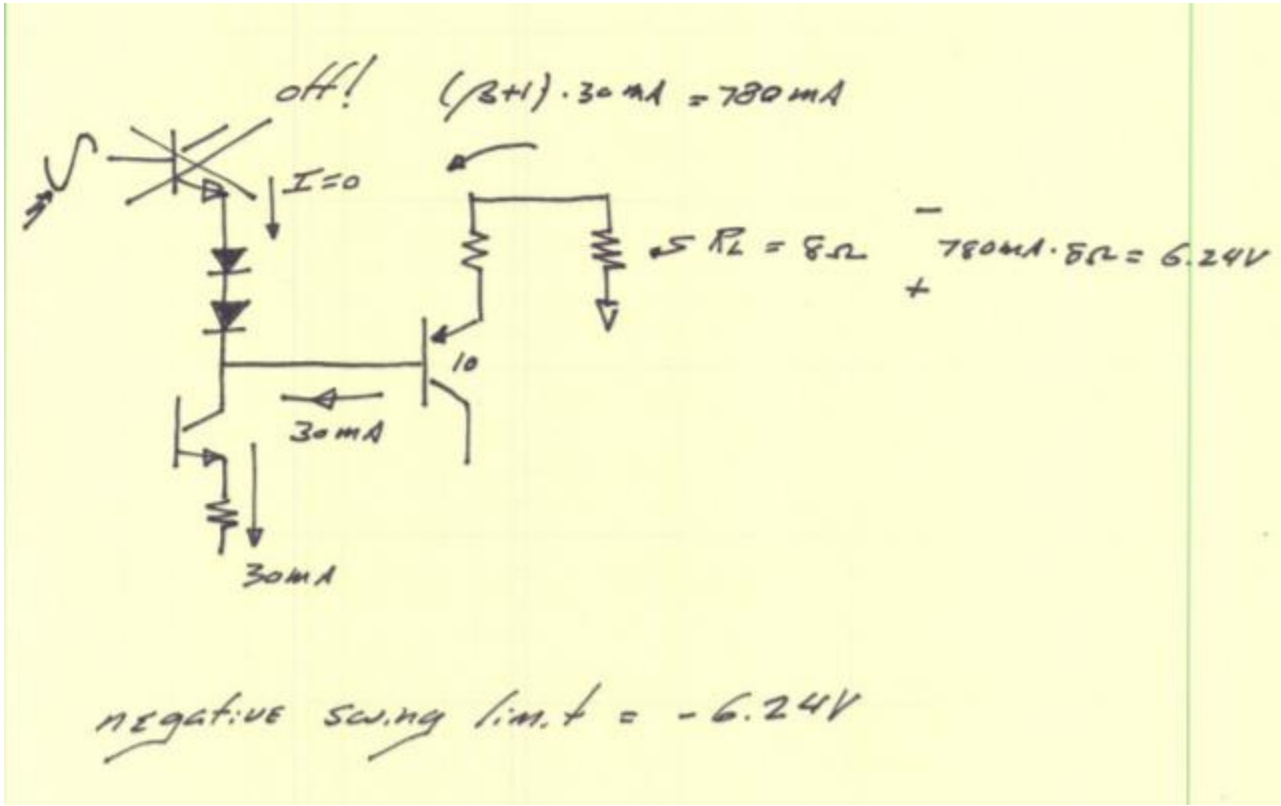
Q_7 emitter voltage$=-5.45\text{V}+0.7\text{V}=-4.75\text{V}$

The corresponding output voltage is 8/9 of this.

$(8/9)(-4.75)=-4.2\text{V}.$

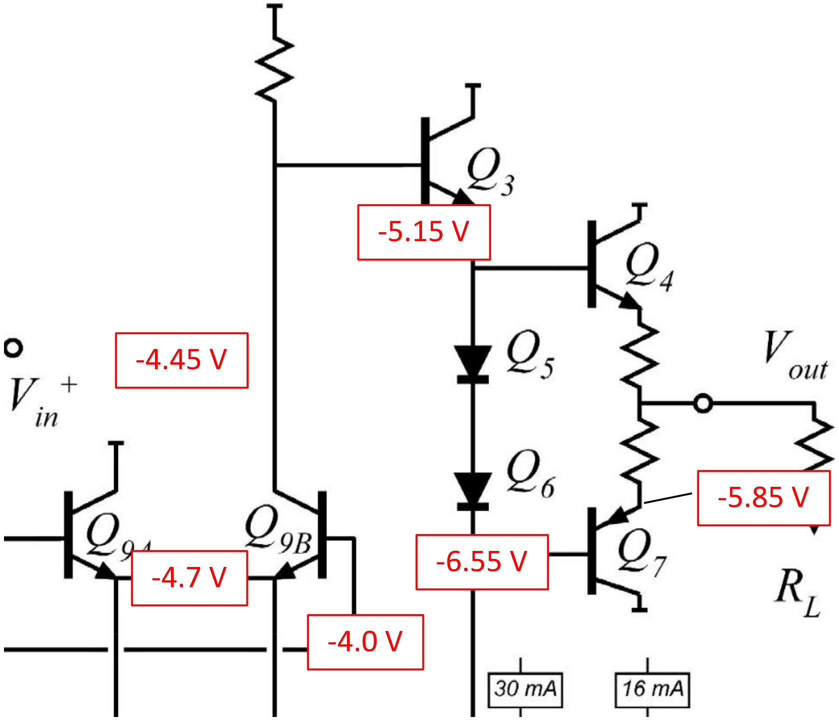
$\rightarrow$ Maximum -4.2V negative swing due to Q13 saturation.

Q13 cutoff



This is the same as saying that the maximum base current of Q_7 is the bias current of Q_{13}.

Q9B saturation



See the circuit diagram: it is easier than using words.

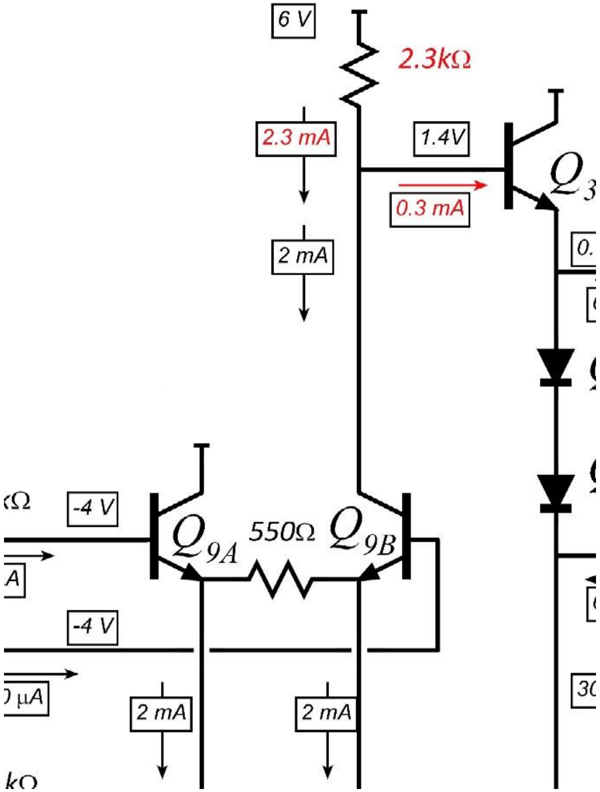
Maximum negative voltage at Q7 emitter: -5.85V

The corresponding output voltage is 8/9 of this.

$(8/9)(-5.85) = -5.2\text{V}.$

$\rightarrow$ Maximum -5.2V negative swing due to Q9B saturation.

Q9A and Q9B cutoff



Q9B cuttoff reduces I_{C9B} by 2mA.

Q9A cuttoff *increases* I_{C9B} by 2mA.

$\rightarrow \pm$2mA maximum signal current from Q9B.

$R_{Leq9B} = 2.0\text{k}\Omega.$

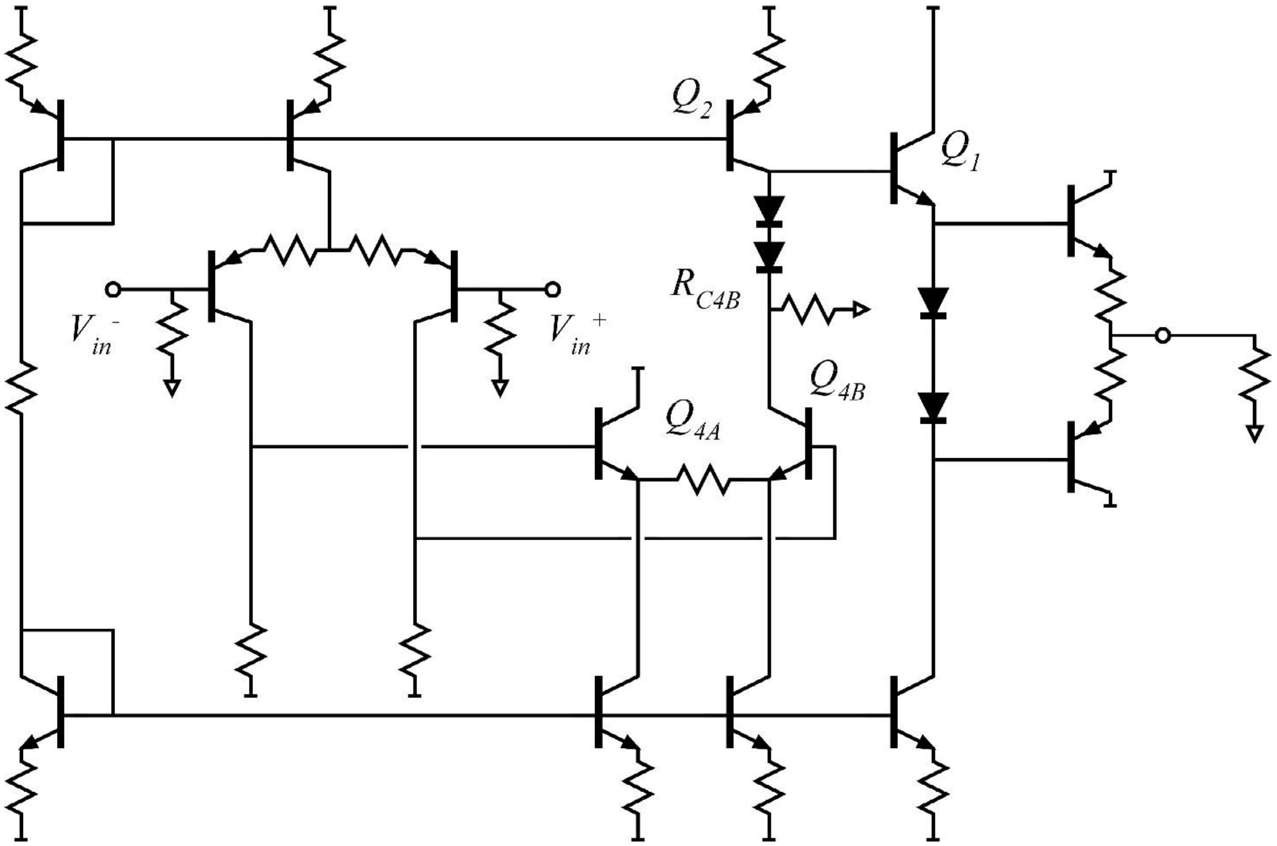
$$\Delta V_{out,Q9B}\Big|_{\max} = \pm 2\text{mA}\cdot 2.0\text{k}\Omega = \pm 4\text{V}.$$

$$\Delta V_{out,amplifier}\Big|_{\max} = \pm 4\text{V}\cdot A_{v3}A_{v4} = \pm 4\text{V}\cdot 0.996\cdot 0.88$$

$$\Delta V_{out,amplifier}\Big|_{\max} = \pm 3.5\text{V}$$

In this design, Q9AB cutoff is our most serious limit to output swing (it depends, of course, on the #s you pick, but the circuit topology you select also plays a role)

Other ideas (1)



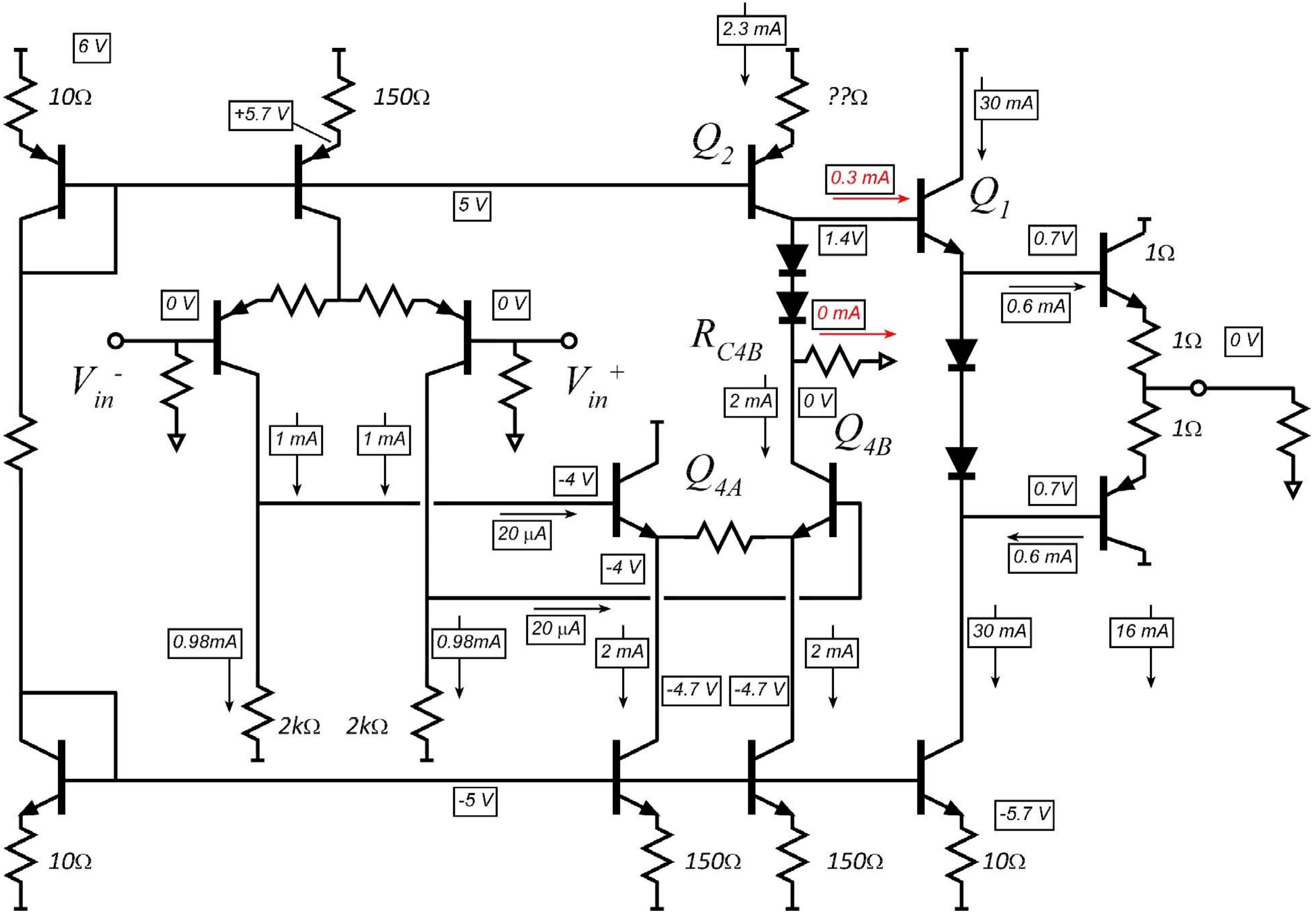
This is a way of attacking the problem of cutoff of Q_{4AB}.

Why might this help ?

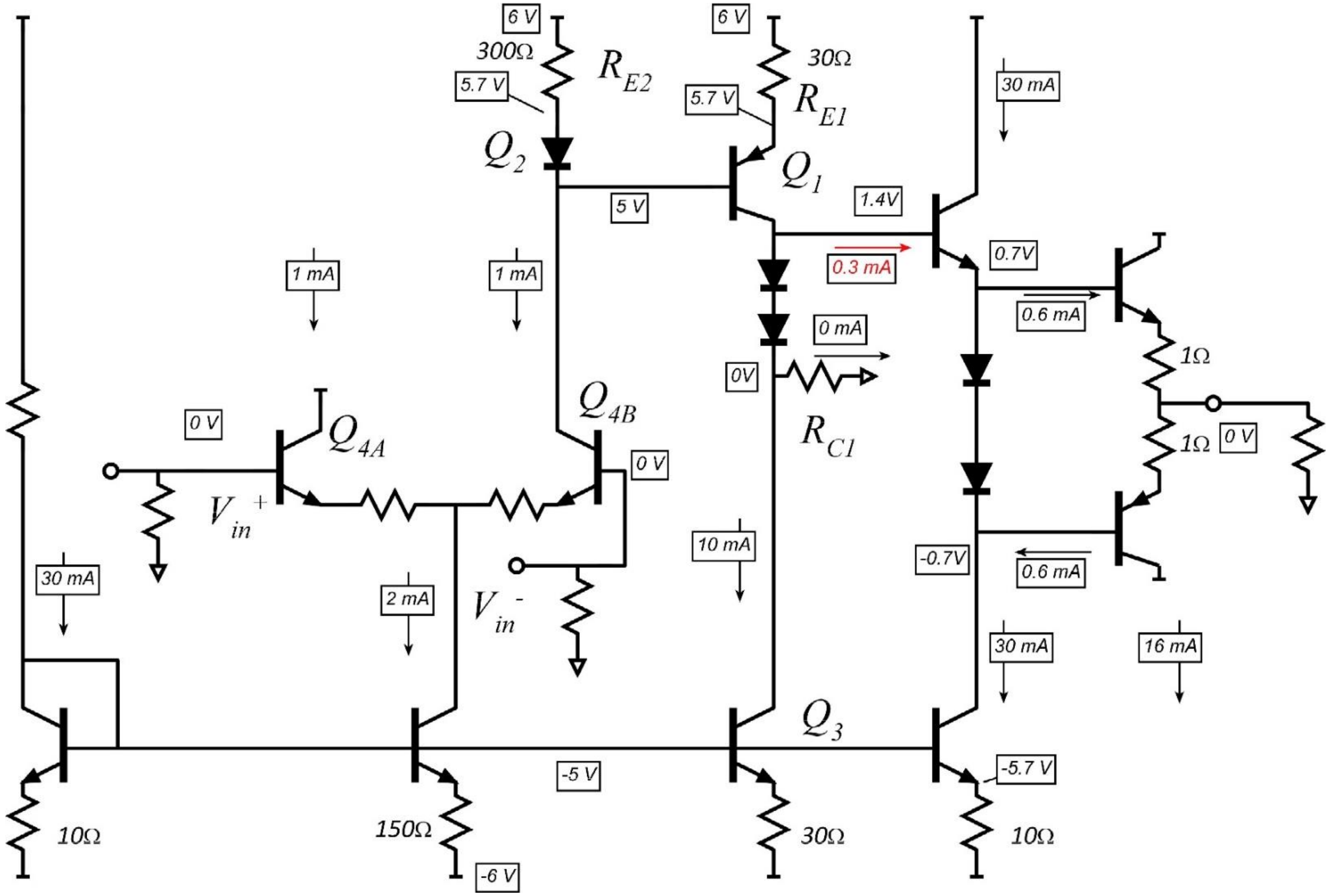
How might you choose the bias current in Q_{4AB} ?

How might you pick R_{C4B}? Why are there two diodes in series with the collector of Q2?

Other ideas (1)



Other ideas (2)



In this design, the 2nd voltage gain stage is not differential. Hint: once you examine clipping limits, you will find that Q1must be designed with substantial voltage gain. This then forces you to design Q4A/4B with low voltage gain. Note that in terms of DC bias, Q1/Q2 are a current mirror. Precise control of DC bias might be a problem

Other ideas (3)