ECE137A, Notes Set 14:
Op-Amps

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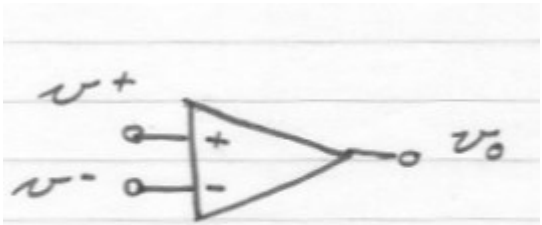
Operational Amplifier

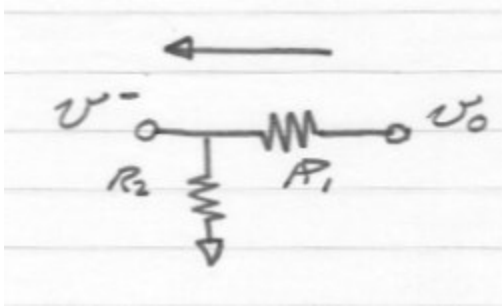


$$V_{out} = A_D (V^+ - V^-)$$

Characteristics of op-amp:

A_d is very large. Very large CMRR

Large R_{in}. Small R_{out}

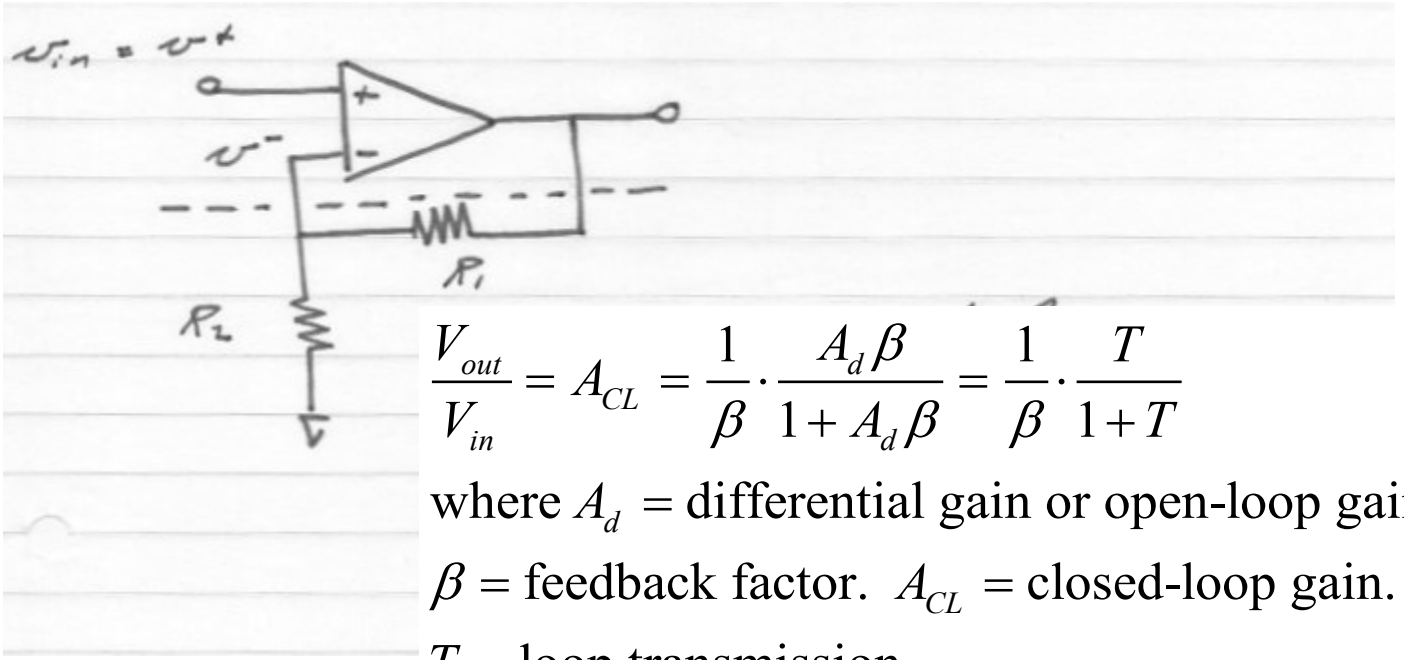


Example of feedback network:

$V^- = \beta V_{out}$ where $\beta = R_2 / (R_1 + R_2)$

Operational Amplifier with Feedback

Combine these:



$$\frac{V_{out}}{V_{in}} = A_{CL} = \frac{1}{\beta}\cdot\frac{A_d\beta}{1+A_d\beta} = \frac{1}{\beta}\cdot\frac{T}{1+T}$$

where A_d = differential gain or open-loop gain, a.k.a. A_{OL}

β = feedback factor. A_{CL} = closed-loop gain.

T = loop transmission

$$\frac{V_{out}}{V_{in}} = A_{CL} = \begin{cases} 1/\beta \text{ if } T >> 1 \\ A_d \text{ if } T << 1 \end{cases}$$

If the loop transmission is very large,

the closed-loop gain is precisely set by the feedback factor

Negative feedback

Feedback can provide precise control of circuit gain.
If $A_d\beta$ is large, then the gain is contolled by the feedback resistors

Note that the external feedback components also set the DC bias.

Op-amp bias is almost always set by the feedback network:
For now, analyze by assuming that Vout=0V,
and work back to the input to find (V^+-V^-).

An op-amp is an amplifier that:
is designed for use with feedback
operates usually over a range of supply voltages
has a very large voltage gain
usually (not always) has a large input impedance
usually (not always) has a small output impedance
is designed to not oscillate when feedback is applied (see ece137B)

Bias analysis of op-amps

There will be a small mismatch between input transistors, and possibly also of their load, etcetera. As a result:

$$V_{out} = A_d (V_d + V_{os}) = A_d (V_{in}^+ - V_{in}^- + V_{os})$$

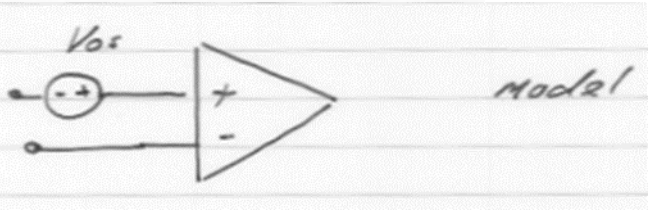
Vos is called the offset voltage, and might be 0.1-10mV.
If A_d=10^6 and V_{os}=1mV, then a zero-volt input would force the output to clipping.

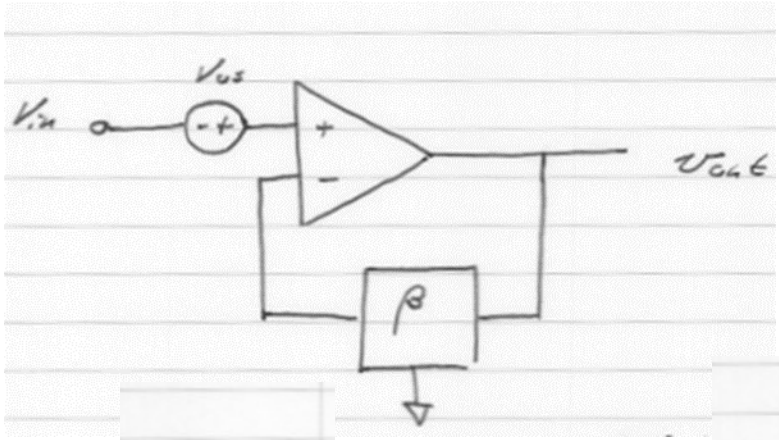
Consequently, op-amps are always used with feedback

DC analysis is performed by assuming that V_{out}=0V,
and working backward to find the required V_d to obtain this.
This value of V_d is the offset voltage V_{os}.

Finding Vout given an offset voltage

$$V_{out} = A_d (V_d + V_{os})$$





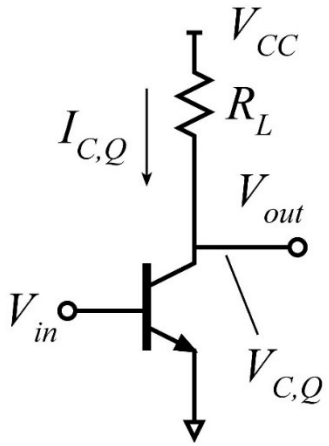
$$v_{out} = A_d \left[v_{in} + v_{os} - \beta v_{out} \right]$$

$$v_{out} = \frac{1}{\beta} \frac{T}{1+T} \left(v_{in} + v_{os} \right) \quad ; \; T = A_d \beta$$

v_{os} is simply amplified by the closed-loop gain.

How to get high voltage gain ?

We seek $A_D\beta >> 1$, so large op-amp gain is desired.

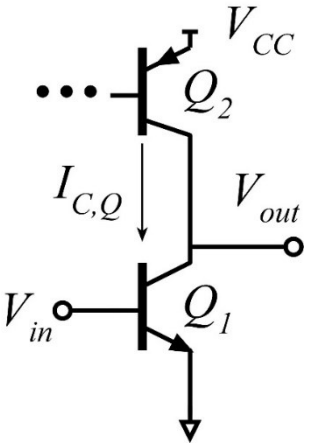


Suppose $V_{CQ} << V_{CC} \rightarrow R_L \cong V_{CC} / I_C$

$-A_V = g_m R_{Leq} = g_m (R_L \,||\, R_{CE}) < g_m R_L = (I_C / V_T)(V_{CC} / I_C) = V_{CC} / V_T$

If $V_{CC} = 10\text{V}$, then $||A_V|| < 10\text{V}/26\text{mV} \cong 400$

$\rightarrow$ gain is limited by the power supply



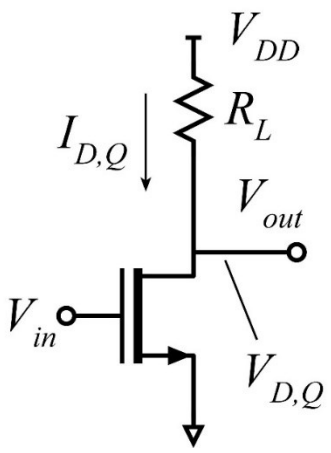
Suppose $V_{A1} = V_{A2}$ Then $R_{CE1} = R_{CE2} = V_A / I_C$

$-A_V = g_{m1} R_{Leq} = g_{m1} (R_{CE1} \,||\, R_{CE2}) = (I_C / V_T)(V_A / 2I_C) = V_A / 2V_T$

If $V_A = 100\text{V}$, then $||A_V|| = 50\text{V}/26\text{mV} \cong 2000$

$\rightarrow$ gain is limited by the Early voltage

How to get high voltage gain ?



Suppose $V_{DQ} << V_{DD} \rightarrow R_L \cong V_{DD} / I_D$

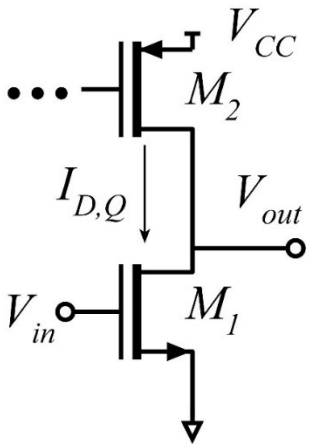
$-A_V = g_m R_{Leq} = g_m (R_L \parallel R_{DS}) < g_m R_L$; now assume mobility-limited

$= (2I_D / (V_{GS} - V_{TH}))(V_{DD} / I_D) = 2V_{DD} / (V_{GS} - V_{TH})$

but only if $(V_{GS} - V_{TH}) > 2V_T$; otherwise $g_m = I_D / nV_T$

If $V_{CC} = 1\text{V}$, then $\|A_V\| \le 1\text{V}/(n \cdot 26\text{mV}) \le 1\text{V}/26\text{mV} \cong 40$

$\rightarrow$ gain is limited by the power supply. Need low $(V_{GS} - V_{TH})$



Suppose $\lambda_1 = \lambda_2$ Then $R_{DS1} = R_{DS2} = 1/\lambda I_D$

$-A_V = g_{m1} R_{Leq} = g_{m1} (R_{DS1} \parallel R_{DS2})$; now assume mobility-limited

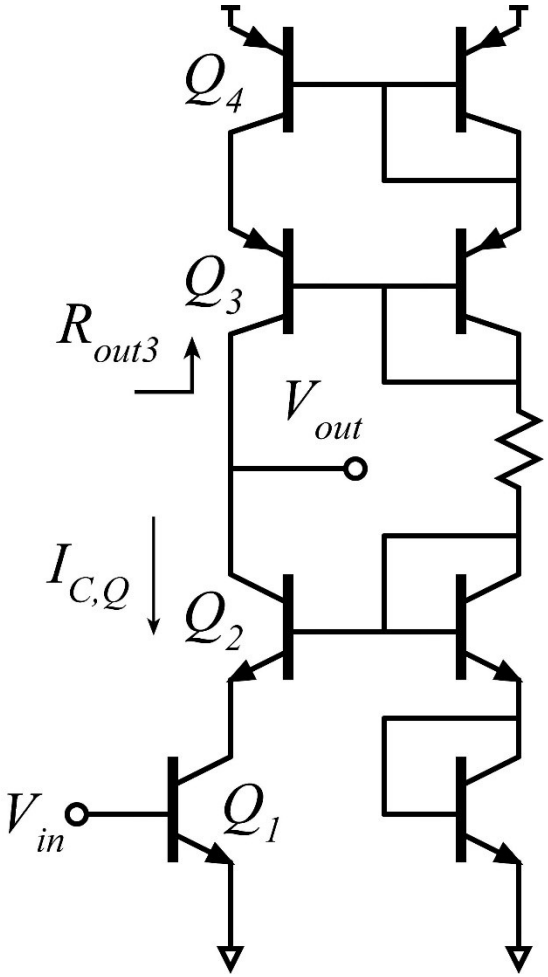
$= (2I_D / (V_{GS} - V_{TH}))(1 / 2\lambda I_D) = 1 / (\lambda (V_{GS} - V_{TH}))$

but only if $(V_{GS} - V_{TH}) > 2V_T$; otherwise $g_m = I_D / nV_T$

If $1/\lambda = 4\text{V}$, then $\|A_V\| \le 4\text{V}/(2 \cdot n \cdot 26\text{mV}) \le 4\text{V}/52\text{mV} \cong 80$

$\rightarrow$ gain is limited by $(1/\lambda)$. Need low $(V_{GS} - V_{TH})$.

Cascodes for high voltage gain



Approximate: Assume impedances presented to bases are small

Note: $g_{m1} = g_{m2} = g_{m3} = g_{m1}$ and $R_{CE1} = R_{CE2} = R_{CE3} = R_{CE4}$

$Q2$: common gate

$$R_{out3} = R_{CE}(1 + g_m R_{CE}) \cong g_m R_{CE}^2$$

$$R_{Leq2} = R_{out3}$$

$$R_{in2} = (1/g_m)(1 + R_{Leq3}/R_{CE}) \cong R_{CE} \quad (!)$$

$$A_{V2} = R_{Leq2}/R_{in2} = g_m R_{CE}$$

$Q1$: common-source

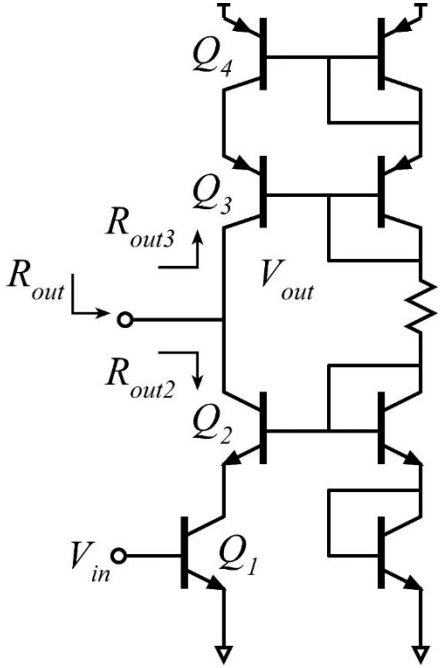
$$R_{Leq1} = R_{CE1} \,||\, R_{in2} = R_{CE} \,||\, R_{CE} = R_{CE}/2$$

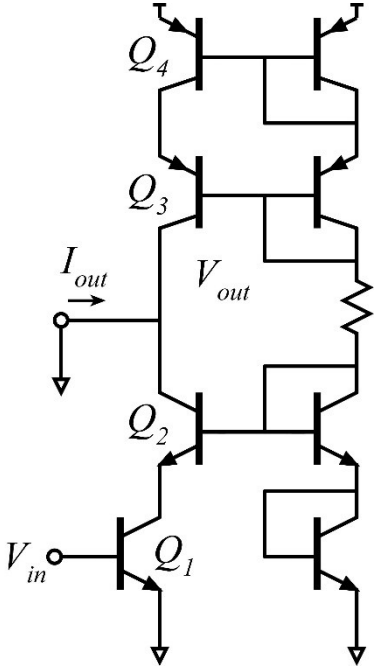
$$A_{V1} = -g_m R_{Leq1} = -g_m R_{CE}/2 \quad (!)$$

Overall: $A_V = A_{V1}A_{V2} = -(g_m R_{CE})^2/2 = -(V_A/V_T)^2/2$

If $V_A = 100\text{V}$ then $-A_V = (100\text{V}/26\text{mV})^2/2 \cong (4000)^2/2 = 8 \cdot 10^6$

Cascode: alternate analysis





Norton (output) resistance

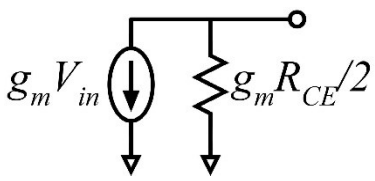
$R_{out2} = R_{out3} \cong g_m R_{CE}^2$

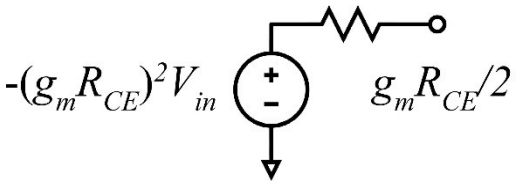
$R_{out} = R_{out3} \,||\, R_{out2} \cong g_m R_{CE}^2 / 2$

Norton (output) current

R_{in2} is now $1/g_m$, so $R_{in2} << R_{CE1}$, so

$I_{out} \cong g_m V_{in}$

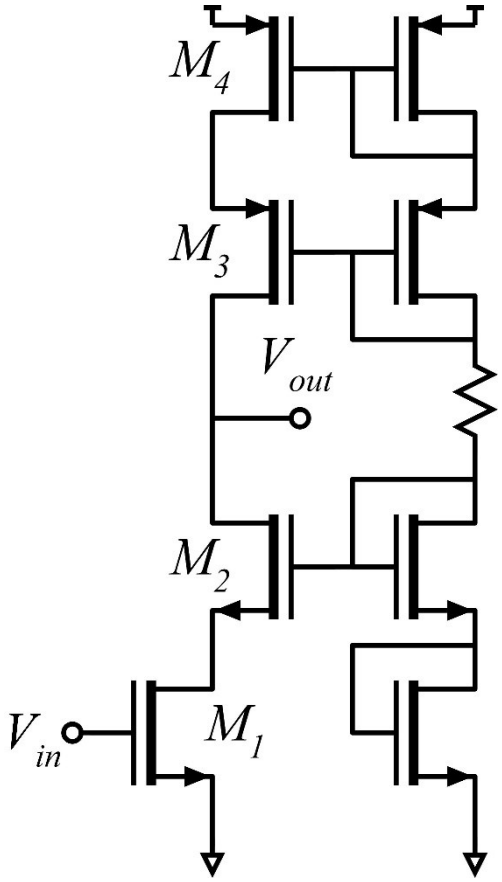




Norton and Thevenin models:

voltage gain is $-(g_m R_{DS})^2 / 2$

FET Cascode



By the same analysis (either method)

$$A_V = A_{V1}A_{V2} = -(g_m R_{DS})^2 / 2$$

If we assume mobility-limited operation,

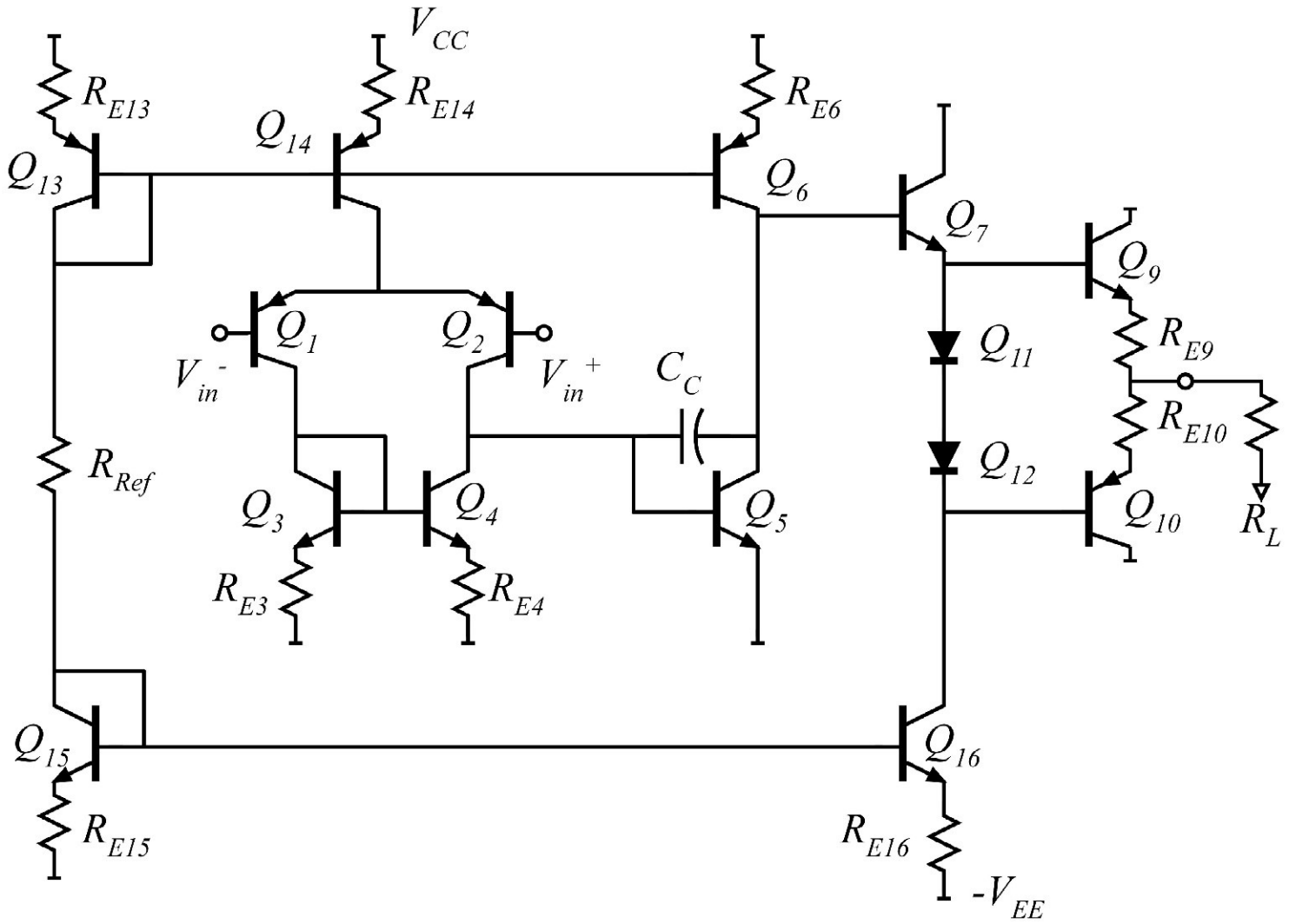
take $R_{DS} = 1/\lambda I_D$

and $g_m = 2I_D / (V_{GS} - V_{TH}) < I_D / nV_T$,

then $A_{V1}A_{V1} = (2/\lambda(V_{GS} - V_{TH}))^2 / 2 \le (1/\lambda n V_T)^2$

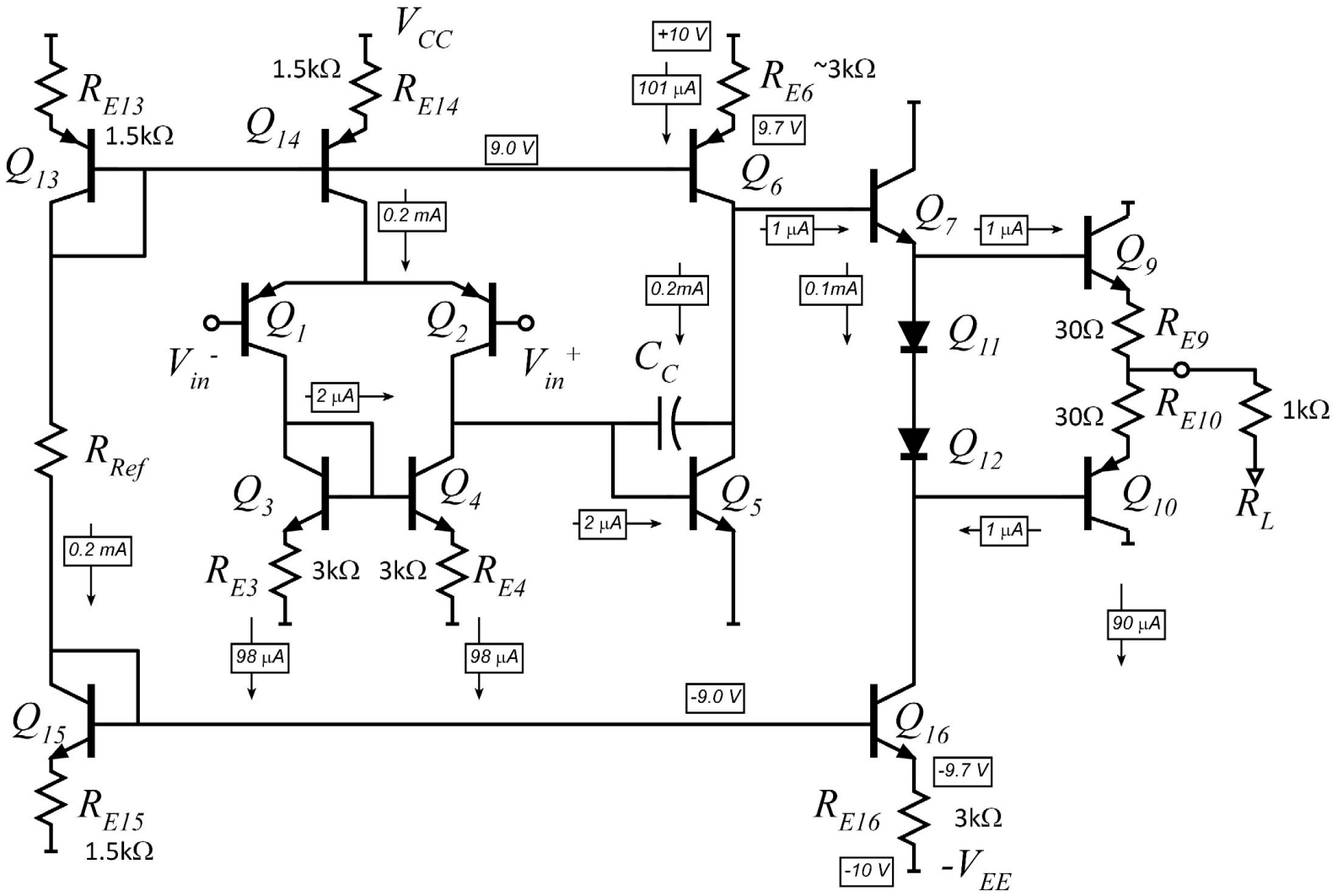
Example: $1/\lambda = 4\text{V}$, $(V_{GS} - V_{TH}) = 0.1\text{V} \rightarrow |A_{V1}A_{V2}| = 800$

A simple op-amp



The compensation capacitor C_C will be explained in ece137B

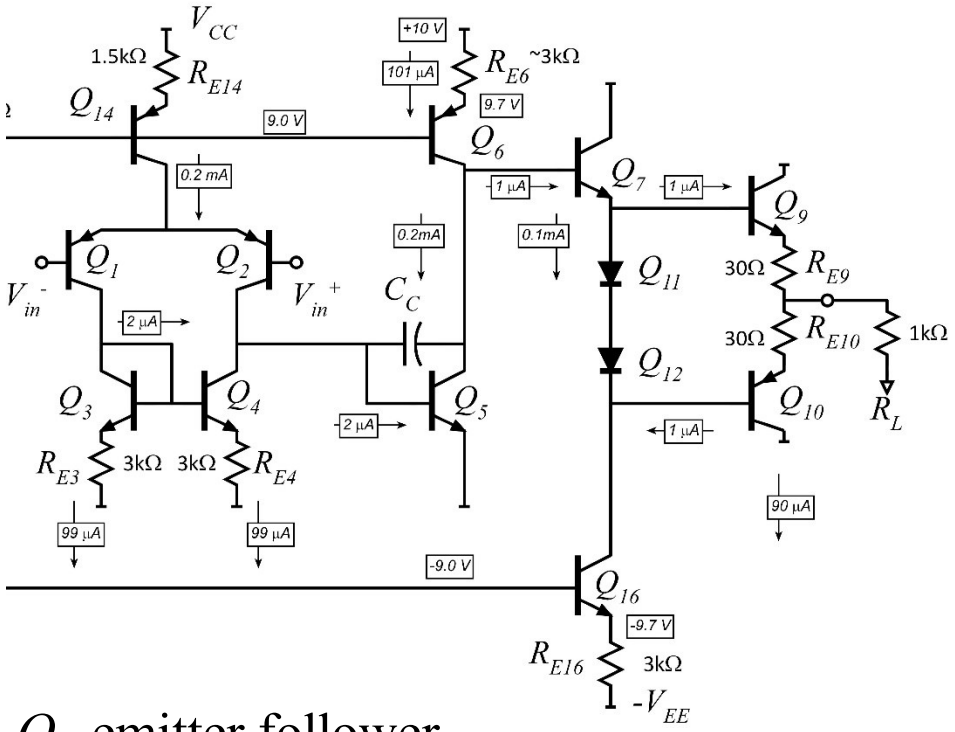
A simple op-amp: DC bias



Assume that all transistors have identical I_S

$\beta = 100,\ V_A = 100\text{V}$

A simple op-amp: Small-signal (1)



Q_9 / Q_{10} : push-pull. Assume Q_9 is on.

Assume $V_{out} = 1\text{V} \rightarrow I_{E9} = 1\text{mA}.$

$g_{m9} = 1/26\Omega$

$R_{Leq9} \cong 1030\Omega$

$A_{v9} = R_{Leq9} / (R_{Leq9} + 1/g_m)$

$= 1000\Omega / (1030\Omega + 26\Omega) = 0.947$

$R_{in9} = \beta(R_{Leq9} + 1/g_{m9}) = 100 \cdot 1056\Omega$

$\cong 100\text{k}\Omega$

Q_7 emitter follower.

$g_{m7} = 1/260\Omega$

$R_{CE7} \cong R_{CE16} = V_A / I_C \cong 100\text{V}/0.1\text{mA}=100\text{k}\Omega$

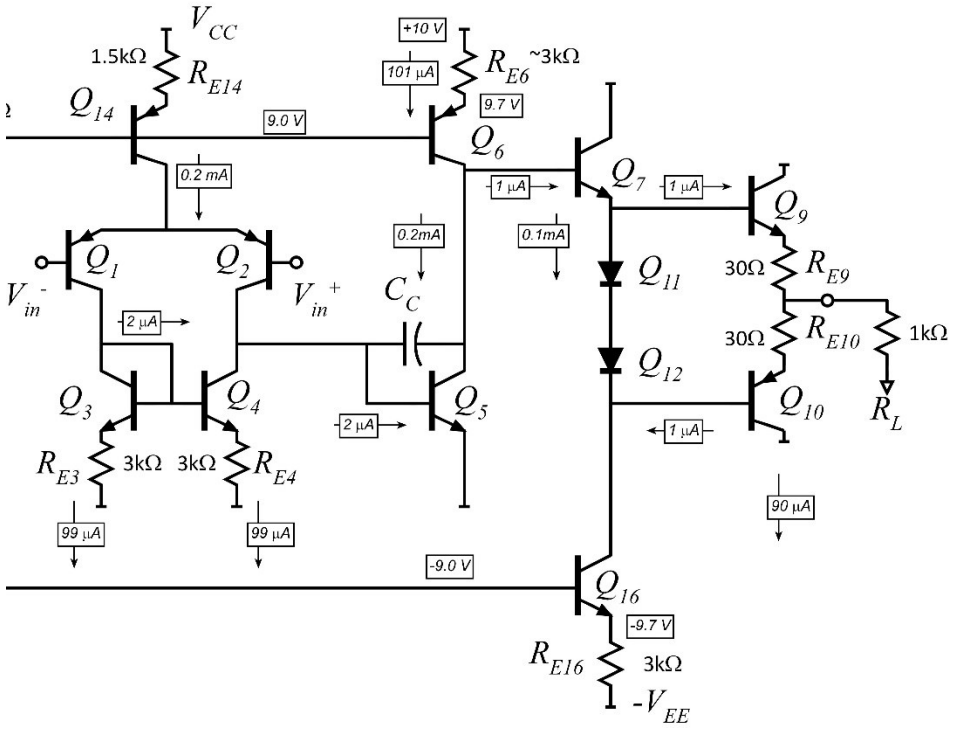
$R_{Leq7} = R_{CE7} \parallel R_{CE16} \parallel R_{in9} = 33.3\text{k}\Omega.$

$A_{v7} = R_{Leq7} / (R_{Leq7} + 1/g_m) = 33.3\text{k}\Omega / (33.3\text{k}\Omega + 260\Omega) = 0.992$

$R_{in7} = \beta(R_{Leq7} + 1/g_{m7}) = 100 \cdot 33.6\text{k}\Omega$

$\cong 3.3\text{M}\Omega$

A simple op-amp: Small-signal (2)



Q_5 common emitter

$$g_{m5} = 1/130\Omega$$

$$R_{CE5} \cong R_{CE16} = V_A / I_C$$

$$\cong 100\text{V}/0.2\text{mA}=500\text{k}\Omega$$

$$R_{out6} \cong R_{CE6}(1+g_{m6}R_{E6})$$

$$= 500\text{k}\Omega(1+3\text{k}\Omega/130\Omega) = 12\text{M}\Omega$$

$$R_{Leq5} = R_{CE5} \,||\, R_{out6} \,||\, R_{in7} =$$

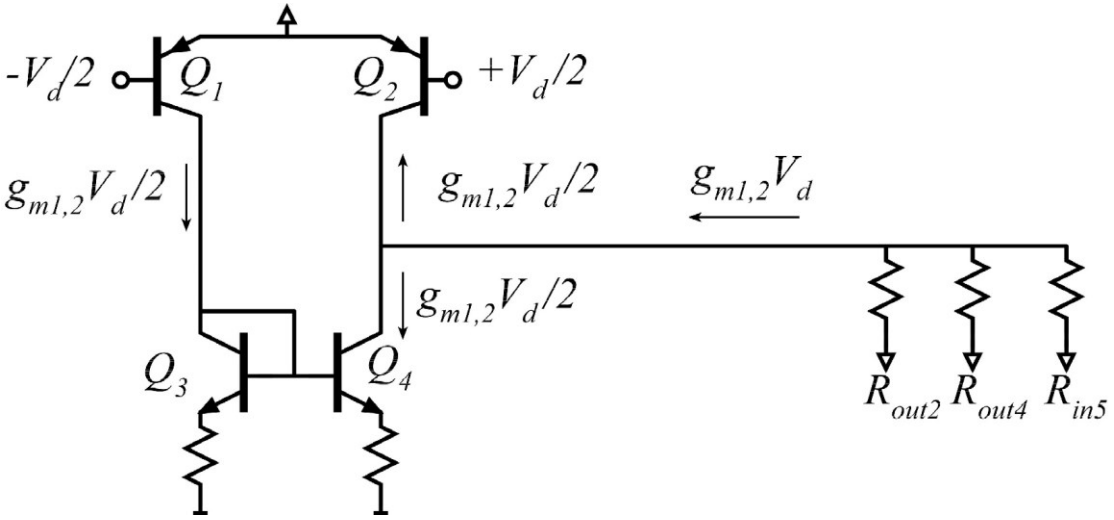
$$= 500\text{k}\Omega \,||\, 12\text{M}\Omega \,||\, 3.3\text{M}=419\text{k}\Omega$$

$$A_{v5} = -g_{m5}R_{Leq5} = -419\text{k}\Omega/130\Omega$$

$$= -3200$$

$$R_{in5} = \beta / g_{m5} = 100 \cdot 130\Omega = 13\text{k}\Omega$$

A simple op-amp: Small-signal (3)



$$g_{m1,2,4,3} = 1/260\Omega$$

$$R_{CE1,2,3,4} = V_A / I_C \cong 100\text{V}/0.1\text{mA}=1\text{M}\Omega$$

$$R_{out4} \cong R_{CE4}(1+g_{m4}R_{E4}) = 1\text{M}\Omega(1+3\text{k}\Omega/260\Omega) = 12.5\text{M}\Omega$$

$$R_{Leq1,2,3,4} = R_{CE2} \parallel R_{out4} \parallel R_{in5} = 1\text{M}\Omega \parallel 12.5\text{M}\Omega \parallel 13\text{k}\Omega \cong 13\text{k}\Omega$$

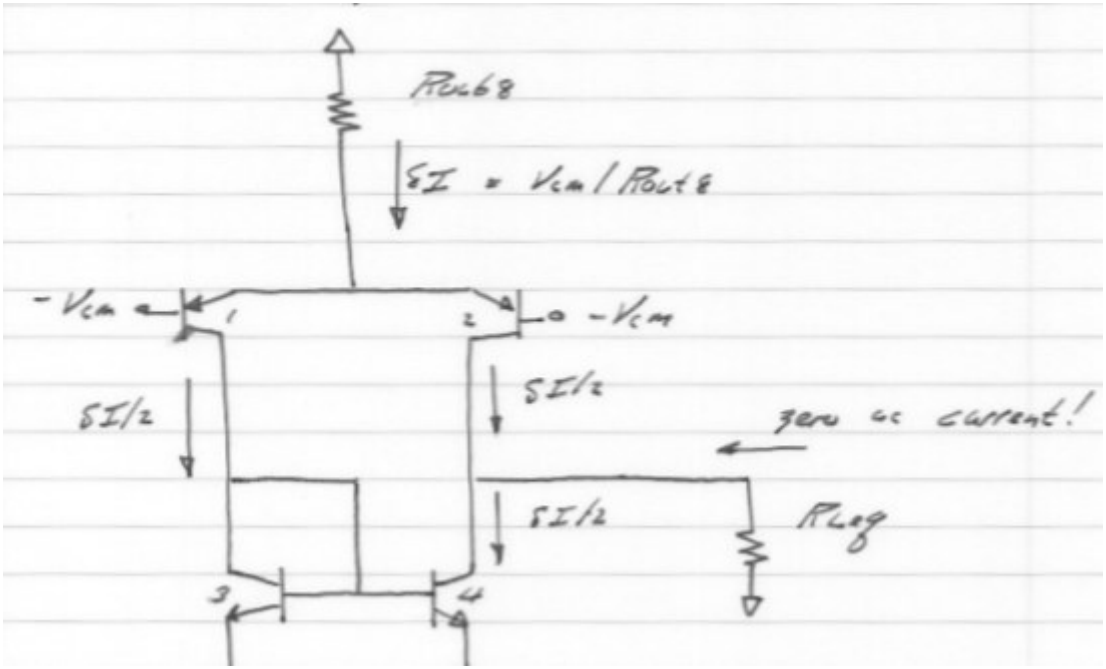
$$A_{v1,2,3,4} = g_{m1,2}R_{Leq} = 13\text{k}\Omega/260\Omega = 50$$

$$R_{in,diff} = 2\beta / g_{m1,2} = 2\cdot 100\cdot 260\Omega = 52\text{k}\Omega$$

Overall differential gain:

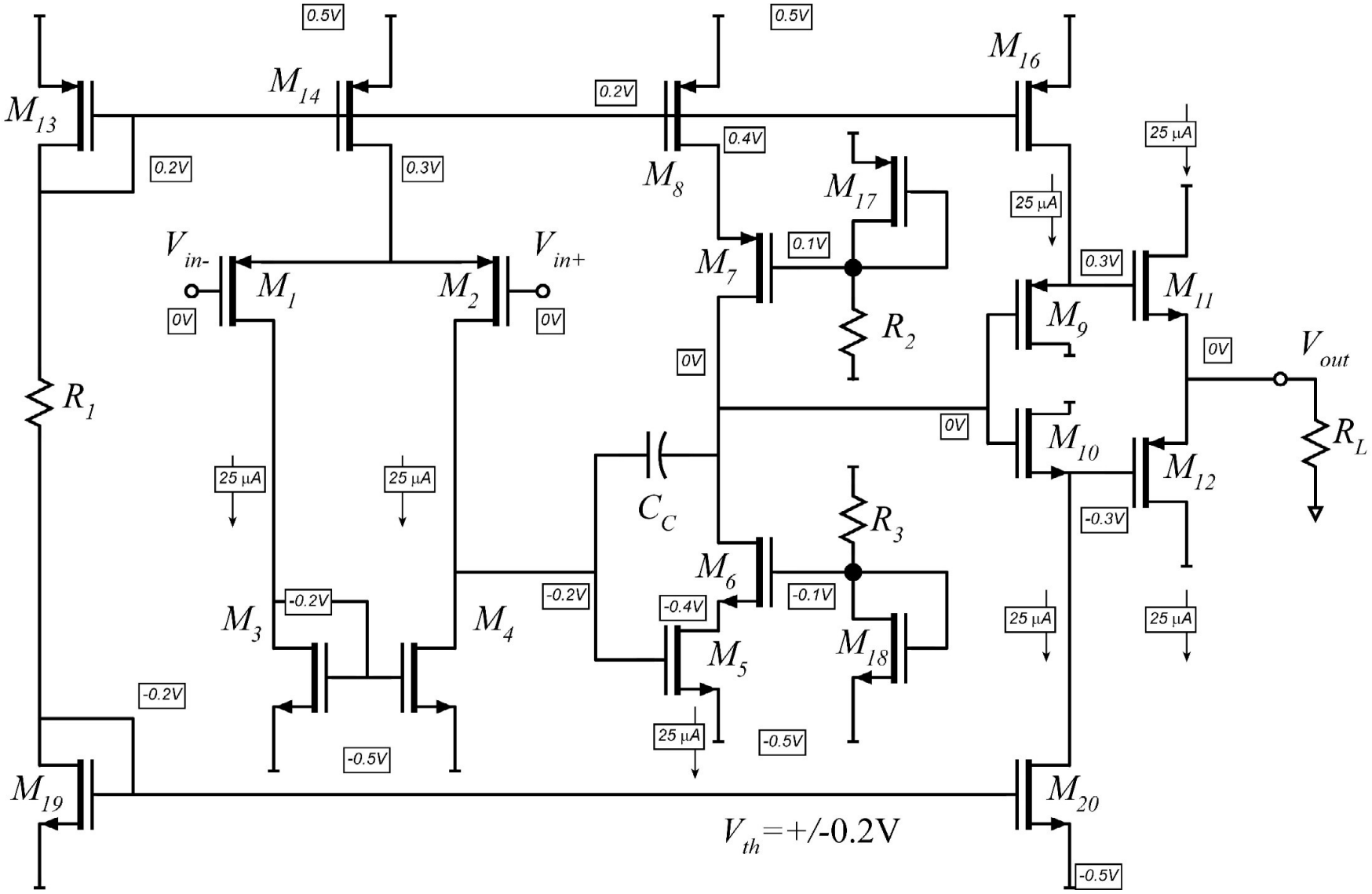
$$A_d = 50\cdot 3200\cdot 0.992\cdot 0.947 = 150,000$$

Common-mode gain (?)

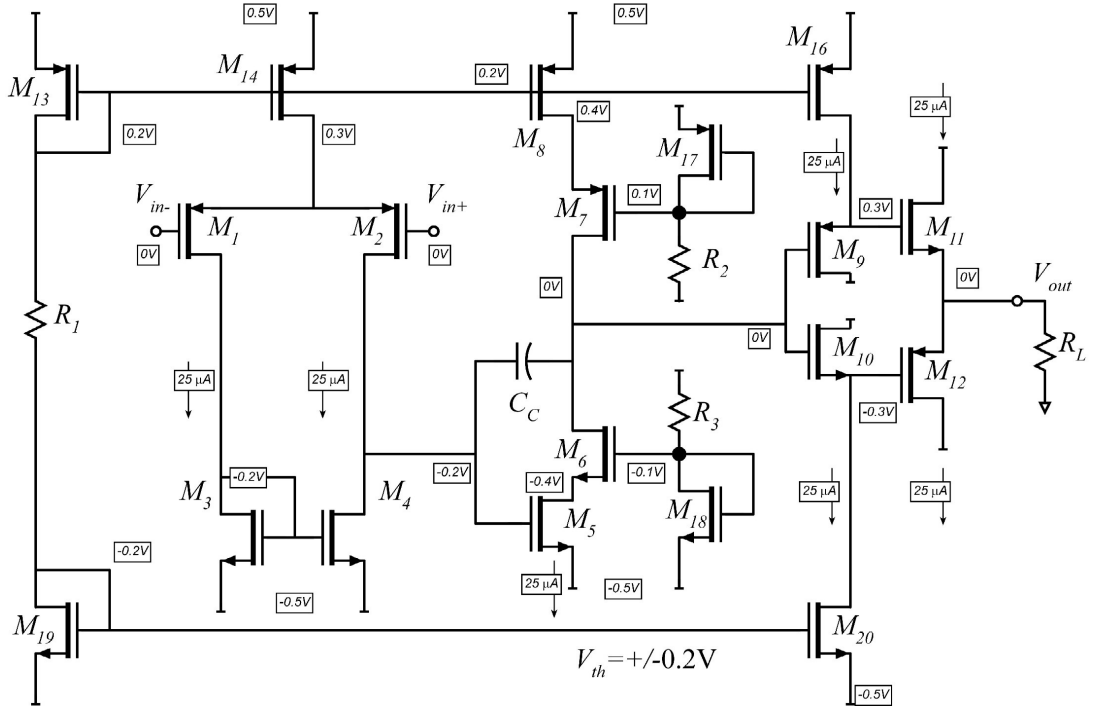


The above analysis suggests infinite cmRR.
It needs to be repeated given assumed
mismatches between Q1-Q2 and Q3-Q4.

Low-voltage CMOS Amplifier



Low-voltage CMOS Amplifier: Comments



FETs:

$K_\mu = 10\text{mA/V}^2 (W_g / 1\mu\text{m})$

$K_v = 2\text{mA/V} (W_g / 1\mu\text{m})$

$\Delta V = 0.1\text{V}$

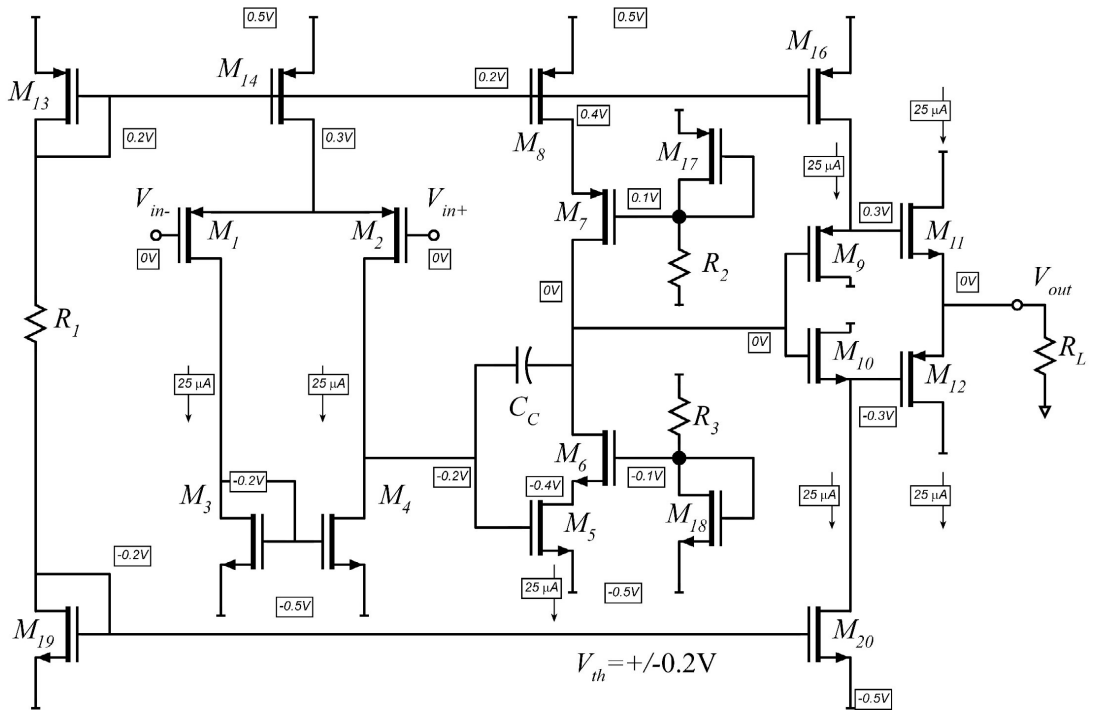
$V_{th} = \pm 0.2\text{V}$

$1/\lambda = 4\text{V}$

Despite the cascode gain stage and the push-pull output stage,
this design can operate with +/- 0.5V supplies and yet provide +/- 0.1V output

Most on-wafer CMOS op-amps do not need to drive significant output current and therefore have no source-follower output stage. Much larger voltage swings are then possible.

Low-voltage CMOS Amplifier



With all FETs except M17,18 operating at $V_{gs} = \pm 0.3\text{V}$ and $V_{th} = \pm 0.2\text{V}$, the FET saturation voltage is $V_{DS,sat} = 0.1\text{V}$.

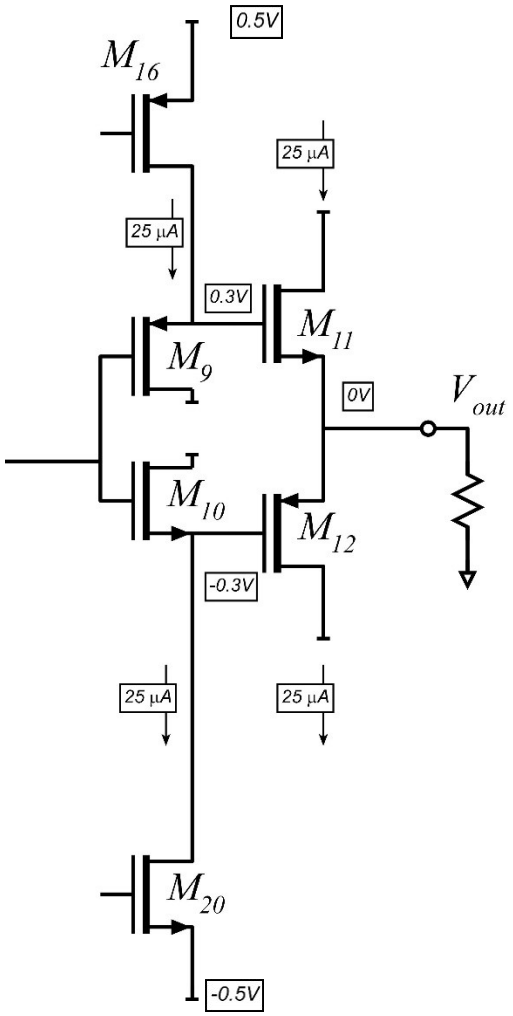
Note carefully that all FETs are biased with $V_{DS} \geq 0.1\text{V}$.

All FET widths can be calculated from

$$I_D = K_\mu (V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$$

where $K_\mu = 10\text{mA/V}^2 (W_g / 1\mu\text{m})$.

Diamond driver output stage



This is a different form of a push-pull output stage.

DC bias design is similar to a current mirror.

$V_{gs9} + V_{gs10} = V_{gs11} + V_{gs12}$.

If $I_{D16,9} = I_{D10,20}$, and if $W_{g11}/W_{g9} = W_{g12}/W_{g10}$

then $I_{D11,12} / I_{D9,10,16,20} = W_{g11}/W_{g9}$

For large output signals,

M9 and M11 carry the positive swing

while M10 and M12 carry the negative swing

Voltage gain is calculated in the usual way.

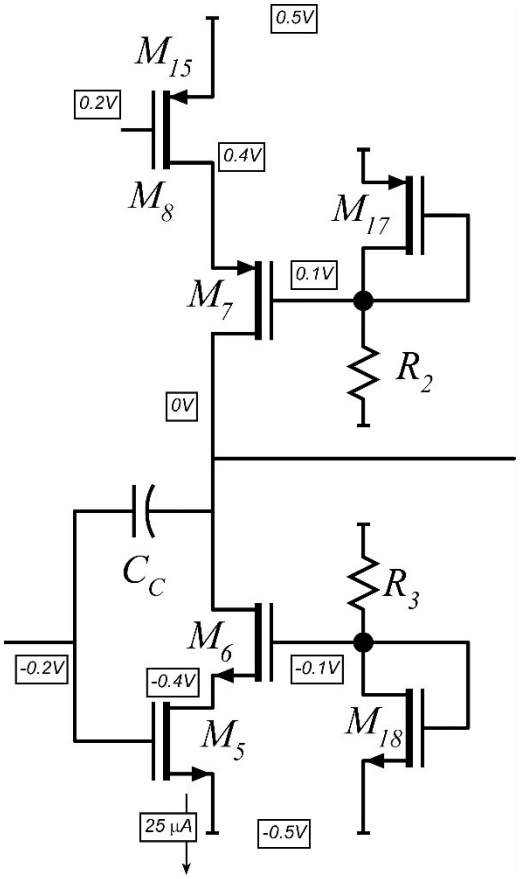
Close to 1 if $R_L >> (1/g_{m11,12})$

M16 and M20 are biased with $|V_{DS}| = 0.2\text{V}$,

while $|V_{DS,sat}| = 0.1\text{V}$, so the maximum

output is $\pm 0.1\text{V}$. Not very large.

Cascode gain stage



Using $I_D = K_\mu (V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$, pick R_2 and R_3 , and W_{g17} and W_{g18} , so that $V_{gs17} = V_{gs1} = 0.4\text{V}$.

This biases M8 and M5 with $V_{DS} = 0.1\text{V}$.

Given the bias conditions, $V_{DS,sat} = 0.1\text{V}$ for M8 and M5.

$g_m = 2I_D / (V_{gs} - V_{th}) = 2(25\mu\text{A})/(0.1\text{V}) = 0.5\text{mS}.$

$R_{DS} = 1/\lambda I_D = 4\text{V}/25\mu\text{A} = 160\text{k}\Omega$

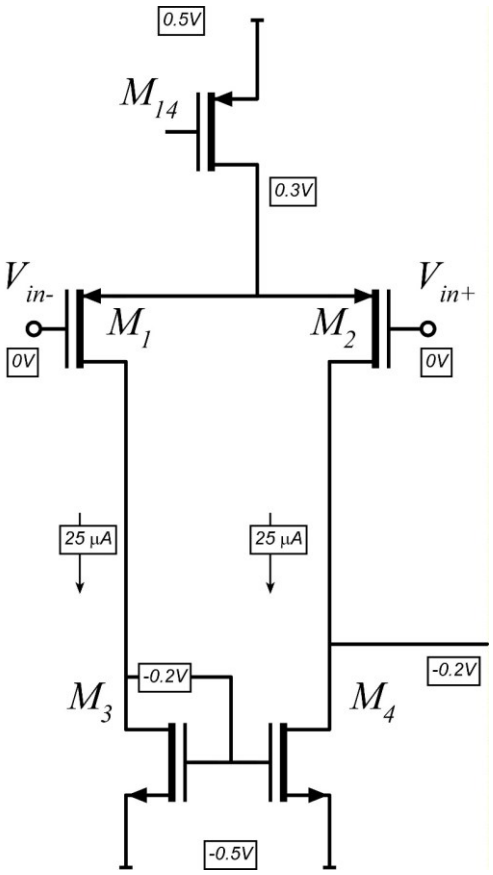
As derived earlier,

$A_{v5}A_{v6} = -(g_m R_{DS})^2 / 2 = 3,200$

For M6 and M7: $V_{DS,sat} = 0.1\text{V}$ but $V_{DS,bias} = 0.4\text{V}$.

Consequently, the maximum output is $\pm 0.3\text{V}$.

Differential Input stage



$$g_m = 2I_D / (V_{gs} - V_{th}) = 2(25\mu\text{A})/(0.1\text{V}) = 0.5\text{mS}.$$

$$R_{DS} = 1/\lambda I_D = 4\text{V}/25\mu\text{A} = 160\text{k}\Omega$$

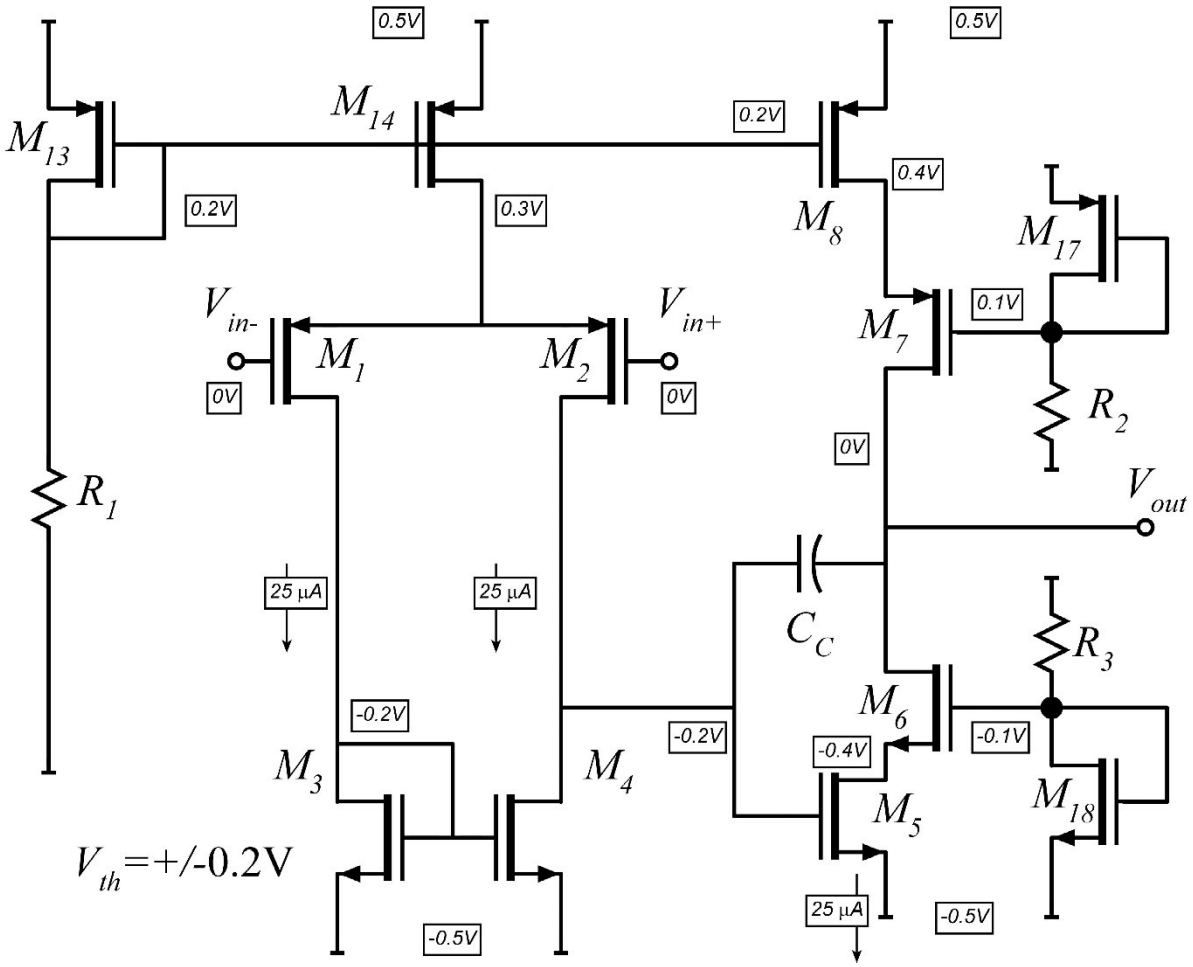
As derived earlier,

$$A_{v1,2,3,4} = (g_m R_{DS})/2 = 40$$

Overall op-amp gain:

$$A_D = A_{v1,2,3,4} A_{V5} A_{V6} A_{V9} A_{V11} \cong 40 \cdot 3200 = 128,000$$

Op-amp with no output buffer



If the load impedances are always very high, then we can remove the output buffer

The outuput can then swing ± 0.3V

More on op-amp design

Please see the documents associated with lab project 3