# ECE137A, notes set 2: MOSFETs

Mark Rodwell, Doluca Family Chair, ECE Department University of California, Santa Barbara rodwell@ece.ucsb.edu

## Goals of this note set:

Rough physical sense of FET operation

FET current-voltage characteristics.

Rough mathematical models of MOSFETs old-fashioned mobility-limited model. slightly less-old-fashioned velocity-limited model

\*We won't cover the ballistic injection velocity model

#### N-Channel MOSFET

		DRAW		
	+	CRAIN	1	
	Vdg	+	In=Is	
Gate		- Vds		
->	+	7	4	

## Field-Effect Transistor Operation



## Field-Effect Transistor Operation



#### N-Channel MOSFET

0 Gmic reg: an Plot Common - source character:stics: ID A ID 64 10/ Vos Vas= Vy Vas , Vgs Constant-current region

# Physical Sketch

F	mainma	a vox de	thickness Tox
N+		(N+)	
	P		
	49		
	-		
4 15.01.			
00 0.00			
Γ	anto	1	
I	gate		
-	gate		+
	gate		1
	gate		1
	gate		Mg
p+	gate	l.t.	Mg
p+	gate electrons	N+	Mg
N+ Source	gate	N+ DRAIN	Mg

## MOSFET Physical Structure: ~130nm node

#### **Cross-Section**



Layout



(6 FETs, each of gate width  $\rm W_g$  , connected in parallel)



# **MOSFET I-V characteristics (approximate)**

If we have drain voltages above the knee voltage :



# **MOSFET I-V characteristics (approximate)**

Then we can plot  $I_D$  vs.  $V_{GS}$ :



The \*\*3 regions \*\*\* in the  $I_D - V_{GS}$  curve : 1) Subthreshold = almost but not quite off 2) mobility-limited:  $I_D \sim (V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$ 3) velocity-limited:  $I_D \sim (V_{gs} - V_{th} - \Delta V/2)^1 (1 + \lambda V_{DS})$ 

# MOSFETs: Three Regions of Gate Voltage





When  $V_{gs}$  is a little above threshold, current is mobility – limited  $I_D \propto (V_{gs} - V_{th})^2$ 

When  $V_{gs}$  is far above threshold, current is velocity-limited  $I_D \propto (V_{gs} - V_{th} - \Delta V/2)$ 

#### **MOSFET DC Characteristics: Mobility-Limited Case**



mobility-limited current:

 $I_D \cong K_{\mu} (V_{gs} - V_{th})^2 (1 + \lambda V_{DS});$  this is only approximate for  $V_{th} < V_{gs} < V_{th} + \Delta V$  where  $K_{\mu} \cong (\mu c_{gs} W_g / 2L_g)$ where  $\Delta V \approx L_g v_{sat} / \mu$ 

Applies for drain voltages larger than the knee voltage,

#### MOSFET DC Characteristics: Velocity-Limited Case



Applies for drain voltages larger than the knee voltage,

#### DC Characteristics: \*Somewhat\* Better Approximation



Generalized Expression

$$\left(\frac{I_D}{I_{D,2}}\right)^2 + \left(\frac{I_D}{I_{D,1}}\right) = 1$$

$$I_{D,1} = K_{\mu} (V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$$
$$I_{D,2} = K_{\nu} (1 + \lambda V_{DS}) (V_{gs} - V_{th})$$

This expression is too complex for us to use in this class: Instead use \*\*as appropriate \*\* either the velocity-limited or mobility limited expressions.

# How well does our approximation work?



#### Black: actual curve Our fit: mobility region and velocity region

Observe: for very large  $(V_{gs} - V_{th})$ , a better fit would be  $I_D \approx K_v (V_{gs} - V_{th} - \Delta V)$ . This is the dotted line.

No simple expression can fit perfectly at all  $V_{gs}$ !

Our simple (red/blue) model will suffice for this class.

# Paramers and Typical #s (1)

 $v_{ini}$  = injection velocity from the source into the channel

~ $1.0 \cdot 10^7$  cm/s for N-MOSFETs

 $\mu$  = carrier mobility at surface ~ 150 – 200 cm<sup>2</sup>/(V-s) for N-MOSFET

In older technologies (~>35nm):

P-channel FETs have both  $v_{ini}$  and  $\mu$  about half that of N-FETs

In newer technologies (~<35nm):

 $v_{ini}$  and  $\mu$  are comparable for the PFET and NFET.

 $V_{th}$  threshold voltage ---usually 0.2-0.4 V for modern N-FETs

 $\lambda$  gives slope of output characteristics:  $1/\lambda$  typically 3-20 V

# Paramers and Typical #s (2)

 $c_{gs}$  = gate-channel capacitance per unit area

=  $(1/c_{ox} + 1/c_{semi})^{-1}$  two capacitances in series

 $c_{ox} = \varepsilon_r \varepsilon_0 / T_{ox}$  ( $\varepsilon_r = 3.8$  for SiO<sub>2</sub>) This is the oxide capacitance  $T_{ox} =$  equivalent oxide thickness - about 1 nm = 10<sup>-9</sup> m

 $c_{semi} \approx 0.1 \text{ F/m}^2$ 

This is the semiconductor surface capacitance, and arises because the semiconductor surface does not approximate that of a perfect conductor

 $(c_{semi} \text{ arises from two effects:}$ 

the finite # of available quantum states within the semiconductor, and the nonzero depth of the wavefunction within the semiconductor )

Stern and Howard: Properties of Semiconductor Surface Inversion Layers in the Electric Quantum Limit, Phys. Rev. 163, 816 – 15 Nov. 1967, https://journals.aps.org/pr/abstract/10.1103/PhysRev.163.816, doi = 10.1103/PhysRev.163.816

constant-current

# Knee Voltage: Mobility-Limited Case

The knee voltage defines the boundary between the Ohmic and constant - current regions

In the mobility-limited regime, the knee in curve occurs when  $V_{dg} = V_{ds} - V_{gs} = -V_{th}$ 

 $V_{GD} = V_{th} -$ 

The Knee Voltage is further increased by voltage drops across the parasitic source & drain resistances.



 $-V_{ds} = v_{inj}L_g / \mu$ 

# Knee Voltage: Velocity-Limited Case

In the velocity-limited regime, the knee in curve occurs when  $V_{ds} = v_{inj}L_g / \mu$ 

Again, the Knee Voltage is further increased by voltage drops across the parasitic source & drain resistances.



#### Which Model to use When ?



If  $V_{gs} - V_{th} < \Delta V$  where  $\Delta V \cong v_{inj}L_g / \mu$ , use the mobility-limited model If  $V_{gs} - V_{th} > \Delta V$ , use the velocity limited model

#### Linear vs. Square-Law Characteristics: 90 nm



Sorin Voinigescu, CSICS RF & High Speed CMOS, Nov. 12, 2006

#### 90 nm MOSFET DC Characteristics



#### N-channel

 $g_m / W_g = c_{gs} v_{inj} = 1.4 \text{ mS} / \mu \text{m} = 1.4 \text{ S} / \text{mm}$  $1/\lambda \sim 3V$ 

#### P-channel

$$g_m / W_g = c_{gs} v_{inj} = 0.7 \text{ mS} / \mu \text{m} = 0.7 \text{ S} / \text{mm}$$
  
 $1/\lambda \sim 3\text{V}$ 

# DC charactistics in the resistive region



$$I_{D} \cong 2K_{\mu} \left( (V_{gs} - V_{th}) \cdot V_{DS} - V_{DS}^{2} / 2 \right) (1 + \lambda V_{DS})$$

1) this is only approximate

2) this is only for \*mobility-limited\* operationUnfortunately, I don't have a derivation in the velocity limit

#### P-Channel MOSFET

P- chennel MOSFET ID To turn the deace on the gate must be more negative than the source, by an amount exceeding the threshold woltage NEL

#### P-Channel MOSFET

NID ID =0 for Vas > Ves V95 Veh  $I_{D,\mu} = K_{\mu} (V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$  $I_{D,v} = K_v (1 + \lambda V_{DS}) (V_{gs} - V_{th} - \Delta V / 2)$  $\Delta V \cong v_{sat} L_g / \mu$ 

#### P-Channel MOSFET

The device is in the constant current region it Vols above the knee walkege. Example: constant mobility model: KAES @ Vog - Vth Example: Suppose the threshold waltage is -14. Then the P-MOSFET is in the constant-current region if the drain is at most IV more positive then the gate.

# FET Small-Signal Model: Mobility-Limited

Drain Current

$$I_{D} = K_{\mu} (V_{gs} - V_{th})^{2} (1 + \lambda V_{DS})$$

Transconductance

 $\sim 1$ 

$$G_{\bullet} \xrightarrow{g_m V_{GS} R_{DS}} \bullet D$$

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} = 2K_\mu (V_{gs} - V_{th})(1 + \lambda V_{DS}) \approx 2K_\mu (V_{gs} - V_{th})$$

**Output Conductance** 

$$G_{ds} = \frac{1}{R_{ds}} \equiv \frac{\partial I_D}{\partial V_{DS}} = \frac{\lambda I_D}{1 + \lambda V_{DS}}$$
  

$$\cong \lambda I_D \text{ to within the accuracy of the models we are using}$$

Note that  $R_{ds}$  varies roughly as  $1/I_D$ .

### FET transconductance: Mobility-Limited

Drain Current

$$I_{D} = K_{\mu} (V_{gs} - V_{th})^{2} (1 + \lambda V_{DS})$$

Transconductance

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} = 2K_{\mu}(V_{gs} - V_{th})(1 + \lambda V_{DS})$$

$$\frac{g_m}{I_D} = \frac{2K_{\mu}(V_{gs} - V_{th})(1 + \lambda V_{DS})}{K_{\mu}(V_{gs} - V_{th})^2(1 + \lambda V_{DS})} = \frac{2}{(V_{gs} - V_{th})}$$

 $\rightarrow g_m = 2I_D / (V_{gs} - V_{th}) \text{, but only in mobility-limited case}$ \*\* and only if  $(V_{gs} - V_{th}) > 2V_T = 2kT / q **$ 

If  $(V_{gs} - V_{th}) \le 2V_T = 2kT / q$ , then the fet is in subthreshold mode and  $g_m \cong I_D / nV_T$ , where  $n \ge 1$  is some parameter characteristic of the device



## FET Small-Signal Model: Velocity-Limited

Drain Current  $I_D = K_v (1 + \lambda V_{DS})(V_{gs} - V_{th} - \Delta V / 2)$ 



Transconductance

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} = K_v (1 + \lambda V_{DS}) \approx K_v$$

**Output Conductance** 

$$G_{ds} = \frac{1}{R_{ds}} \equiv \frac{\partial I_D}{\partial V_{DS}} = \frac{\lambda I_D}{1 + \lambda V_{DS}}$$
$$\cong \lambda I_D$$

#### Transconductance vs Vgs

#### mobility-limited

$$I_{D,\mu} = K_{\mu} (V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$$
  

$$\rightarrow g_m = \frac{\partial I_D}{\partial V_{GS}} = 2K_{\mu} (V_{gs} - V_{th}) (1 + \lambda V_{DS})$$



### Example #1: NMOS @ 15nm gate length



Then:

$$K_{\mu} = \mu c_{gs} W_g / 2L_g = 16 \text{mA/V}^2 \cdot (W_g / 1\mu\text{m})$$
  

$$K_{\nu} = c_{gs} v_{inj} W_g = 2.40 \text{mA/V} \cdot (W_g / 1\mu\text{m})$$
  

$$\Delta V = v_{inj} L_g / \mu = 75 \text{mV}: \text{ Note how small is the mobility-limited region}$$

## Example #2: 250 nm NMOS:



Then:

$$K_{\mu} = \mu c_{gs} W_g / 2L_g = 0.55 \text{mA/V}^2 \cdot (W_g / 1\mu\text{m})$$
  

$$K_v = c_{gs} v_{inj} W_g = 0.69 \text{mA/V} \cdot (W_g / 1\mu\text{m})$$
  

$$\Delta V = v_{inj} L_g / \mu = 0.625 \text{V} \text{ Note how *large* is the mobility-limited region}$$

# Example #3: for easy hand calculations

For easy hand calculations with examples in the notes, we will often use:

$$K_{\mu} = 10 \text{mA/V}^2 \cdot (W_g / 1\mu\text{m})$$
$$K_v = 2 \text{mA/V} \cdot (W_g / 1\mu\text{m})$$
$$\Delta V = 0.1 \text{V}$$
$$V_{th} = 0.3 \text{V}$$



I suppose this might be roughly the characteristics of a MOSFET with ~30nm physical gate length.

# Caution regarding examples 1,2 and 3

To keep analysis simple, we have ignored the effect of  $R_s$  and  $R_D$ .

We therefore considerably over-estimated the MOSFET drain current at a given  $V_{gs}$ .

In the interest of simplicity, we will accept this limitation in this class.

A proper analysis would need to include the effect of  $R_s$  and  $R_D$ , by treating  $R_s$  and  $R_D$  as separate external resistances, or by adjusting the FET model parmeters to fit the overall DC charateristics.

# MOSFET model: comments

1) MOS models in most undergraduate texts ignore injection velocity limits, yet this is a huge effect in modern MOSFETs.

2) Given (1), there is no consensus on how to teach velocity limited operatoin in undergraduate classes.

3) The 137ab method, here, is my attempt at a reasonably accurate yet simple model.

4) The more accurate expression given here is derived by assuming

an exit velocity  $v_{ini}$  at the drain end of the channel.

5) Even the more accurate expression is only very approximate for highly scaled MOSFETs: for detailed design, we use foundry CAD models.

6) See publications by M. Lundstrom and D. Antoniadis for good derivations of modern FET I-V characteristics.