ECE137A, Notes Set 9: Multi-stage examples: active loads, current mirrors, Darlingtons, cascodes, push-pull stages

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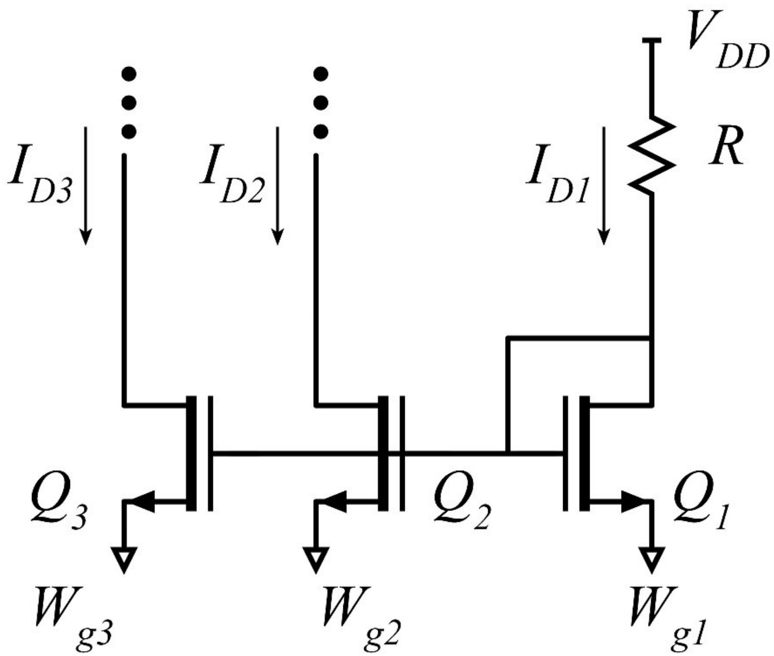
MOSFET Current Mirrors

Suppose we want to provide desired, fixed bias currents to several circuits:



Required: $V_{DS} > V_{knee}$ to operate correctly

Either

$$I_D \cong K_\mu (V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$$

Or:

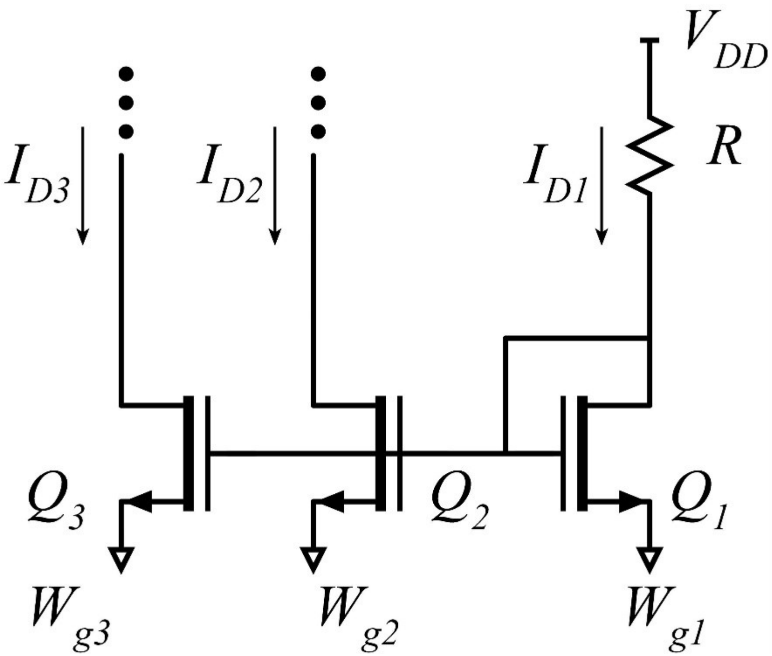
$$I_D \cong K_v (1 + \lambda V_{DS})(V_{gs} - V_{th} - \Delta V / 2)$$

In either case:

$$\frac{I_{D2}}{I_{D1}} = \frac{W_{g2}}{W_{g1}} \cdot \frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})}$$; similar expression for $\frac{I_{D3}}{I_{D1}}$

We would like to have $I_{D2}/I_{D1} = W_{g2}/W_{g1}$

MOSFET Current Mirrors

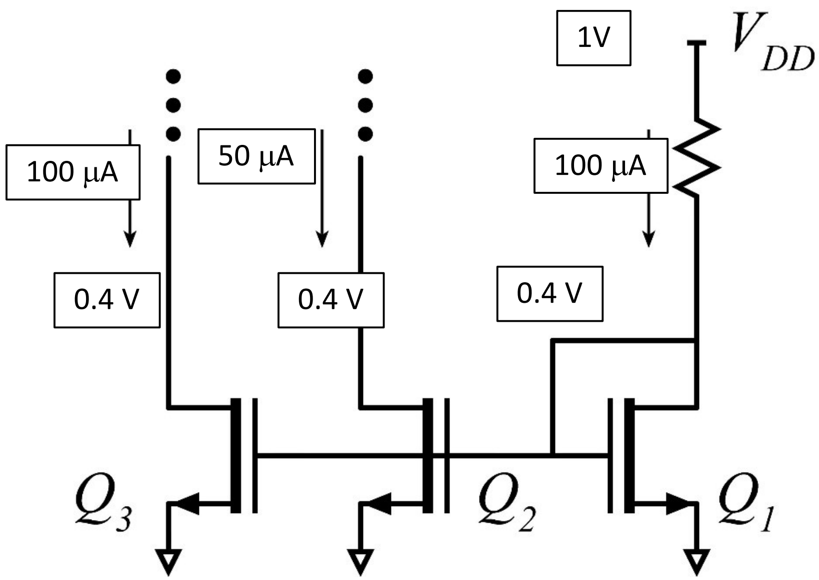


$$\frac{I_{D2}}{I_{D1}} = \frac{W_{g2}}{W_{g1}} \cdot \frac{(1+\lambda V_{DS2})}{(1+\lambda V_{DS1})}$$

If we ignore the $(1+\lambda V_{DS})$ terms, then
$I_{D2} / I_{D1} = W_{g2} / W_{g1}$;
We pick FET widths to set DC currents

The $(1+\lambda V_{DS})$ terms then represent
a loss in precision in setting
the desired currents

MOSFET Current Mirror Example



$K_\mu = 10\text{mA/V}^2 \cdot (W_g / 1\mu\text{m})$

$K_v = 2\text{mA/V} \cdot (W_g / 1\mu\text{m})$

$\Delta V = 0.1\text{V}$

$V_{th} = 0.3\text{V}$

$1/\lambda = 4\text{V}$

Let us design the circuit to give the indicated currents

Q_1 carries 0.1mA at $V_{gs} = V_{DS} = 0.4\text{V}$

$(V_{gs} - V_{th}) = 0.1\text{V} = \Delta\text{V} \rightarrow$ boundary of velocity- and mobility-limited regions.

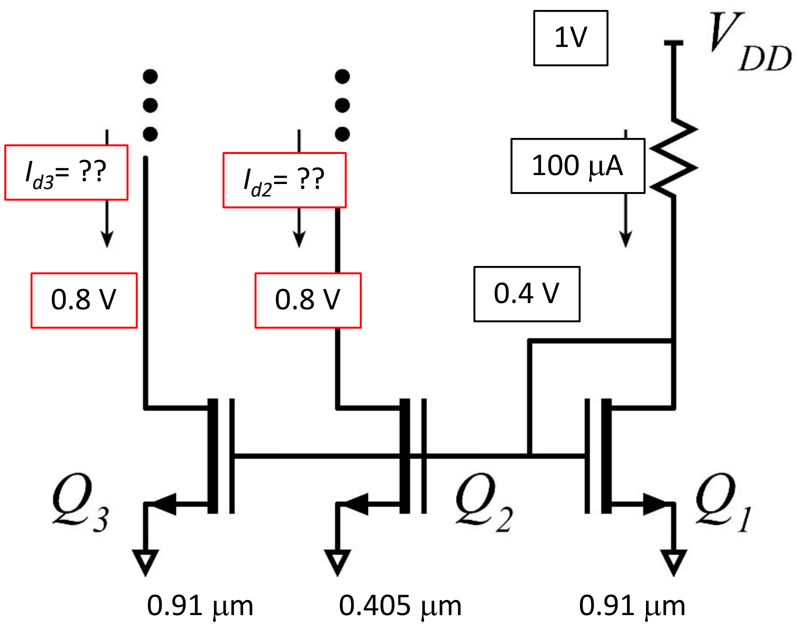
$$I_{D1} = K_\mu (V_{gs} - V_{th})^2 (1 + \lambda V_{DS1})$$

$$0.1\text{mA} = 10\text{mA/V}^2 (W_g / 1\mu\text{m})(0.1\text{V})^2 (1 + 0.4\text{V}/4\text{V}) \rightarrow W_g = 0.91\mu\text{m}$$

Q_2 and Q_3 carry 50μA and 100μA at $V_{gs} = V_{DS} = 0.4\text{V}$

$\rightarrow$ Similar calculations $\rightarrow W_{g2} = 0.45\mu\text{m}$, $W_{g3} = 0.91\mu\text{m}$

MOSFET Current Mirror Example



Now suppose V_{DS2} and V_{DS3} are increased

How much do I_{D2} and I_{D3} change ?

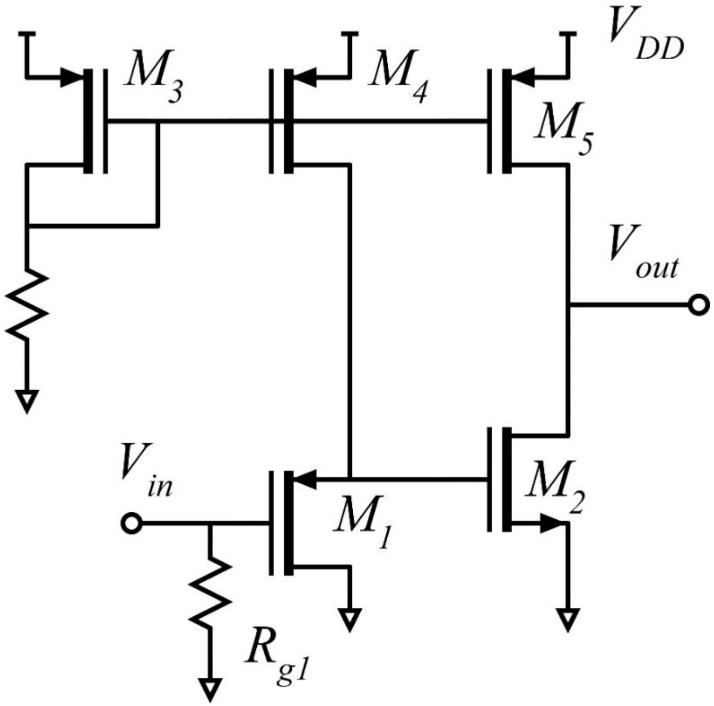
$$\frac{I_{D2}}{I_{D1}} = \frac{W_{g2}}{W_{g1}} \cdot \frac{(1+\lambda V_{DS2})}{(1+\lambda V_{DS1})} = \frac{1}{2} \cdot \frac{(1+0.8\text{V}/4\text{V})}{(1+0.4\text{V}/4\text{V})} = \frac{1}{2} \cdot \frac{11}{10}$$

$I_{D2} = 55\mu\text{A}.$

Similar calculation $\rightarrow I_{D3} = 110\mu\text{A}$

Variation in output currents due to $(1+\lambda V_{DS})$ terms.

MOS multi-stage amplifier example



FET parameters

$$K_\mu = 10\text{mA/V}^2 \cdot (W_g / 1\mu\text{m})$$

$$K_v = 2\text{mA/V} \cdot (W_g / 1\mu\text{m})$$

$$\Delta V = 0.1\text{V}$$

$$V_{th} = 0.3\text{V}$$

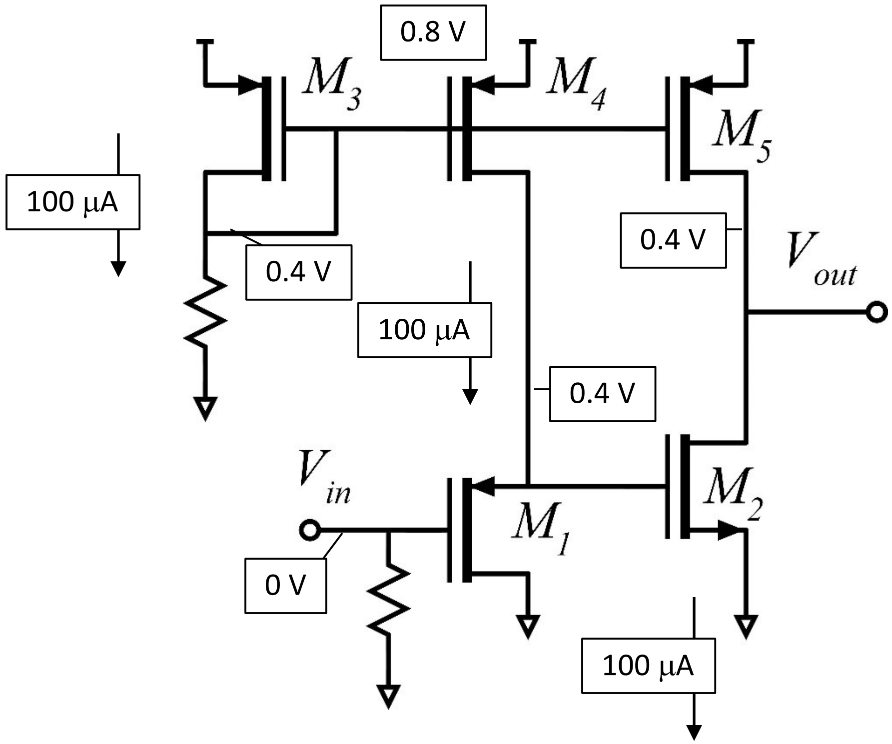
$$1/\lambda = 4\text{V}$$

Simple two-stage amplifier:

Low-voltage operation

DC-coupled input, at zero volts, even with only a positive supply voltage.

MOS multi-stage amplifier example



Let us design the circuit to give the indicated currents at the indicated node and supply voltages.

Each FET carries 0.1mA at $|V_{GS}|=|V_{DS}|=0.4\text{V}$

$|V_{GS}|=0.4\text{V} \rightarrow$ boundary of velocity- and mobility-limited regions.

$I_{D1} = K_\mu (V_{gs} - V_{th})^2 (1+\lambda V_{DS1}) \rightarrow W_g = 0.91\mu\text{m}$ for all FETs

Multi-stage amplifier: small-signal analysis

FET small-signal parameters:

mobility-limited $\rightarrow$ $g_m = 2I_D/(V_{gs} - V_{th}) = 2\text{mS}$

$R_{DS} = 1/\lambda I_D = 4\text{V}/0.1\text{mA}{=}40\text{k}\Omega$

M_2: common-source

$R_{Leq2} = R_{DS2} \,||\, R_{DS5} = 40\text{k}\Omega \,||\, 40\text{k}\Omega = 20\text{k}\Omega$

$A_{v2} = -g_{m2}R_{Leq2} = 2\text{mS} \cdot 20\text{k}\Omega = -40$

$R_{in2} {=} \infty\ \Omega$

M_1: common-drain, a.k.a. source follower

$R_{Leq1} = R_{DS1} \,||\, R_{DS4} \,||\, R_{in2} = 40\text{k}\Omega \,||\, 40\text{k}\Omega \,||\, \infty\Omega = 20\text{k}\Omega$

$$A_{v2} = \frac{R_{Leq1}}{R_{Leq1} + 1/g_{m1}} = \frac{20\text{k}\Omega}{20\text{k}\Omega + 500\Omega} = \frac{40}{41} = 0.976$$

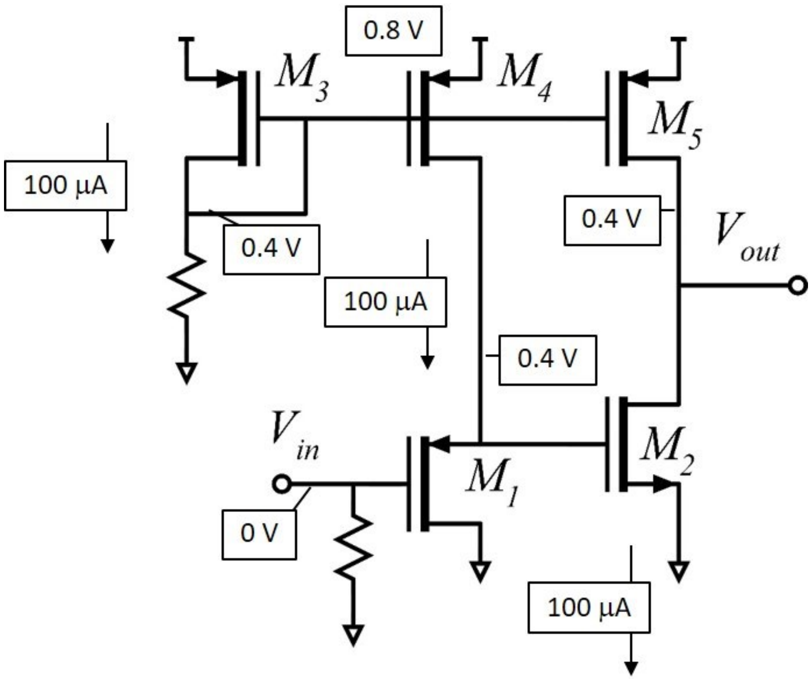
$R_{in1} {=} \infty\ \Omega$

Overall: $A_v = A_{v1}A_{v2} = 0.976(-40) = -39$

Multi-stage amplifier: maximum signal swings

Transistors are operating at mobility/velocity boundary.

OK to use either model. Mobility model: $V_{DS,knee} = V_{gs} - V_{th}$



M_2 bias voltage: $V_{DSQ} = 0.4\text{V}.$

M_2 knee voltage:

$V_{DSKnee} = V_{gs} - V_{th} = 0.4\text{V} - 0.3\text{V} = 0.1\text{V}$

$\Delta V_{D2\max} \downarrow = 0.4\text{V} - 0.1\text{V} = 0.3\text{V}$

0.3V maximum negative swing

M_2 bias current: $I_{DQ} = 100\mu\text{A}.$

M_2 minimum current: $I_{D\min} = 0\mu\text{A}.$

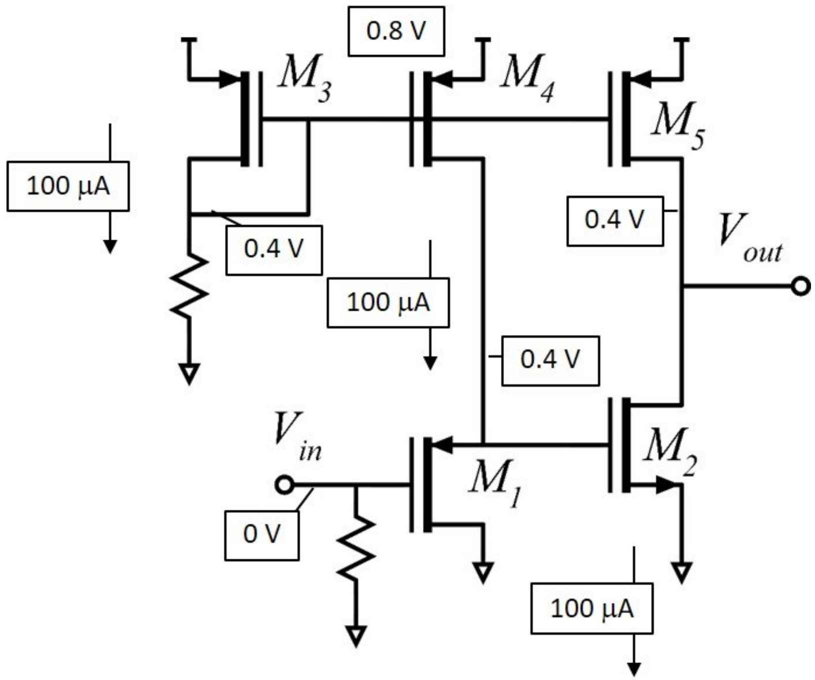
$\Delta I_{D,\max} \downarrow = 100\mu\text{A}$ (decrease)

$R_{Leq2} = 20\text{k}\Omega$

$\Delta V_{D,\max} \uparrow = 100\mu\text{A} \cdot 20\text{k}\Omega = 2\text{V}$

2V maximum positive swing

Multi-stage amplifier: maximum signal swings



M_5 bias voltage: $V_{DSQ} = 0.4\text{V}.$

M_5 knee voltage:

$$V_{DSKnee} = V_{gs} - V_{th} = 0.4\text{V} - 0.3\text{V} = 0.1\text{V}$$

$$\Delta V_{D5\max} \uparrow = 0.4\text{V} - 0.1\text{V} = 0.3\text{V}$$

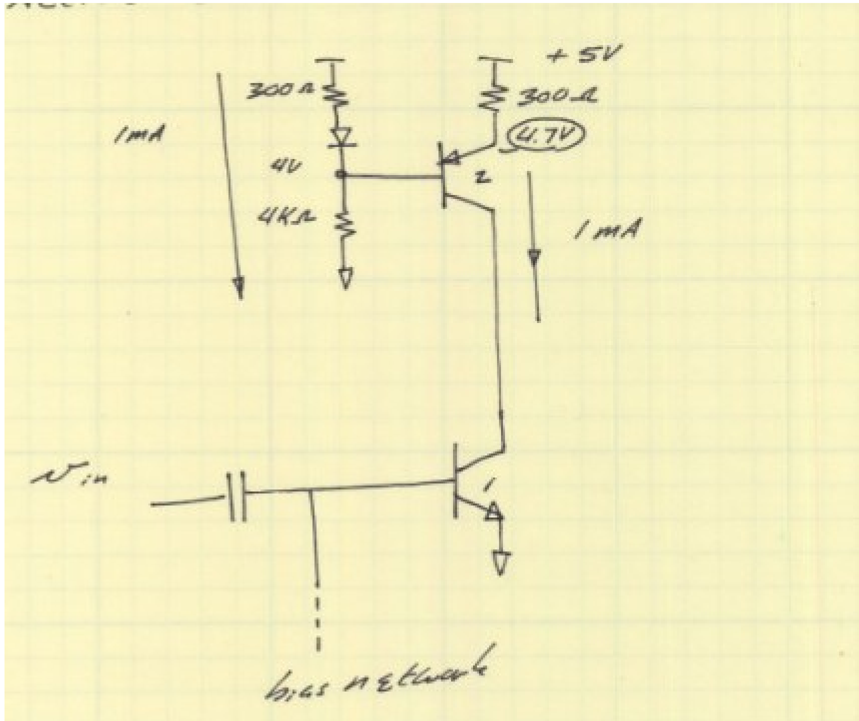
0.3V maximum positive swing

No cutoff calculation for M_5;
it is a constant-current source

We can (and should) do similar calculations for cutoff and knee voltage of M_1, and knee voltage of M_4 to find the maximum voltage swing at the drain of M_1. The resulting answers must then be multiplied by the voltage gain of M_5 to find the associated maximum output voltage swing.

Finding: M_2, M_5 limits dominate: $+/-0.3$ V maximum linear output swing.

Active loads: constant current sources



note that the bias network is not shown

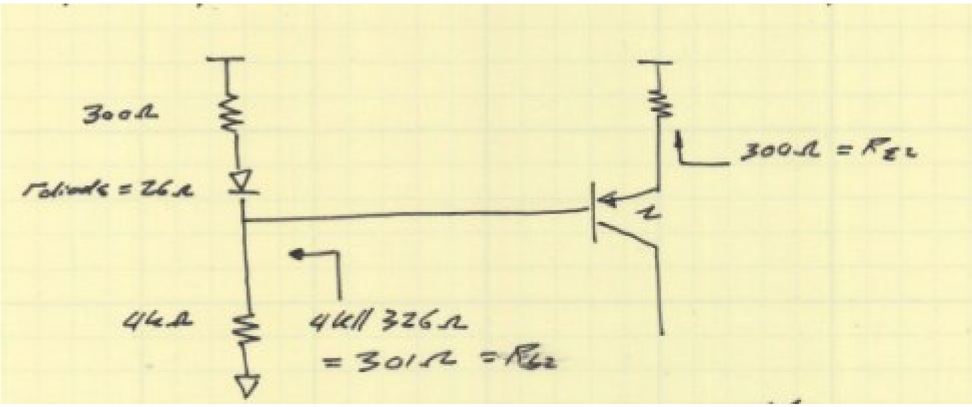
stages with c.c. loads usually have high gains

and often can only be properly biased as part

of a feedback amplifier

Active loads: constant current sources

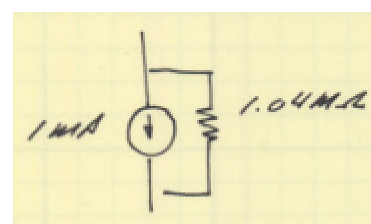
output impedance of Q2: $V_A = 100V$, $\beta = 100$



$$R_{out2} = \underbrace{r_{ce2}}_{100k}\left[1 + \frac{\overbrace{R_{E2}}^{300\Omega}}{r_{E2}} \frac{\beta \overbrace{r_{E2}}^{26\Omega}}{\beta r_{E2} + \underbrace{R_{B2}}_{301\Omega} + R_{E2}}\right]$$

$$= \underbrace{1.04\,M\Omega}_{\text{very large, much larger than } R_{ce}.}$$

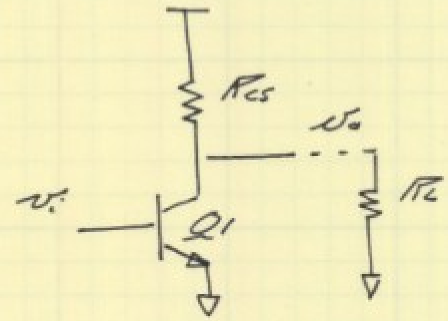
$\Rightarrow$ Norton Model of constant-current source:



Active loads: constant current sources

gain of the amplifier:

$$v_o/v_i = -\frac{R_L \| R_{cs} \| r_{ce1}}{r_{E1}}$$



Because R_{cs} is very large, 10:1 larger than r_{ce1} in this example, it has little effect upon the gain.

In contrast, had a biasing resistor been used, its value would have been a few kΩ in order to supply 1mA → less gain

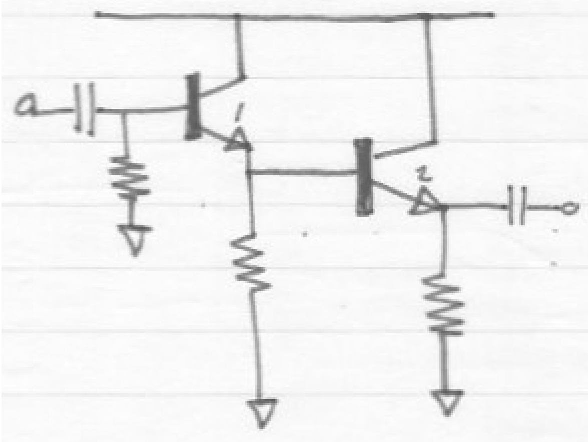
If R_L and R_{cs} are both >> r_{ce}, then:

$$\frac{v_o}{v_i} \cong -\frac{r_{ce}}{r_{E1}} = -\frac{V_A/I_C}{V_T/I_C} = \frac{-V_A}{V_T} \cong -4000$$ in this case

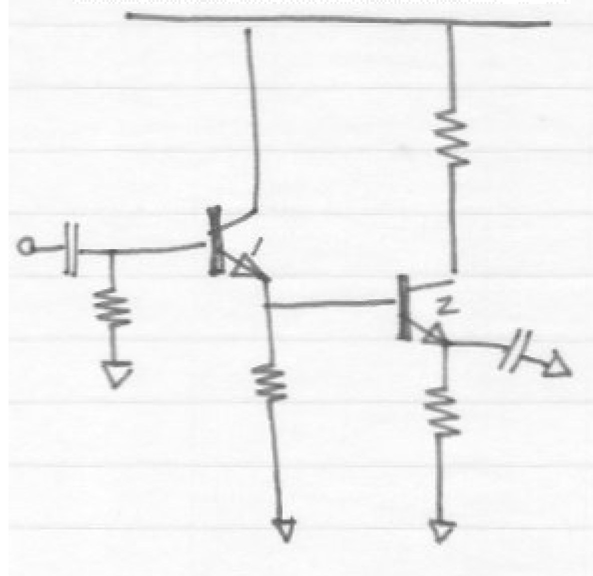
Constant-current loads allow
large stage voltage gains.

Darlington Pairs

2 cascaded emitter followers.

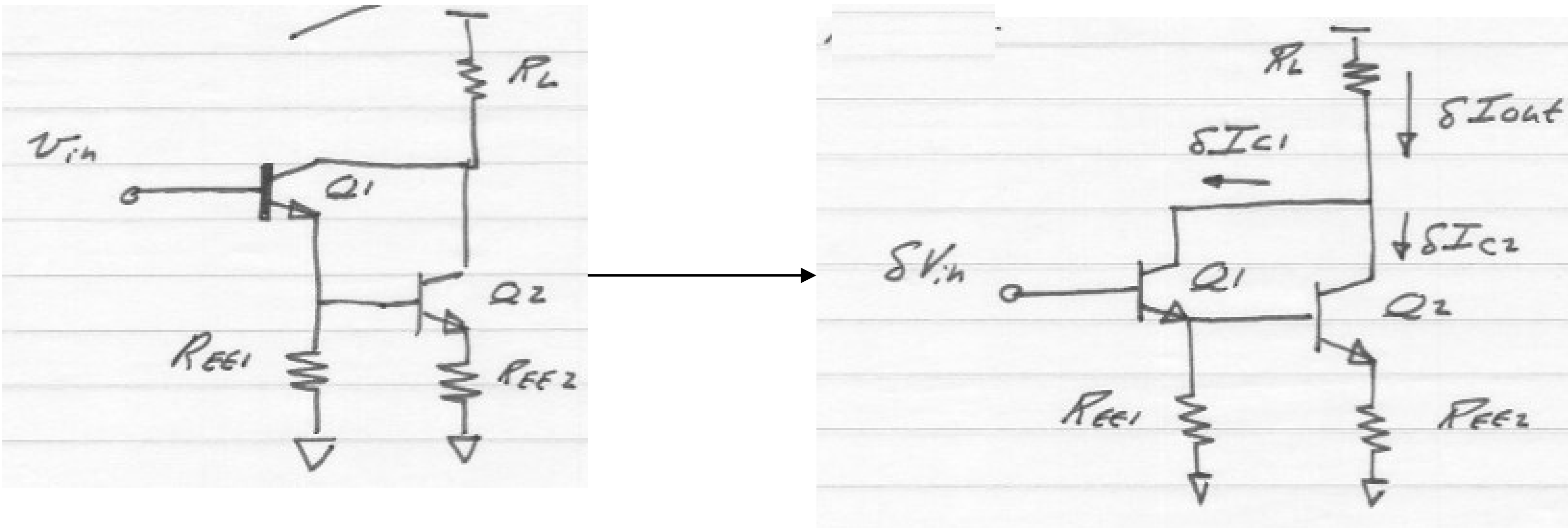


emitter follower driving a common-emitter stage



In both cases Q1 is used to further increase the input impedance.

Darlington Pairs: Alternate and Common Form



simplify analysis : set $R_{CE}=\infty$
$\beta=\infty$

Darlington Pairs: Alternate and Common Form

apply δV_{e1}

then $\delta V_{E1} = \delta V_{in1} \cdot \dfrac{R_{EE1}}{R_{EE1} \cdot r_{e1}} = \delta V_{in1} \cdot A_{v1}$

$$\downarrow$$

$$\delta I_{c1} = \frac{\delta V_{E1}}{R_{EE1}} = \frac{\delta V_{in}}{r_{e1} + R_{EE1}}$$

$$\delta I_{c2} = \frac{\delta V_{E1}}{R_{EE2} + r_{e2}} = \delta V_{in} \cdot \frac{A_{v1}}{R_{EE2} + r_{e2}}$$

$$\delta I_{out} = \delta I_{c1} + \delta I_{c2}$$

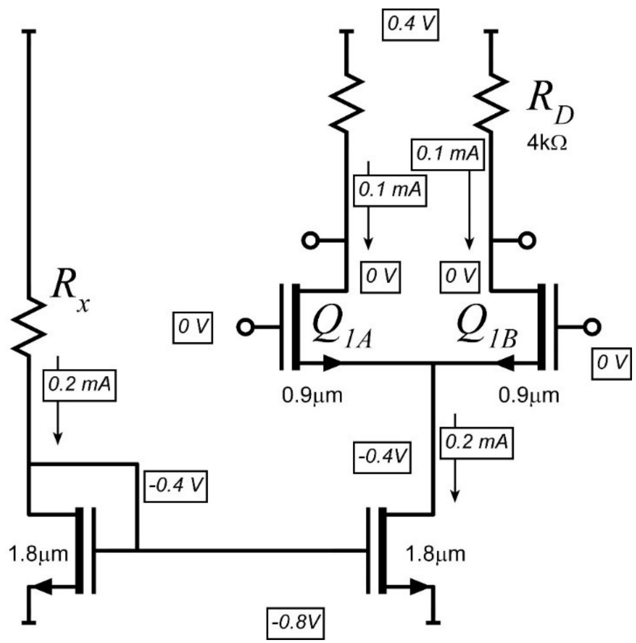
$$\delta V_{out} = -\delta I_{out} \cdot R_L$$

$$\boxed{\frac{\delta V_{out}}{\delta V_{in}} = A_v = -A_{v1} \cdot \frac{R_L}{r_{e2} + R_{EE2}} - \frac{R_L}{R_{EE1} + r_{e1}}}$$

Answer is a bit more complex for finite β, finite R_{CE}.

Differential common-source stage

Starting point for comparison... (note the odd, asymmetric power supplies)



FETs:

$K_\mu = 10\text{mA/V}^2 (W_g / 1\mu\text{m})$

$K_v = 2\text{mA/V} (W_g / 1\mu\text{m})$

$\Delta V = 0.1\text{V}$

$V_{th} = \pm 0.3\text{V}$

$1/\lambda = 4\text{V}$

DC bias design: setting $V_{gs} = 0.4\text{V}$ for all FETs

$\rightarrow$ boundary of velocity- and mobility-limited regions.

For Q_{1A}: $I_D = K_\mu (V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$

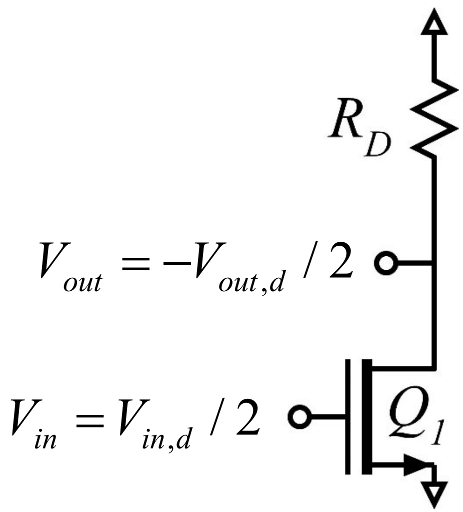
$0.1\text{mA} = 10\text{mA/V}^2 (W_g / 1\mu\text{m})(0.1\text{V})^2 (1 + 0.4\text{V}/4\text{V})$

$\rightarrow W_g = 0.91\mu\text{m}$

Similar calculation for all other FET widths

Differential gain

Small-signal analysis: differential mode



$$R_{DS1} = 1/\lambda I_D = 4\text{V}/0.1\text{mA}{=}40\text{k}\Omega$$

Mobility-limited FET:

$$I_D = K_\mu (V_{gs} - V_{th})^2 (1+\lambda V_{DS})$$

$$g_m = 2K_\mu (V_{gs} - V_{th})(1+\lambda V_{DS})$$

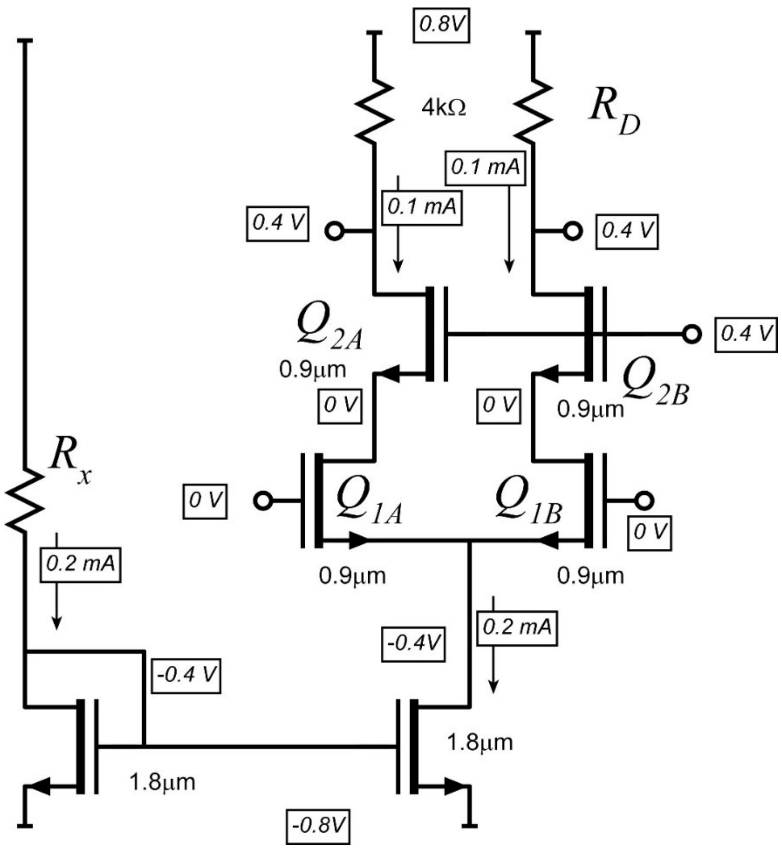
$$g_m = 2I_D (V_{gs} - V_{th}) \text{ only in mobility-limited case}$$

$$g_m = 2(0.1\text{mA})/0.1\text{V}{=}2\text{mS}.$$

$$R_{Leq1} = R_{DS1} \,||\, R_D = 40\text{k}\Omega || 4\text{k}\Omega = 3.66\text{k}\Omega$$

$$V_{od}/V_{id} = g_{m1} R_{Leq1} = 2\text{mS}(3.66\text{k}\Omega) = 7.27$$

Differential Pair with Cascode



Transistors Q_{2A} and Q_{2B} have been added.

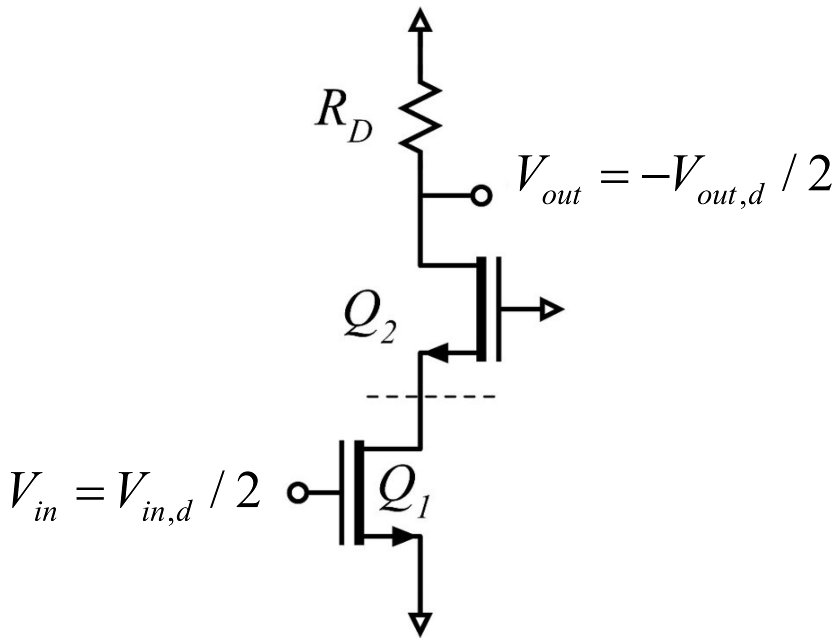
We've increased the positive supply to 0.8V, and we've picked DC levels to keep $V_{DS}=V_{gs}=0.4\text{V}$ for all transistors.

So: given that $I_D=K_\mu(V_{gs}-V_{th})^2(1+\lambda V_{DS})$, we have the same FET widths as before

The load resistance is also unchanged

Differential Pair with Cascode

Small-signal analysis: differential mode



Q_2 : common-gate

$$R_{Leq2} = R_D = 4\text{k}\Omega$$

$$R_{in2} = (1/g_{m2})(1 + R_{Leq2}/R_{DS2})$$

$$= 500\Omega(1 + 4\text{k}\Omega / 40\text{k}\Omega) = 550\Omega$$

$$A_{v2} = R_{Leq2} / R_{in2} = 4\text{k}\Omega / 550\Omega = 7.27$$

Q_1 : common-source

$$R_{Leq1} = R_{in2} \,\|\, R_{DS1} = 550\Omega \,\|\, 40\text{k}\Omega = 542\Omega$$

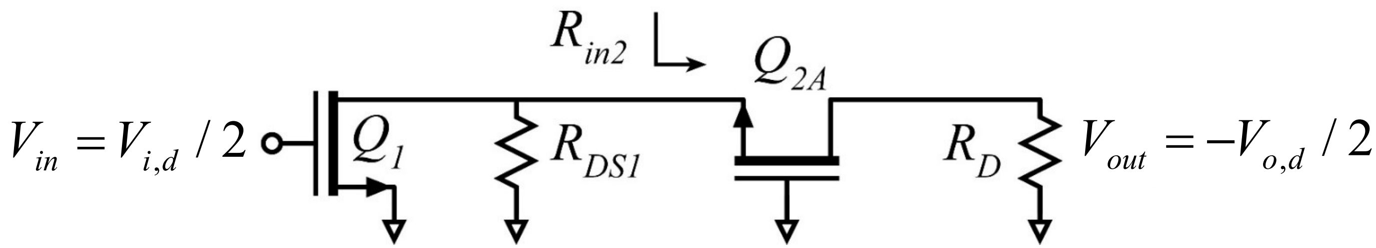
$$A_{v1} = -g_{m1} R_{Leq1} = -2\text{mS} \cdot 542\Omega = -1.09$$

Total gain: common-source

$$V_{out} / V_{in} = A_{v,total} = A_{v1} A_{v2} = -1.09 \cdot 7.27 = -7.89$$

but $V_{out} = -V_{out,d} / 2$ and $V_{in} = V_{in,d} / 2$ so $V_{out,d} / V_{in,d} = 7.89$

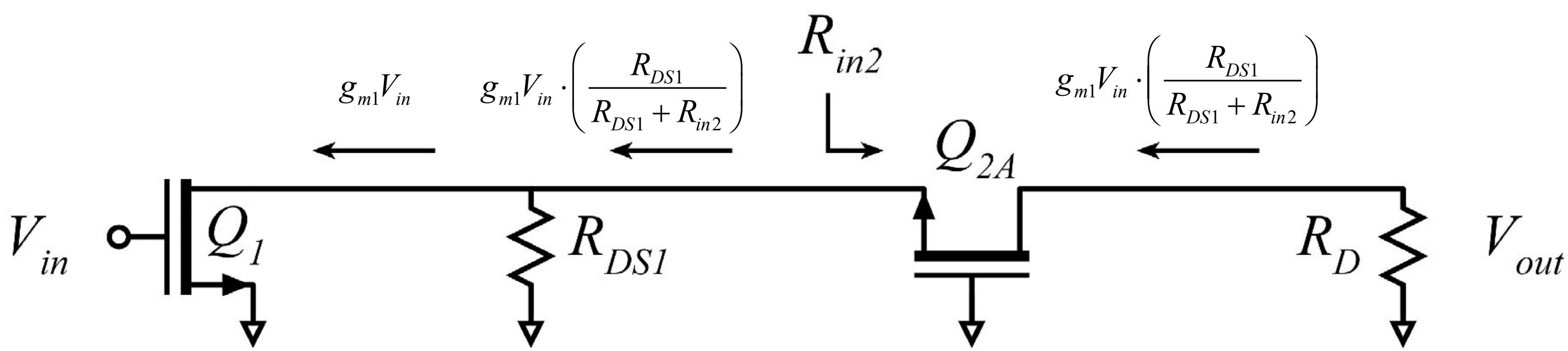
Another way of calculating the gain



$$V_{out}/V_{in} = A_{v1}A_{v2} = -g_{m1}R_{Leq1}\left(\frac{R_{Leq2}}{R_{in2}}\right) = -g_{m1}\left(\frac{R_{DS1}R_{in2}}{R_{DS1}+R_{in2}}\right)\left(\frac{R_{Leq2}}{R_{in2}}\right)$$

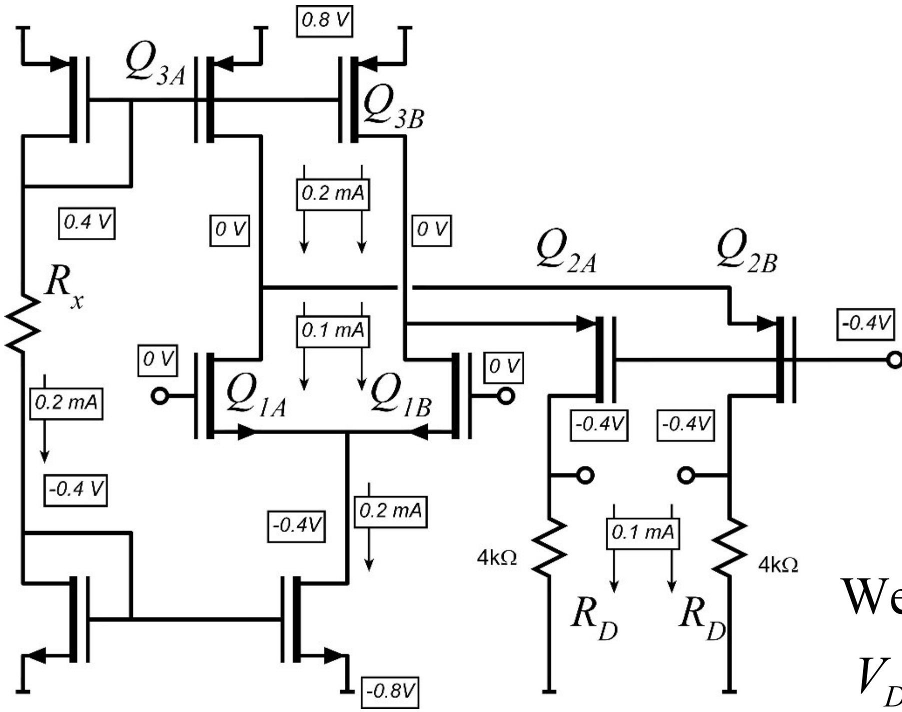
$$= -g_{m1}\left(\frac{R_{DS1}}{R_{DS1}+R_{in2}}\right)R_{Leq2}$$

Consider the currents



The output current of Q_1 is current-divided between R_{DS1} and R_{in2}, and then passes through Q_2 to the load

Differential Pair with *Folded* Cascode



Instead we add PFETs Q_{2A} and Q_{2B}.

We've biased these at 0.1mA each.

Also added: current sources Q_{2A} and Q_{2B}.

Clearly, these must carry 0.2mA each.

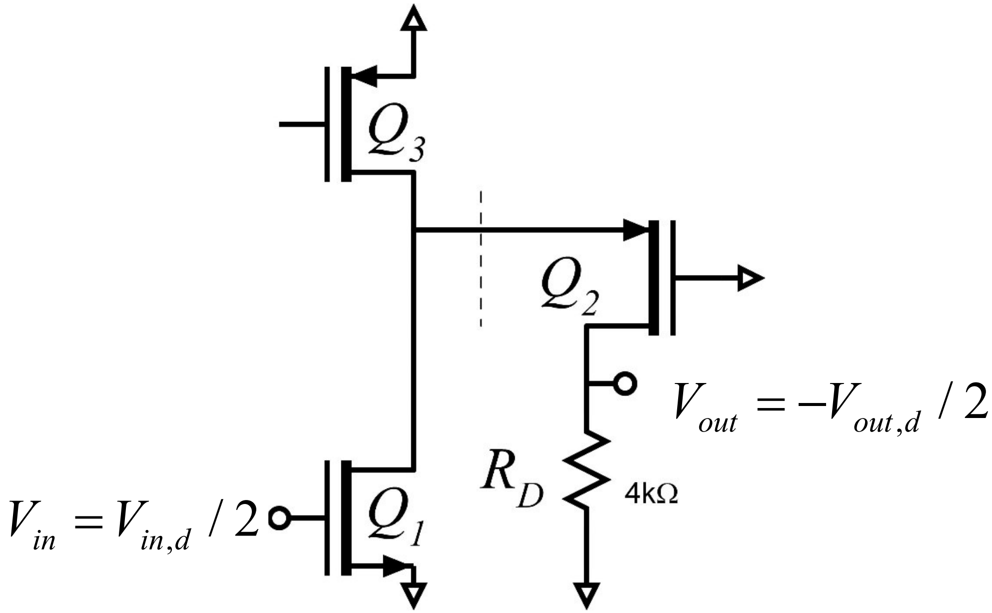
The load resistance is unchanged

We've picked DC levels to keep $V_{DS} = V_{gs} = 0.4\text{V}$ for all transistors.

So: given that $I_D = K_\mu (V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$, we have the same FET widths as before

Folded Cascode: Differential Half-Circuit

Small-signal analysis: differential mode



Q_2 : common-gate

$$R_{Leq2} = R_D$$

$$R_{in2} = (1/g_{m2})(1 + R_{Leq2}/R_{DS2})$$

$$A_{v2} = R_{Leq2}/R_{in2}$$

Q_1 : common-source

$$R_{Leq1} = R_{in2} \,||\, R_{DS1} \,||\, R_{DS3}$$

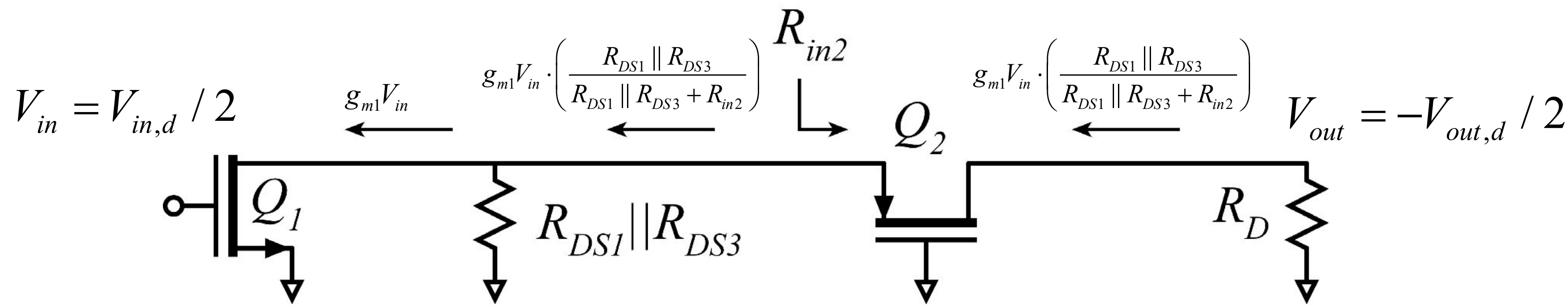
$$A_{v1} = -g_{m1}R_{Leq1}$$

Total gain: common-source

$$V_{out}/V_{in} = A_{v,total} = A_{v1}A_{v2}$$

but $V_{out} = -V_{out,d}/2$ and $V_{in} = V_{in,d}/2$ so $V_{out,d}/V_{in,d} = -A_{v1}A_{v2}$

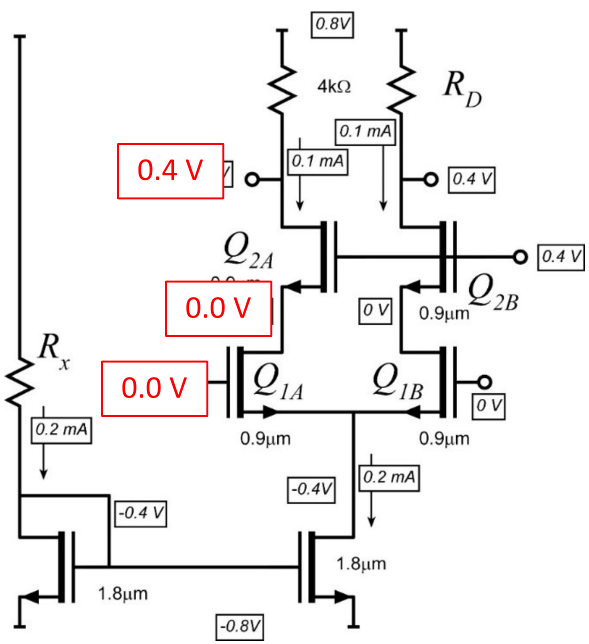
Folded Cascode: tracking the currents

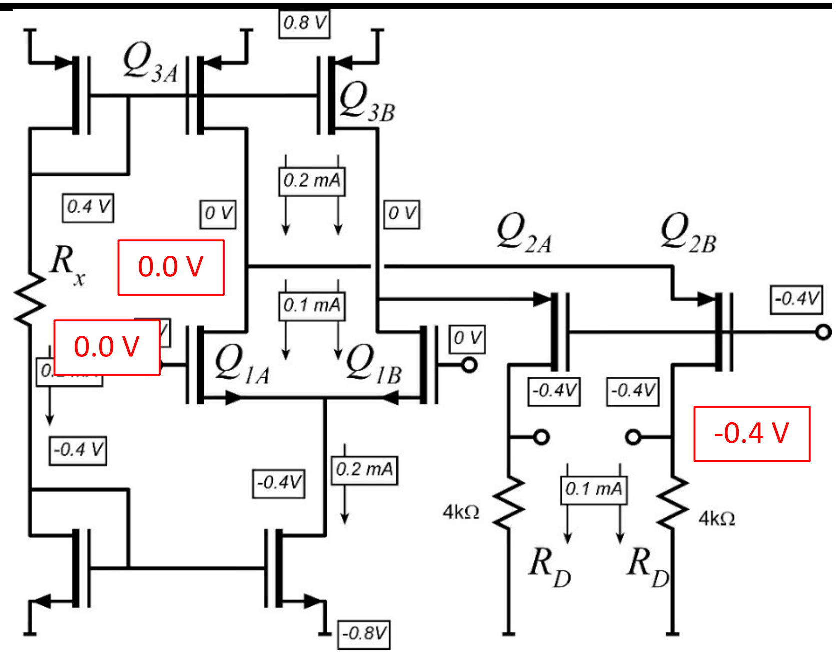


$$V_{out}/V_{in} = A_{v1}A_{v2} = -g_{m1}\left(\frac{R_{DS1}\|R_{DS3}}{R_{DS1}\|R_{DS3}+R_{in2}}\right)R_{Leq2}$$

The output current of Q_1 is current-divided between $R_{DS1}\|R_{DS3}$ and R_{in2}, and then passes through Q_2 to the load

Why use *folded* cascode?

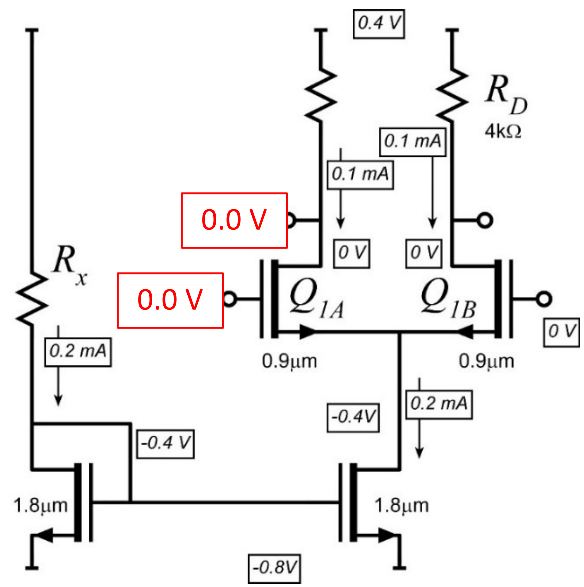




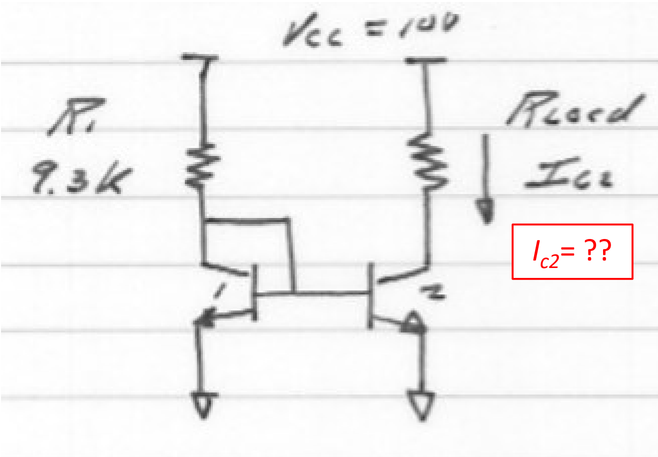
In DC-coupled circuits, the DC ouput voltage of one stage is the DC input voltage of the next.

The PFET common-gate stages have shifted the DC levels to more negative voltages.

This can be useful in DC bias design.



Bipolar current mirror



Assume β, V_A are infinite

We have $I_C = I_S \exp(V_{be}/V_T) \rightleftarrows \qquad {}_T \ln(I_C/I_S)$

where $V_T = kT/q = 26\text{mV} \;@T{=}300\text{K}$

$I_S = J_S A_E$

A_E = emitter junction area

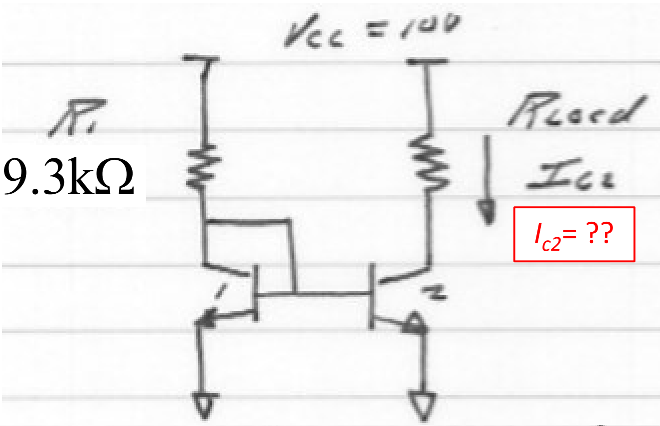
J_S = emitter saturation current density (A/cm^2).

Key points:

1) We will no longer blindly assume that $V_{be} \cong 0.7\text{V}$. Instead, $V_{be} = V_T \ln(I_C/I_S)$.

2) I_S is proportional to the emitter junction area.

Bipolar current mirror



$$I_{c1} \cong (V_{cc} - V_{be,on})/R_1 = 1 \text{ mA} \quad \to R_1 = 9.3\text{k}\Omega$$

Note that $V_{be1} = V_{be2}$

but $I_{c1} = I_{s1}\left(e^{V_{be1}/V_T} - 1\right)$

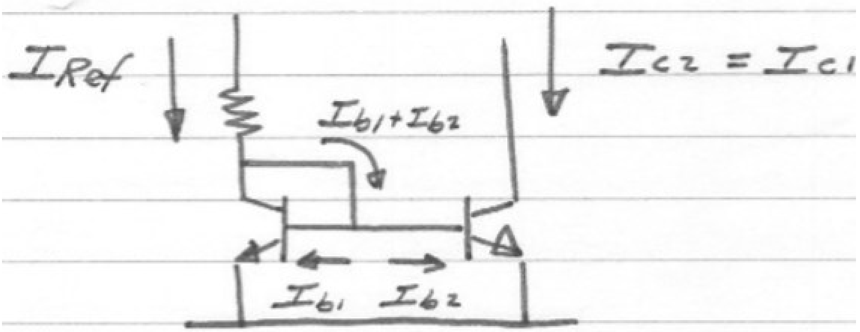
$$I_{c2} = I_{s2}\left(e^{V_{be2}/V_T} - 1\right)$$

$$\boxed{I_{c2} = \frac{I_{s2}}{I_{s1}} \cdot I_{c1} = \frac{A_{E2}}{A_{E1}} I_{c1}}$$

We can set up a desired ratio of currents

We can set up a desired ratio of currents by using transistors with a defined ratio of emitter areas

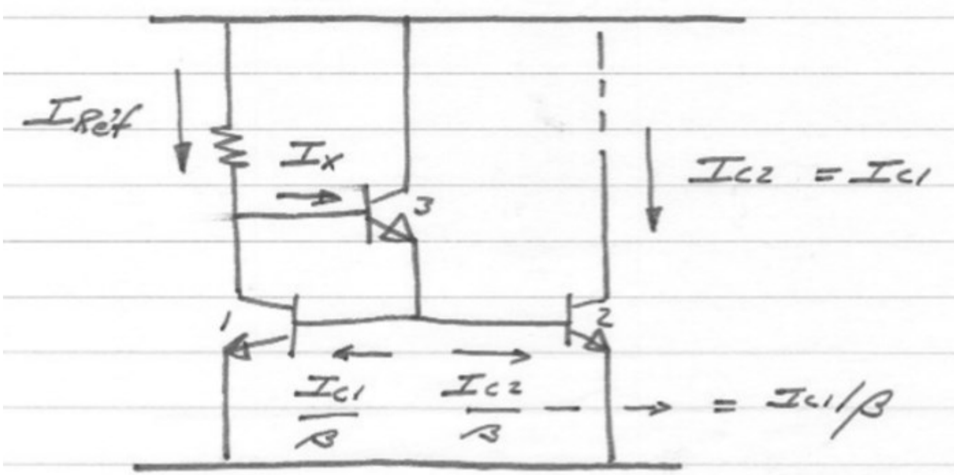
Effects of base currents



$$I_{Ref} = I_{c1} + 2I_{c1}/\beta$$

$$\Rightarrow I_{c1} = \frac{I_{Ref}}{1+2/\beta}$$

If base currents have too large an effect, then do this:

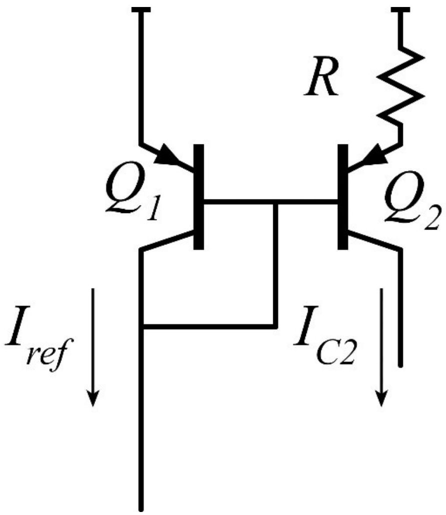


$$I_x = 2I_{c1}/\beta^2$$

$$\Rightarrow$$

$$I_{c1} = \frac{I_{Ref}}{1+2/\beta^2}$$

Reducing current with a resistor (Widlar)



$$V_{be1} = V_T \ln(I_{C1} / I_{S1})$$

$$V_{be2} = V_T \ln(I_{C2} / I_{S2})$$

But:

$$V_{be1} = V_{be2} + I_{C2}R$$

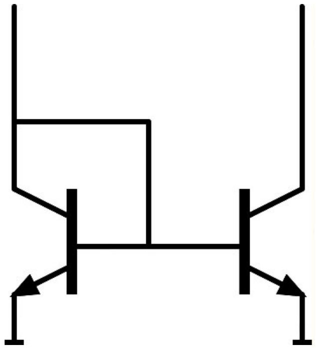
$$V_T \ln(I_{C1} / I_{S1}) = V_T \ln(I_{C2} / I_{S2}) + I_{C2}R$$

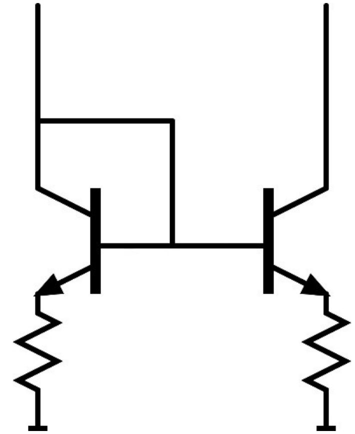
$$V_T \ln(I_{C1}I_{S2} / I_{C2}I_{S1}) = I_{C2}R$$

$$I_{C2}R = V_T \ln\left(\frac{I_{C1}}{I_{C2}} \cdot \frac{I_{S2}}{I_{S1}}\right) = V_T \ln\left(\frac{I_{C1}}{I_{C2}} \cdot \frac{A_{E2}}{A_{E1}}\right)$$

We can use a resistor to set up a desired current ratio

Mirrors: Textbook vs. practical design





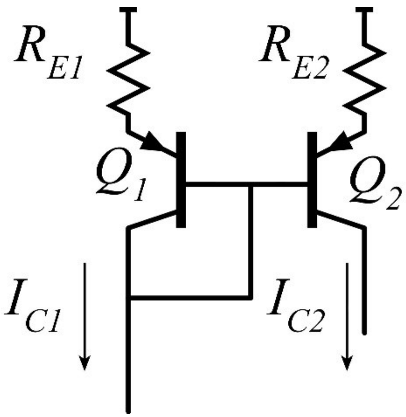
Textbooks frequently show mirrors without resistors.

Such designs are frequently *thermally unstable*.

Adding at least small resistors avoids this.

We will examine this in detail later.

Current Mirrors with resistors



$$V_{be1} + I_{E1}R_{E1} = V_{be2} + I_{E2}R_{E2} \quad \text{and: } V_{be} = V_T \ln(I_C / I_S)$$

so

$$V_T \ln(I_{E1} / I_{S1}) + I_{E1}R_{E1} = V_T \ln(I_{E2} / I_{S2}) + I_{E2}R_{E2}$$

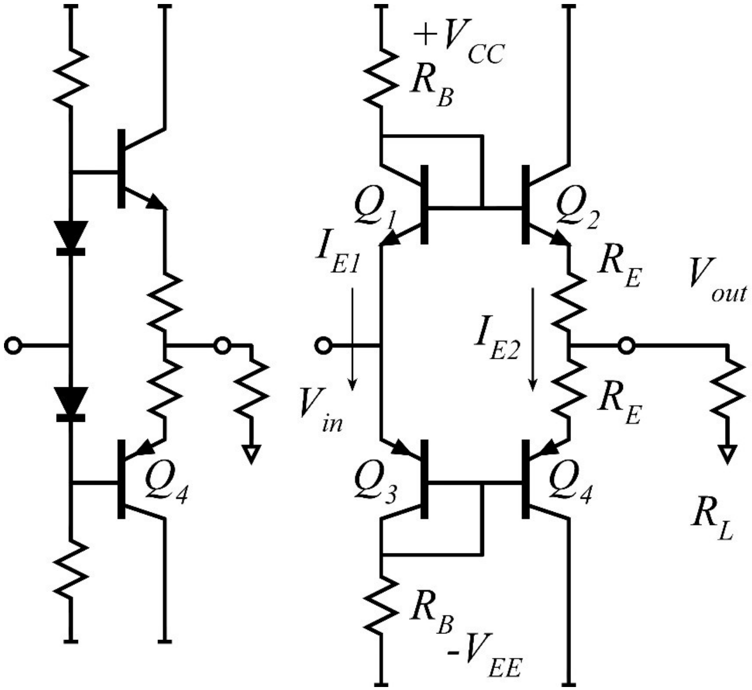
$$\rightarrow V_T \ln\left(\frac{I_{E1}}{I_{E2}}\frac{I_{S2}}{I_{S1}}\right) = I_{E2}R_{E2} - I_{E1}R_{E1}$$

Even if $(I_{E1}I_{S2}/I_{E2}I_{S1})$ were 3, $(kT/q)\ln(10)$ is only 30mV.

So, if we make the IR drops >>60mV, then the currents tend to be controlled by the resistor ratios, not by the I_S ratios.

Particularly useful if using discrete parts, as transistors then will be poorly-matched

Push-pull output stage.



Q_1: diode-connected transistor, matched to Q_2.

Q_3: diode-connected transistor, matched to Q_4.

First do bias analysis: $V_{in} = V_{out} = 0\text{V}$.

$$V_{be1} + V_{be3} = V_{be2} + V_{be4} + 2I_{E2}R$$

but:

$$V_{be} = V_T \ln(I_C / I_S)$$

so

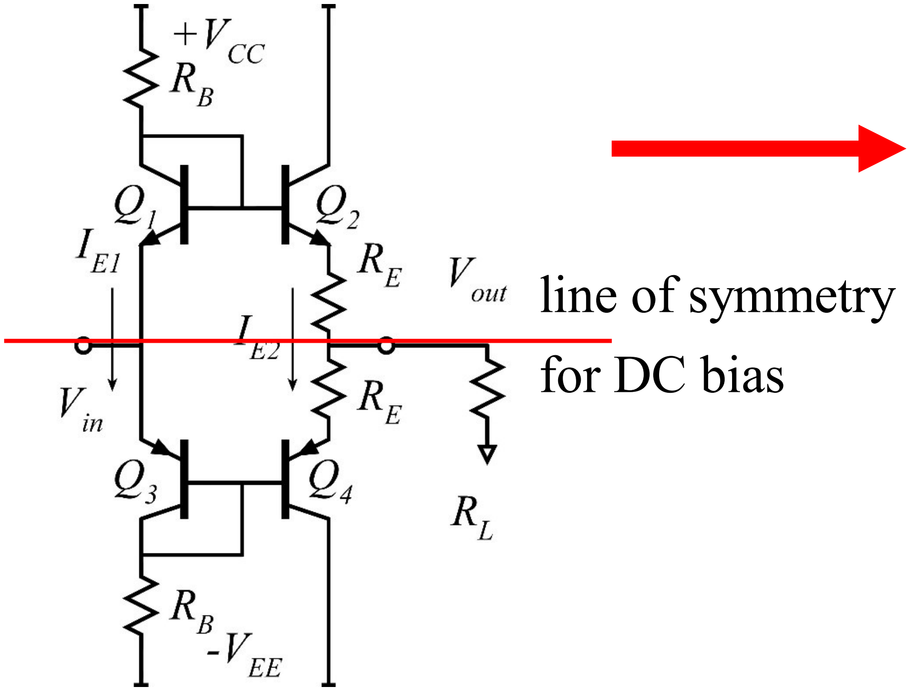
$$V_T \ln(I_{E1} / I_{S1}) + V_T \ln(I_{E3} / I_{S3}) = V_T \ln(I_{E2} / I_{S2}) + V_T \ln(I_{E4} / I_{S4}) + 2I_{E2}R$$

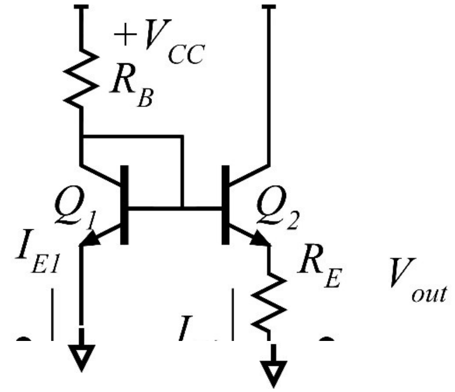
So: $V_T \ln\left(\frac{I_{E2}^2}{I_{E1}^2} \frac{I_{S1} I_{S3}}{I_{S2} I_{S4}} \right) = 2I_{E2}R$

Assuming matching, i.e. $I_{S1} = I_{S3}$, $I_{S2} = I_{S4} :\rightarrow V_T \cdot \ln\left(I_{E2} / I_{E1}\right) = I_{E2}R$

$$V_T \cdot \ln\left(I_{E2} / I_{E1}\right) = I_{E2}R$$

Push-pull output stage.



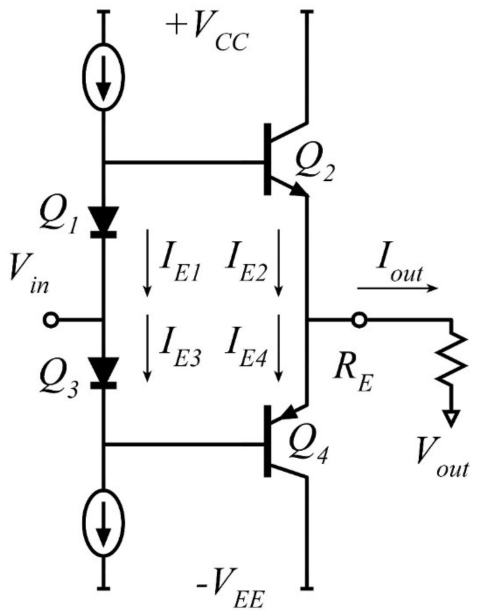


$$V_T \cdot \ln\left(I_{E2} / I_{E1}\right) = I_{E2}R$$

$$V_T \cdot \ln\left(I_{E2} / I_{E1}\right) = I_{E2}R$$

DC bias analysis is same as for current mirror

Push-pull output stage: AC operation



Approximately greatly: we just seek understanding

(1) Ignore emitter resistors.

(2) replace R_B with current source, set $\beta=\infty$.

The latter forces $I_{E1}=I_{E3}$ even under AC operation

$$V_{be1}+V_{be3}=V_{be2}+V_{be4}$$

$$V_T\ln\left(I_{E1}/I_{S1}\right)+V_T\ln\left(I_{E3}/I_{S3}\right)=V_T\ln\left(I_{E2}/I_{S2}\right)+V_T\ln\left(I_{E4}/I_{S4}\right)$$

$$\rightarrow I_{E1}I_{E3}/I_{S1}I_{S3}=I_{E2}I_{E4}/I_{S2}I_{S4}$$

but: $I_{S1}=I_{S2}$, $I_{S3}=I_{S4}$, $I_{E1}=I_{E3}$, so: $I_{E2}I_{E4}=I_{E1}^2$

$$I_{E2}I_{E4}=I_{E1}^2.\quad \text{But } I_{out}=V_{out}/R_L=I_{E2}-I_{E4}$$

Strong positive output ($I_{out}>>I_{E1}$):

$$I_{out}=I_{E2}-I_{E4}=I_{E2}-I_{E1}^2/I_{E2.}$$

$$\rightarrow I_{E2}\cong I_{out} \text{ and } I_{E4}\cong I_{E1}^2/I_{out}$$

$\rightarrow Q_2$ carries the output current and Q_4 is almost off

Strong negative output ($-I_{out}>>I_{E1}$):

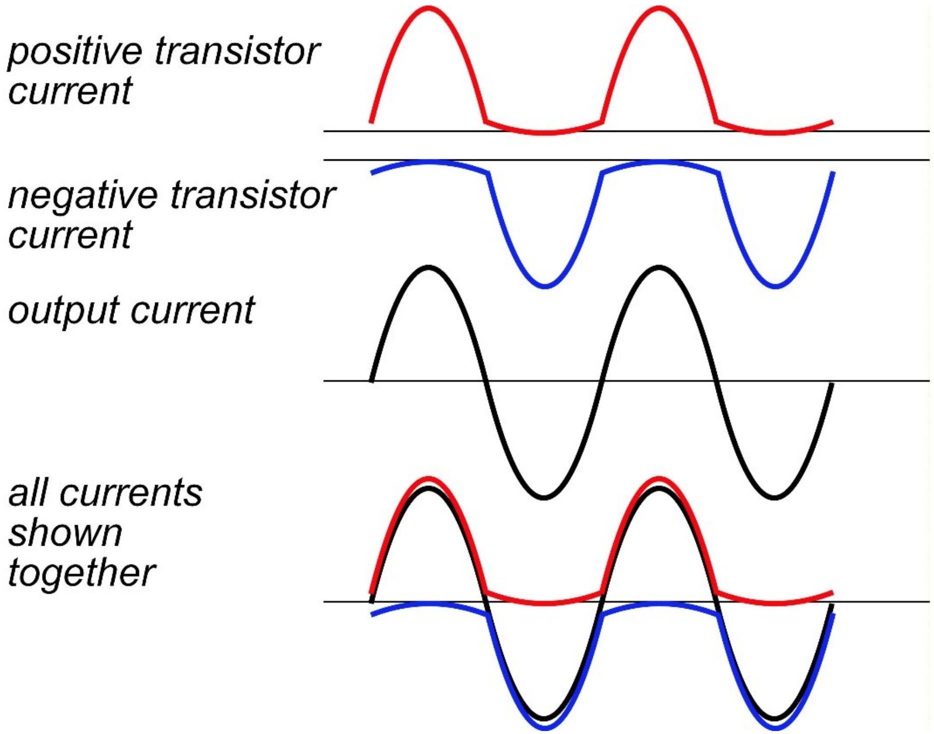
$$I_{out}=I_{E2}-I_{E4}=I_{E1}^2/I_{E4.}-I_{E4}$$

$$\rightarrow I_{E4}\cong -I_{out} \text{ and } I_{E4}\cong I_{E1}^2/(-I_{out})$$

$\rightarrow Q_4$ carries the output current and Q_2 is almost off

Push-pull waveforms

Sketch of the current waveforms:



The positive transistor carries the positive output current

The negative transistor carries the negative output current

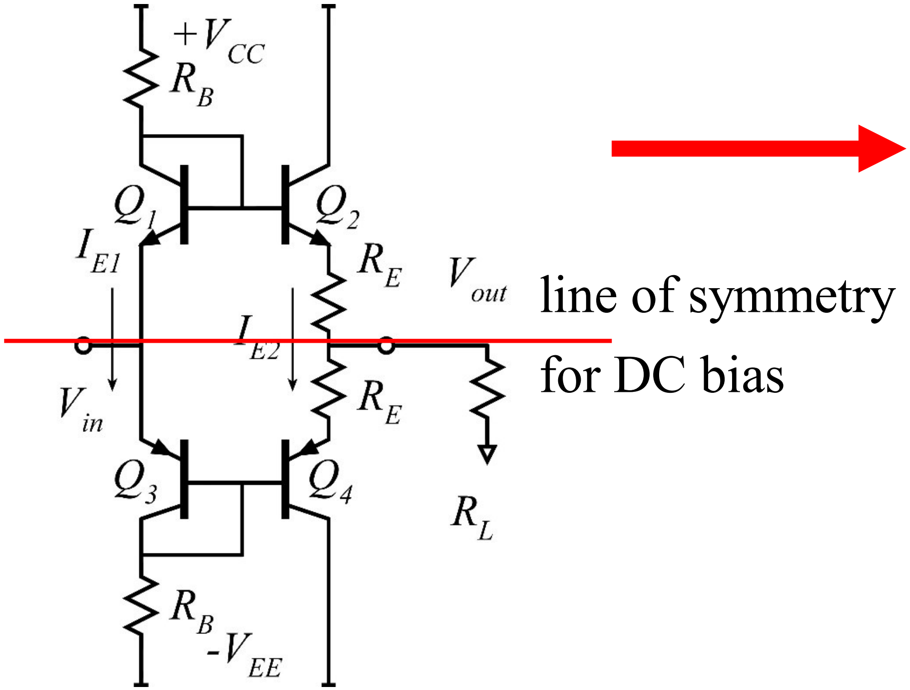
Benefit of push-pull output stage:

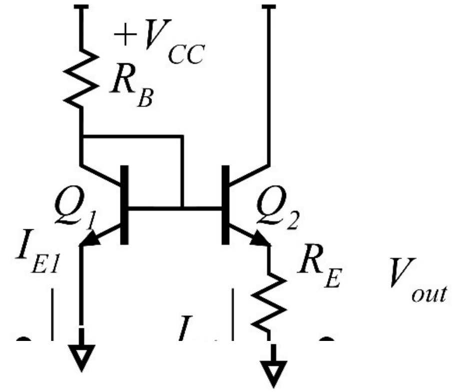
No clipping limit due to cutoff

→ No need for large bias current

even if stage must deliver large output current.

Thermal instabilty: mirrors and push-pull stages



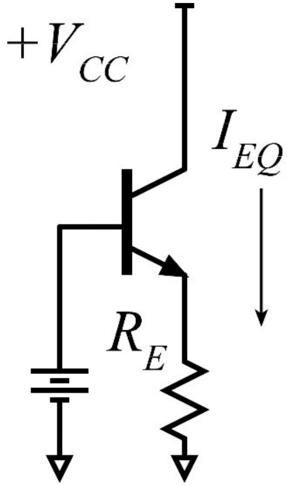


$$\ln\left(I_{E2} / I_{E1}\right) = I_{E2} R$$

Mirrors and push-pull stages are prone to thermal instability

The analysis is the same for the two circuits

Thermal instabilty: mirrors and push-pull stages



This equivalent circuit will model both problems

The problem: V_{be} decreases with junction temperature

Increased junction temperature

$\rightarrow$ decreased V_{be}

$\rightarrow$ increased current

$\rightarrow$ increased power in transistor

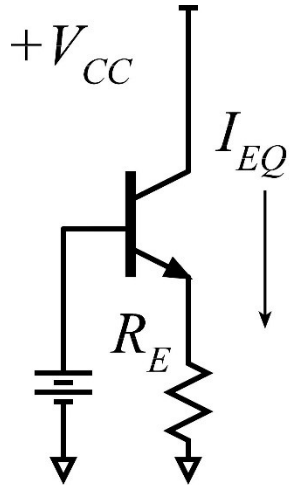
$\rightarrow$ increased junction temperature

$\rightarrow$ ....

Current can increase without limit

Can lead to transistor self-destruction

Thermal instabilty: definition of terms



$$\left.\frac{dV_{be}}{dT}\right|_{\text{at fixed } I_C} \approx -2.2\text{mV/K for Si bipolars}$$

$$\frac{dT}{dP} = \text{Thermal resistance} = \theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA}$$

θ_{JA} = Junction-to-ambient thermal resistance

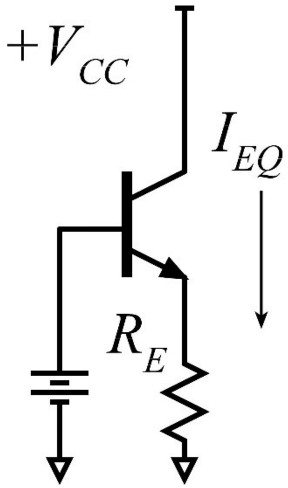
θ_{JC} = Junction-to-case thermal resistance

θ_{CH} = case-to-heatsink thermal resistance

θ_{HA} = heatsink-to-ambient thermal resistance

$P = I_E V_{CC}$ = Device power dissipation

Thermal instabilty: analysis



Assume a infinitesimal change in temperature δT

$$\delta V_{be} = -\left.\frac{dV_{be}}{dT}\right|_{I_C} \delta T$$

$$\delta I_E = (-\delta V_{be})/(R_E + 1/g_m)$$

$$\delta P = V_{CC} \cdot \delta I_E$$

$$\delta T = \theta_{JA} \cdot \delta P$$

The series $1 + x + x^2 + x^3 + ...$ diverges if $|x| > 1$

So, to be thermally stable, we must have $K_{themal} < 1$,

where $K_{thermal} = \left(\left.\frac{-dV_{be}}{dT}\right|_{I_C} \right) \frac{V_{CC}\theta_{JA}}{R_E + 1/g_m}$

We need either a good heatsink, significant emitter resistance, or both.