ECE 2C, notes set 3: Small-Signal Models of Active Devices

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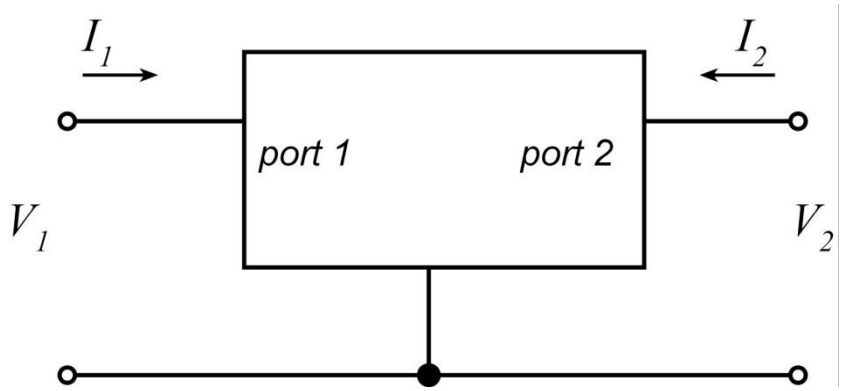
Goals of this note set:

What is a two-port (input, output) network?

Linear vs. nonlinear circuit elements

How to make linear small-signal models of nonlinear devices

2-Port Descriptions (3-Wire Network or Device)

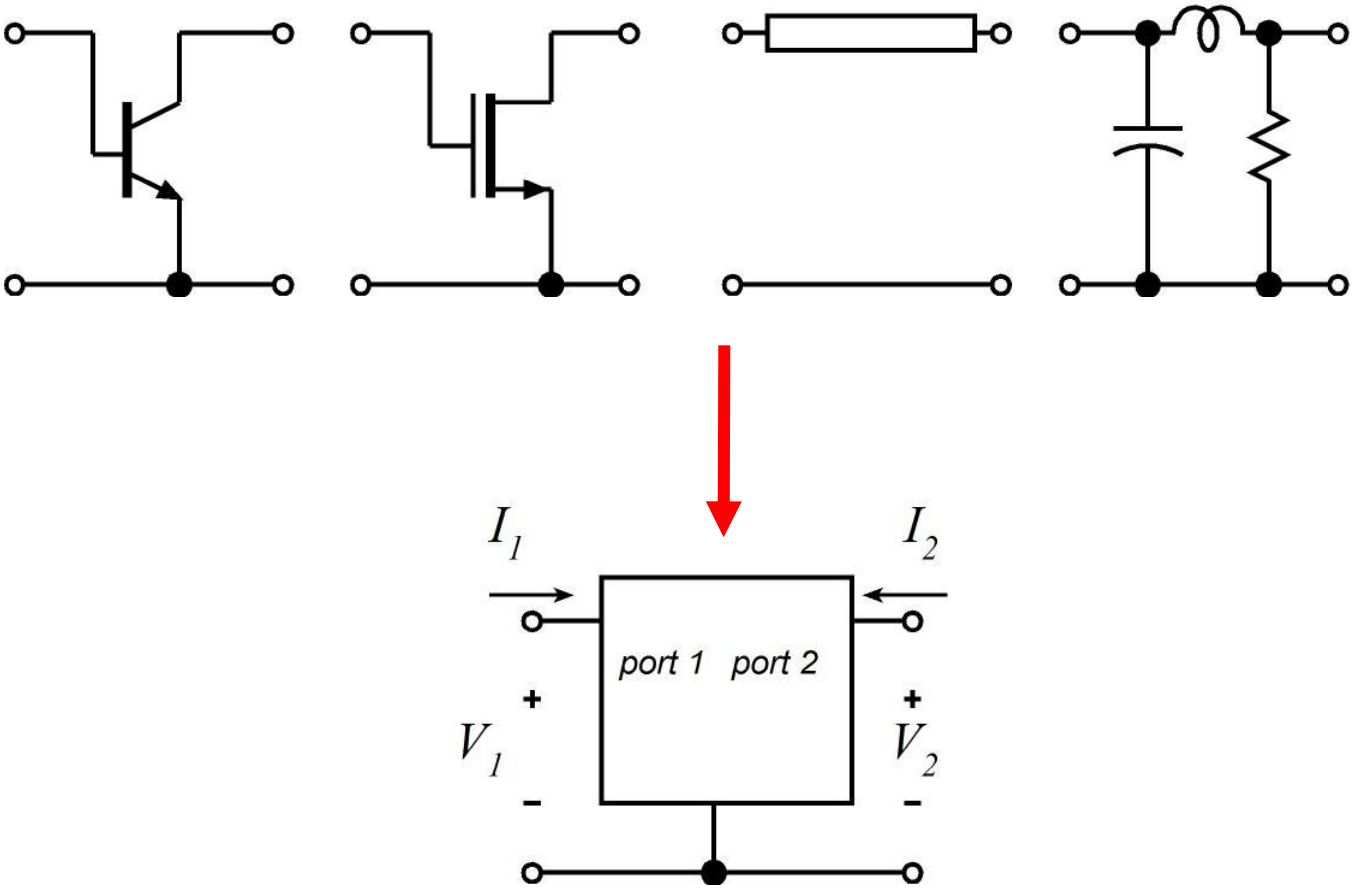


Box might contain : a transistor, a passive element, a subcircuit

The terminal characteristics relate the variables V_1, V_2, I_1, and I_2.
There are 2 degrees of freedom.

Any two variables can be set as the *independent variables*.
The remaining two variables, the *dependent variables*,
can then be written as functions of the independent variables.

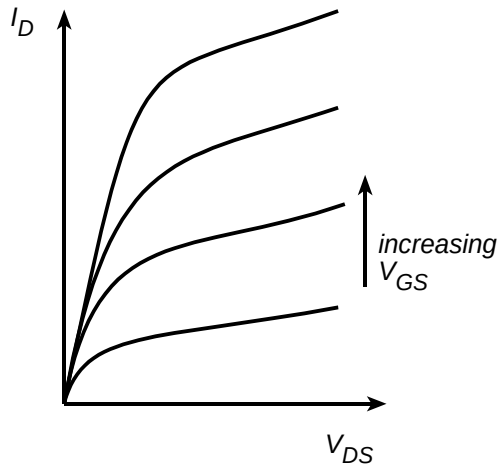
Two-Port Parameters: Represent Device or Network



We can use a two-port to represent any network.

But, now our focus is on modeling active devices.

Transistors are Nonlinear Elements



$$I_{D,\mu} = (\mu c_{ox} W_g / 2L_g)(V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$$

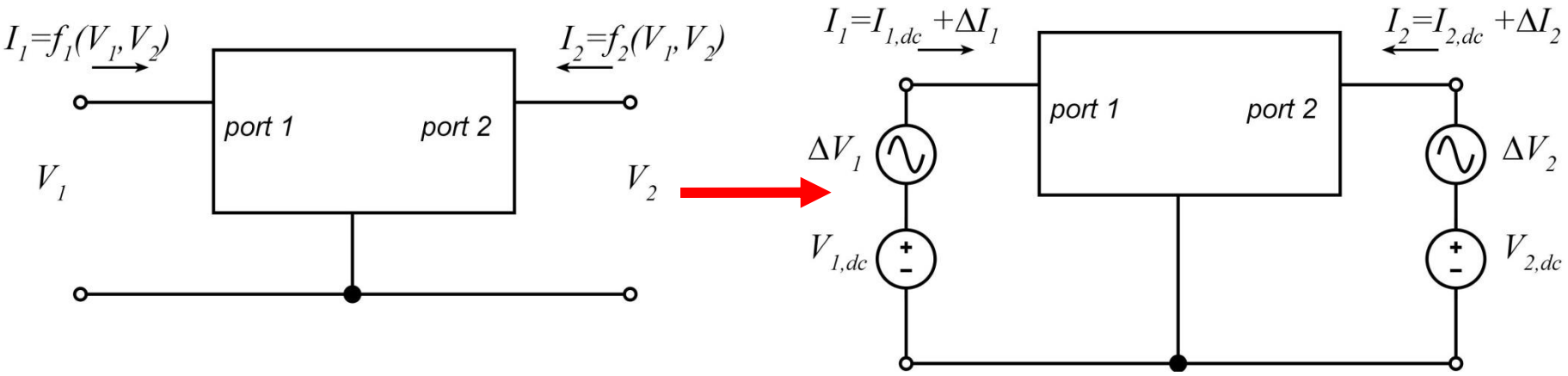
Transistor currents are nonlinear functions of the applied voltages.

The principle of superposition does not apply.

Exact transistor circuit analysis is therefore very difficult.

Analysis is made easy if we assume *small signals *

A Nonlinear Two-Port



The currents are nolinear functions of the voltages.

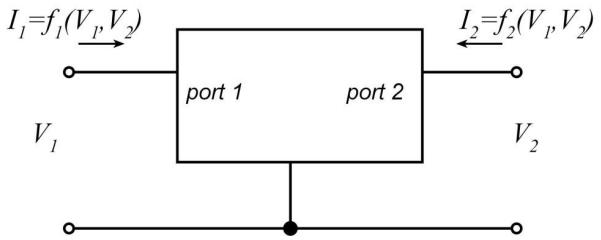
In transistor circuits, the voltages and currents are often sums of DC bias voltages and DC bias currents

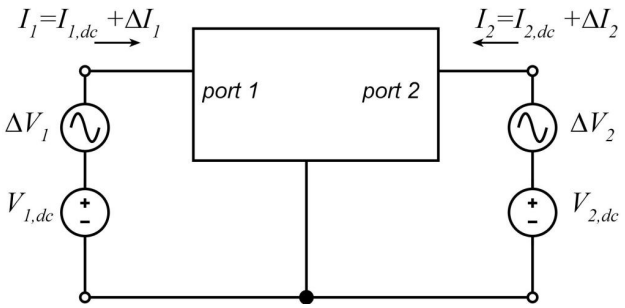
plus

AC signal voltages and AC signal currents.

...and the AC signals are often very small (but not always).

Nonlinear Two-Port Characteristics





Write a Taylor series...

$$\Delta I_1 = \frac{\partial I_1}{\partial V_1}\Delta V_1 + \frac{\partial I_1}{\partial V_2}\Delta V_2 + \frac{\partial^2 I_1}{\partial^2 V_1}\frac{(\Delta V_1)^2}{2} + \frac{\partial^2 I_1}{\partial^2 V_2}\frac{(\Delta V_2)^2}{2} + \frac{\partial^2 I_1}{\partial V_1 \partial V_2}(\Delta V_1 \Delta V_2) + \ldots$$

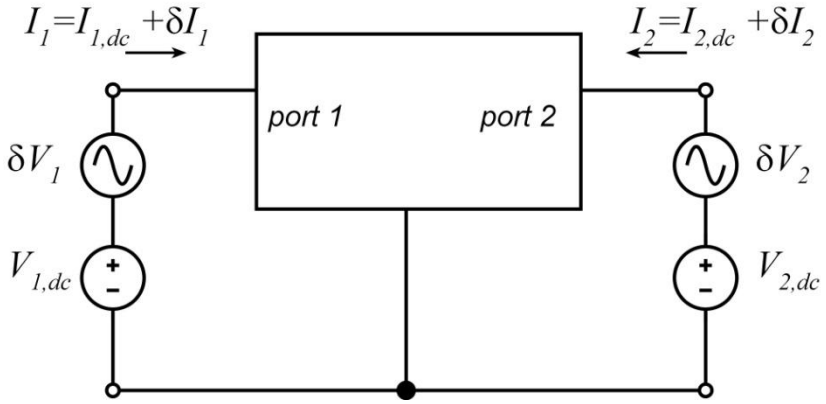
$$\Delta I_2 = \frac{\partial I_2}{\partial V_1}\Delta V_1 + \frac{\partial I_2}{\partial V_2}\Delta V_2 + \frac{\partial^2 I_2}{\partial^2 V_1}\frac{(\Delta V_1)^2}{2} + \frac{\partial^2 I_2}{\partial^2 V_2}\frac{(\Delta V_2)^2}{2} + \frac{\partial^2 I_2}{\partial V_1 \partial V_2}(\Delta V_1 \Delta V_2) + \ldots$$

This is still very complicated.

But if ΔV_1 and ΔV_2 are small, then $(\Delta V_1)^2$, $(\Delta V_2)^2$, and $(\Delta V_1 \Delta V_2)$ are even smaller.

In this case, we can neglect all but the first-order terms in the Taylor series

Assuming Small Signals (Derivatives)



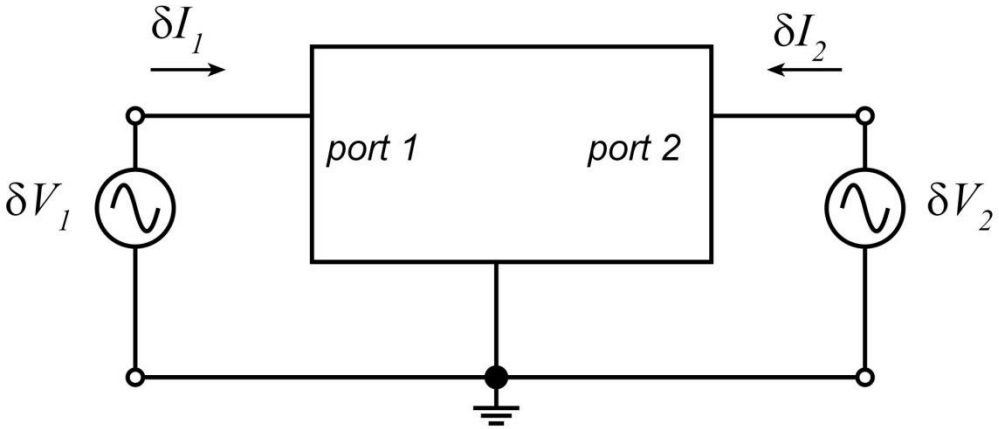
If ΔV_1 and ΔV_2 are very small $\rightarrow$ write δV_1 and δV_2 instead.

$$\delta I_1 = \frac{\partial I_1}{\partial V_1}\delta V_1 + \frac{\partial I_1}{\partial V_2}\delta V_2 + \ldots$$

$$\delta I_2 = \frac{\partial I_2}{\partial V_1}\delta V_1 + \frac{\partial I_2}{\partial V_2}\delta V_2 + \ldots$$

We can neglect the higher - order terms if δV_1 and δV_2 are small.

Small-Signal 2-Port Admittance Parameters



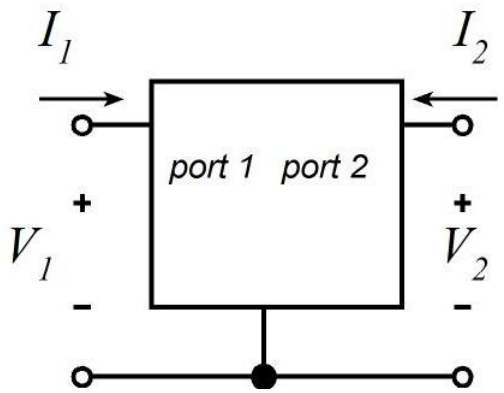
DC voltages & currents are taken as implicit (..are not shown)

$$\delta I_1 = Y_{11}\delta V_1 + Y_{12}\delta V_2$$
$$\delta I_2 = Y_{21}\delta V_1 + Y_{22}\delta V_2$$

Where

$$Y_{11} = \frac{\partial I_1}{\partial V_1} \quad Y_{12} = \frac{\partial I_1}{\partial V_2}$$
$$Y_{21} = \frac{\partial I_2}{\partial V_1} \quad Y_{22} = \frac{\partial I_2}{\partial V_2}$$

Admittance Parameters



Frequency - domain description :

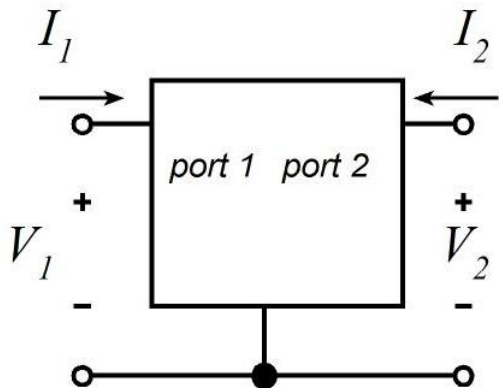
$$v_1(t) = \mathrm{Re}\left\{V_1 e^{j\omega t}\right\} \quad , i_1(t) = \mathrm{Re}\left\{I_1 e^{j\omega t}\right\}, \text{ etc.}$$

$$\begin{bmatrix} I_1(j\omega) \\ I_2(j\omega) \end{bmatrix} = \begin{bmatrix} Y_{11}(j\omega) & Y_{12}(j\omega) \\ Y_{21}(j\omega) & Y_{22}(j\omega) \end{bmatrix} \begin{bmatrix} V_1(j\omega) \\ V_2(j\omega) \end{bmatrix}$$

Currents are written as functions of voltages.

DC bias is taken as implicit.

Side Point: Impedance Parameters



$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

Voltages are written as functions of currents.

The Z matrix is the inverse of the Y matrix.

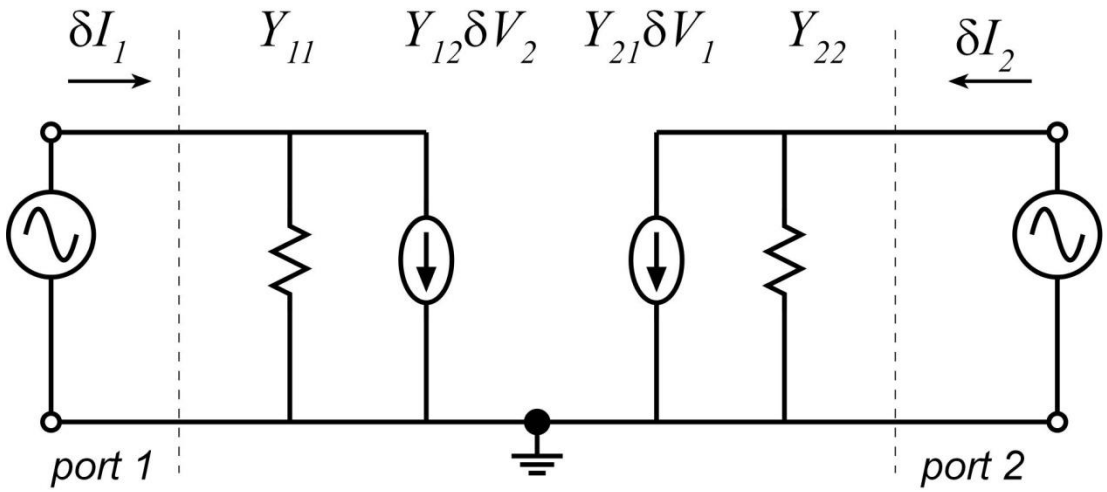
General Comment About 2-Port Parameters

There is much more to discuss about 2-port parameters.

My view: this can be left until the Junior or Senior years.

We have introduced 2-port parameters because they provide a natural way to explain transistor small-signal models.

Small-Signal Equivalent-Circuit

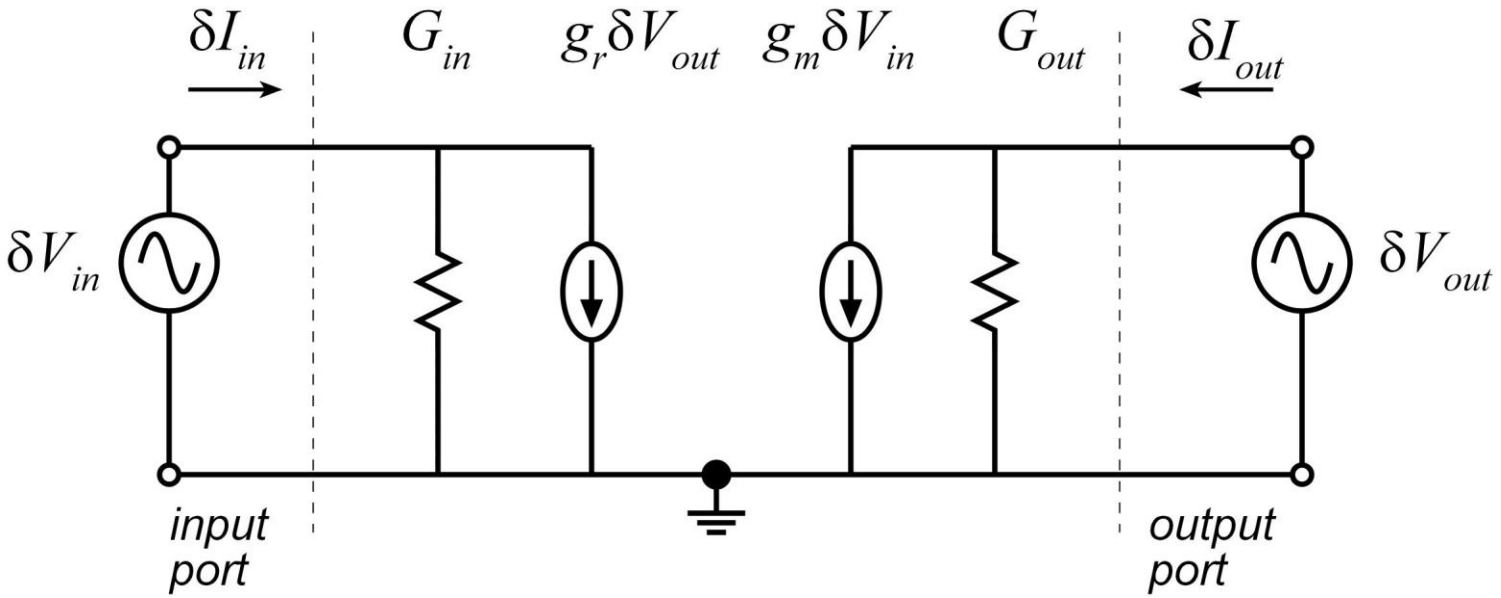


$$\delta V_2 \quad \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

We are now representing the four Y-parameters
as two admittances and two controlled current generators.

So far, we have assumed $Y(j\omega)$ might vary with frequency
and might have real and imaginary parts: $Y(j\omega) = G(j\omega) + jB(j\omega)$

Small-Signal Equivalent-Circuit



Now suppose that the Y-parameters do not vary with frequency, and have no imaginary parts. $Y(j\omega) \rightarrow G$

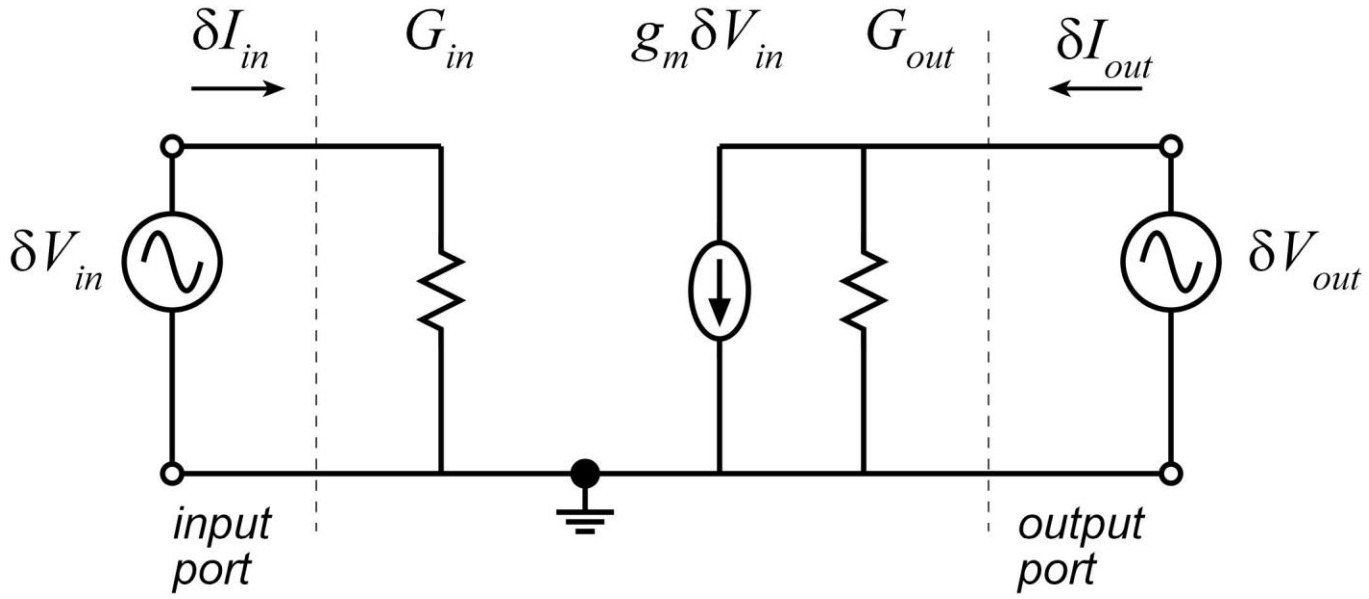
Note that we have also changed the notation:

$$G_{11} \rightarrow G_{in} = \frac{\partial I_{in}}{\partial V_{in}} = \text{input conductance} \qquad G_{22} \rightarrow G_{out} = \frac{\partial I_{out}}{\partial V_{out}} = \text{output conductance}$$

$$G_{21} \rightarrow g_m = \frac{\partial I_{out}}{\partial V_{in}} = \text{transconductance} \qquad G_{12} \rightarrow g_r = \frac{\partial I_{in}}{\partial V_{out}} = \text{reverse transconductance}$$

For transistors (but not other 2-ports), g_r is usually negligible.

Small-Signal Equivalent-Circuit: Neglecting Gr.

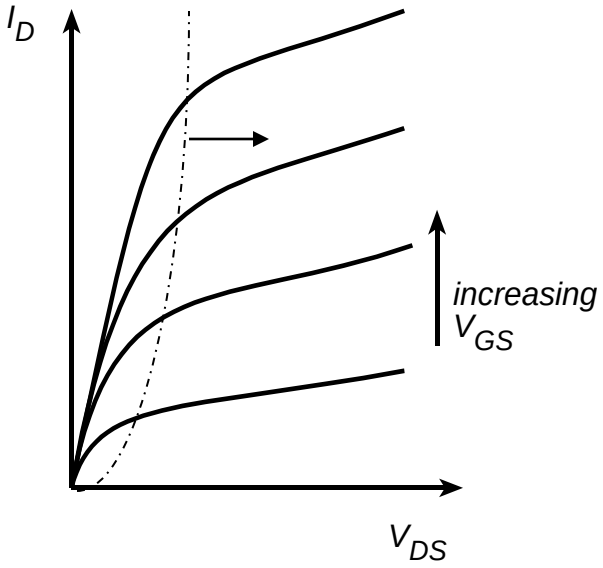


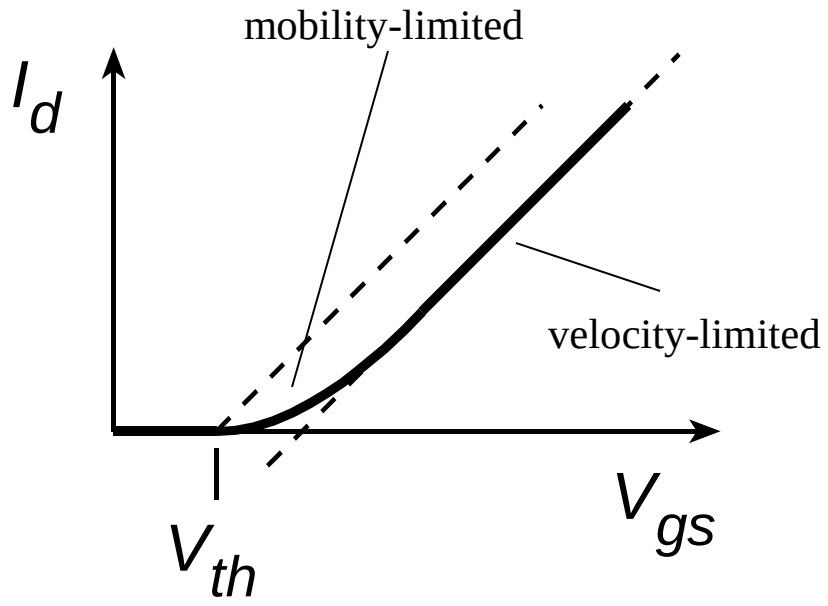
$$G_{in} = \frac{\partial I_{in}}{\partial V_{in}} = \text{input conductance} \qquad G_{out} = \frac{\partial I_{out}}{\partial V_{out}} = \text{output conductance}$$

$$g_m = \frac{\partial I_{out}}{\partial V_{in}} = \text{transconductance}$$

This is a typical transistor low-frequency equivalent circuit model.

Recall MOSFET Characteristics: Mobility-Limited Case



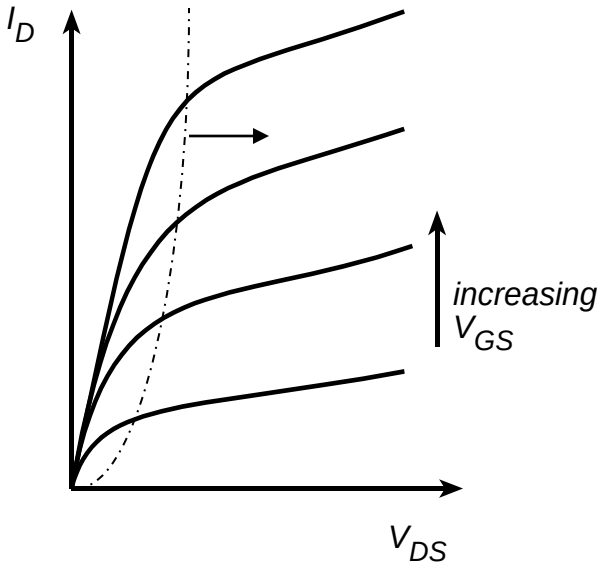


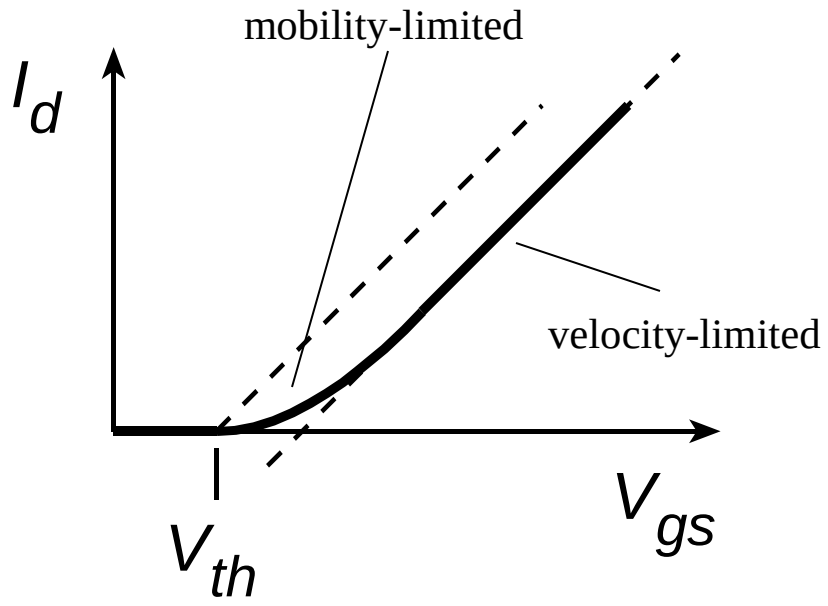
mobility – limited current :

$$I_{D,\mu} = (\mu c_{ox} W_g / 2L_g)(V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$$

Applies for drain voltages larger than the knee voltage,

Recall MOSFET Characteristics: Velocity-Limited Case





velocity – limited current

$$I_{D,v} = c_{ox} W_g v_{sat} (1 + \lambda V_{DS})(V_{gs} - V_{th} - \Delta V)$$

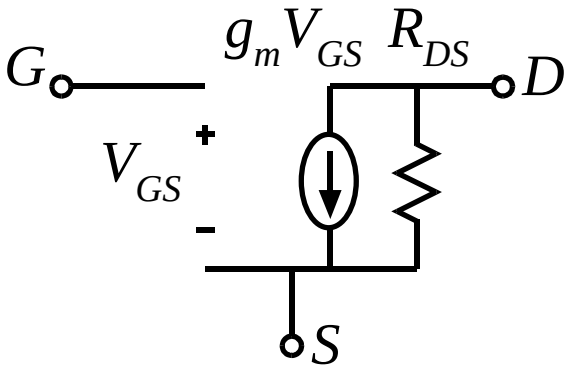
$$\Delta V = v_{sat} L_g / \mu$$

Applies for drain voltages larger than the knee voltage,

FET Small-Signal Model: Mobility-Limited

Drain Current

$$I_{D,\mu} = (\mu c_{ox} W_g / 2L_g)(V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$$



Transconductance

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} = (\mu c_{ox} W_g / L_g)(V_{gs} - V_{th})(1 + \lambda V_{DS}) \approx (\mu c_{ox} W_g / L_g)(V_{gs} - V_{th})$$

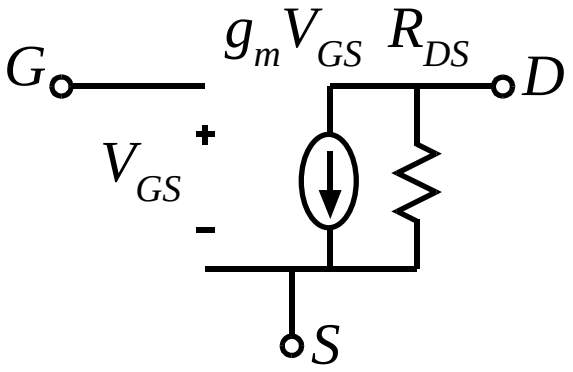
Output Conductance

$$G_{ds} = \frac{1}{R_{ds}} \equiv \frac{\partial I_D}{\partial V_{DS}} = \frac{\lambda I_D}{1 + \lambda V_{DS}}$$

$$\cong \lambda I_D \text{ to within the accuracy of the models we are using}$$

Note that R_{ds} varies roughly as $1/I_D$.

FET Small-Signal Model: Velocity-Limited



Drain Current

$$I_{D,v} = c_{ox} v_{sat} W_g (1 + \lambda V_{DS})(V_{gs} - V_{th} - \Delta V)$$

Transconductance

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} = c_{ox} v_{sat} W_g (1 + \lambda V_{DS}) \approx c_{ox} v_{sat} W_g$$

OutputConductance

$$G_{ds} = \frac{1}{R_{ds}} \equiv \frac{\partial I_D}{\partial V_{DS}} = \frac{\lambda I_D}{1 + \lambda V_{DS}}$$

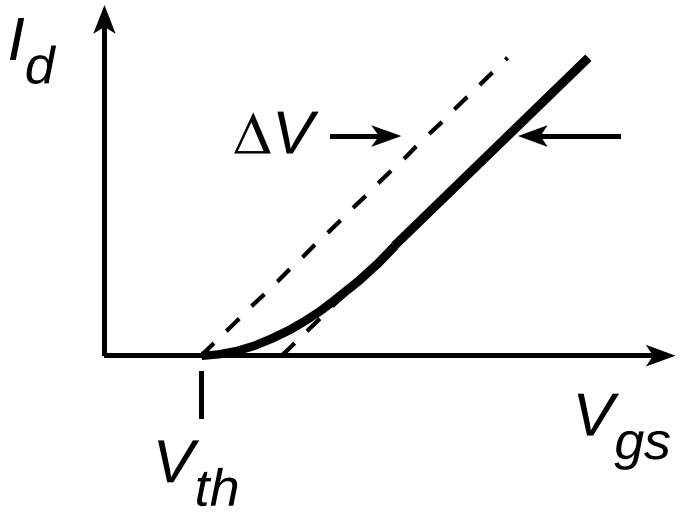
$$\cong \lambda I_D$$

Transconductance vs Vgs

mobility – limited

$$I_{D,\mu} = \mu c_{ox} W_g (V_{gs} - V_{th})^2 / 2L_g$$

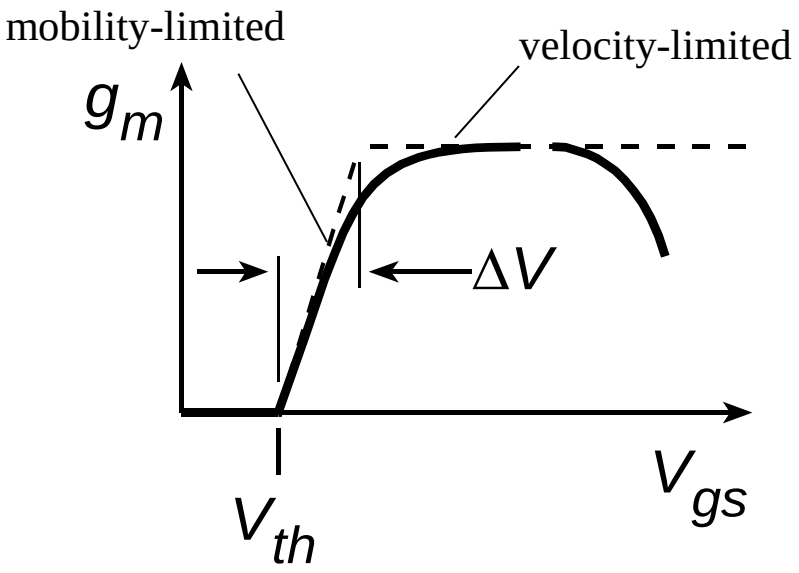
$$\rightarrow g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu c_{ox} W_g (V_{gs} - V_{th}) / L_g$$



velocity – limited

$$I_{D,v} = c_{ox} W_g v_{sat} (V_{gs} - V_{th} - \Delta V)$$

$$\rightarrow g_m = \frac{\partial I_D}{\partial V_{GS}} = c_{ox} W_g v_{sat}$$



Rough Estimate: 250 nm NMOS Characteristics

These are rough numbers - not real VLSI parameters

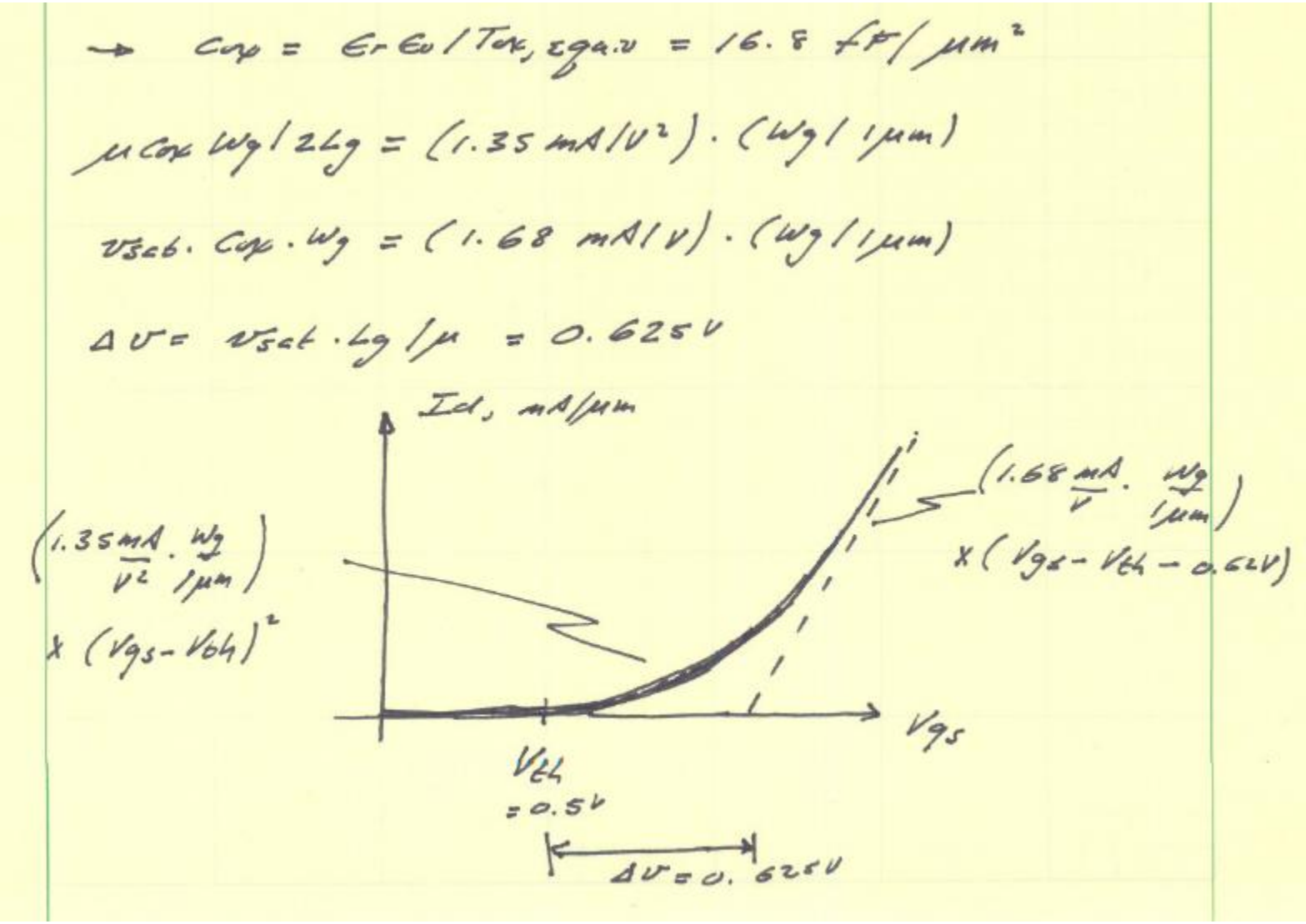
Case 1 250nm NMOS

$\mu = 400\ cm^2/V\cdot s$ $T_{ox,eqv} = 2\ nm$, $\kappa = 3.8$

$L_g = 1/4\ \mu m$ $v_{sat} \sim 10^7\ cm/s$

$V_{th} \cong 0.5V$

Rough Estimate: 250 nm NMOS Characteristics



Rough Estimate: 250 nm PMOS Characteristics

$\mu \sim 200\ cm^2/V\cdot sec$ $\quad T_{ox,\,Equ.} = 2\ nm, \quad \epsilon_r = 3.9$

$L_g = 1/4\ \mu m$ $\quad v_{sat} \sim 0.5 \cdot 10^7\ cm/s$

$|V_{GT}| = 0.5V$

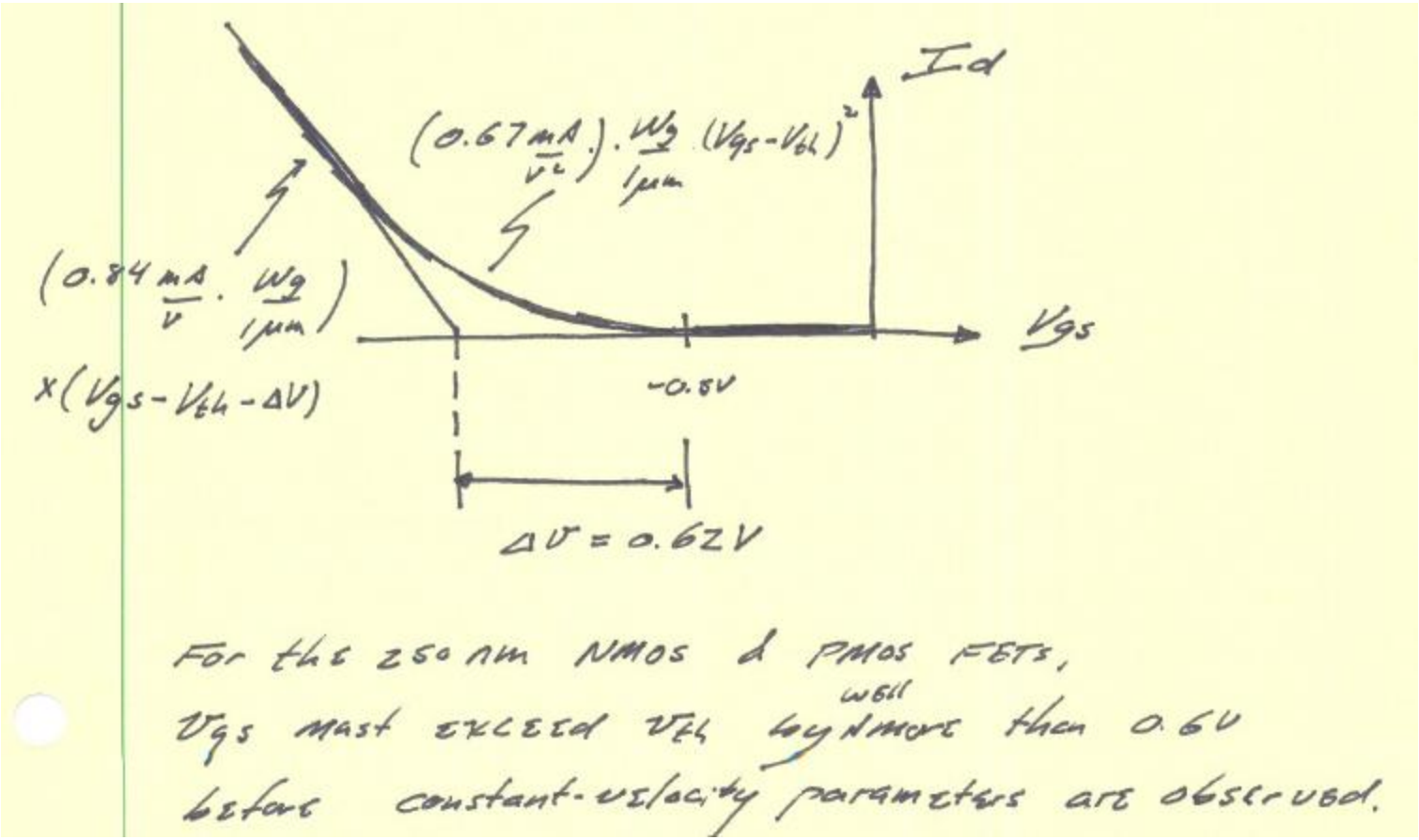
$\rightarrow \Delta V = v_{sat} L_g/\mu = 0.625\ V.$

$\rightarrow C_{ox} = \epsilon_r \epsilon_0 / T_{ox,\,Equ.} = 16.8\ fF/\mu m^2$

$\mu \cdot C_{ox} \cdot W_g / 2L_g = (0.67\ mA/V^2) \cdot (W_g / 1\mu m)$

$v_{sat} \cdot C_{ox} \cdot W_g \simeq (0.84\ mA/V) \cdot (W_g / 1\mu m)$

Rough Estimate: 250 nm PMOS Characteristics



Rough Estimate: 45 nm NMOS Characteristics

$\mu \sim 300\ cm^2/V.sec$ $\quad T_{ox,\,equiv} = 1.2\ nm,\ \kappa = 3.8$

$L_g = 45\ nm$ $\quad v_{sat} \sim 10^7\ cm/sec$

$V_{tL} = 0.3\ V$

$v_{sat} \cdot L_g / \mu = \Delta V = 0.15\ V$

$\mu \cdot C_{ox} \cdot W_g / 2L_g = (9.35\ mA/V^2) \cdot (W_g / 1\ \mu m)$

$C_{ox} \cdot v_{sat} \cdot W_g = (2.8\ mA/V) \cdot (W_g / 1\ \mu m)$

Rough Estimate: 45 nm NMOS Characteristics

note - this device is velocity-limited once $(V_{gs} - V_t)$ exceeds about 0.2V

note: production 45nm NMOS FETs, circa 2007, have roughly 1/2 the current calculated above; the physical parameters I have used are rough estimates.

Rough Estimate: 45 nm PMOS Characteristics

$\mu \sim 150\ cm^2/V\cdot sec$ $\quad T_{ox,EOT} = 1.2nm,\quad \epsilon_r = 3.8$

$L_g = 45nm$ $\quad v_{sat} \sim 5\cdot 10^6\ cm/sec$

$|V_{th}| = 0.3V$

$v_{sat}\cdot L_g/\mu = \Delta V = 0.15V$

$\mu\cdot C_{ox}\cdot W_g/2L_g = (4.7\ mA/V^2)\cdot(W_g/1\mu m)$

$v_{sat}\cdot C_{ox}\cdot W_g = (1.4\ mA/V)\cdot(W_g/1\mu m)$

Rough Estimate: 45 nm PMOS Characteristics

once again, for this short-Lg device, very little gate overdrive ($V_{gs}-V_{tl}$) is needed before Id vs Vgs becomes velocity-saturated ($I_d \propto (V_{gs}-V_{tl}-\Delta V)$)

once again, these rough hand #'s give currents ~ 2:1 larger than real 45nm PMOS FETs.