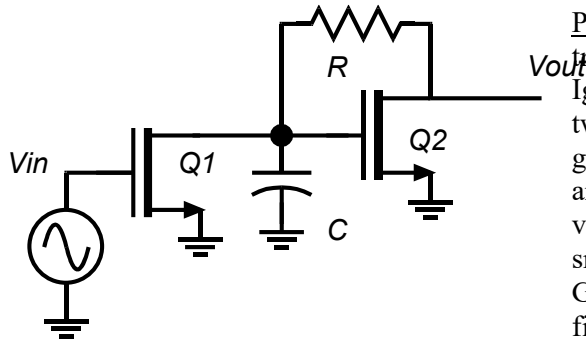
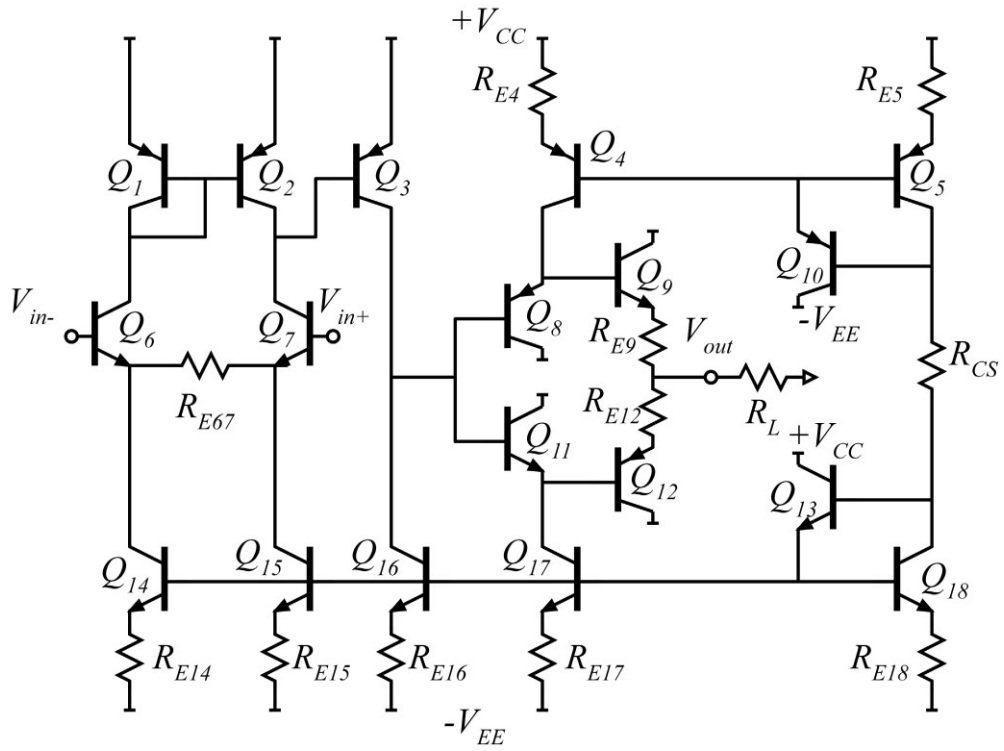
ECE137A Problem set 7



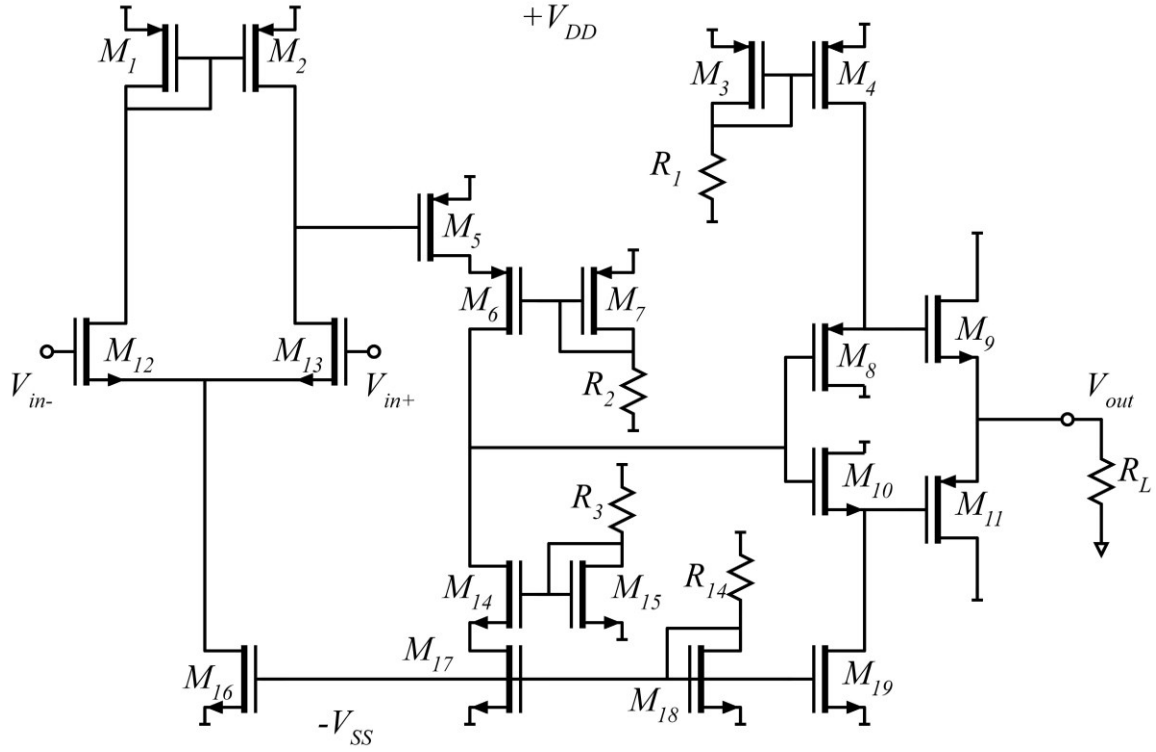
Problem 1: Nodal Analysis exercise: a transconductance-transimpedance amplifier. Ignore DC bias analysis. You don't need it. The two transistors have transconductance gm1 and gm2 respectively. Their output resistances Rds1 and Rds2 are both infinity. The capacitor C has value= zero Farads. (a)Find, by nodal analysis, a small-signal expression for Vout/Vin. (b) Gm1=20 mS. Gm2=10 mS. R=1kOhm. Again find Vout/Vin.

Problem 2:



This is an Op-Amp---analyze the bias under the assumption that DC output voltage is zero volts, that the positive input Vi+ is zero volts, and that we must determine the DC value of the negative input voltage (Vi-) necessary to obtain this. All the transistors have the same (matched) I_S, have β=500, and V_A = *infinity* Volts. $V_{CE(sat)}$=0.3V. V_{be} is approximately 0.7 V, but use $V_{be}=(kT/q)\ln(I_E/I_S)$ when necessary or appropriate. The supplies are +3 Volts and -3 Volts. All transistors have the same I_S. The resistors RE5 and RE18 have a 150mV DC voltage drop acoss them. Re67=200 Ohms, RL=2000 Ohms. DC bias currents: Ic6=Ic7=Ic9=Ic12=Ic18=50 μA. Ic3=Ic8=Ic11=0.1mA. (a) find all resistor values, (b) Find the overall differential gain $/V_{out}/(V_{in}^{+}-V_{in}^{-})$. (c) Find the maximum output voltage swings due to saturation of Q3,4,8,and 9.

Problem 3:



This is an Op-Amp---analyze the bias under the assumption that DC output voltage is zero volts, that the positive input Vi+ is zero volts, and that we must determine the DC value of the negative input voltage (Vi-) necessary to obtain this. The NMOSFETs have $K_\mu = 10\text{mA/V}^2 \cdot (W_g / 1\mu\text{m})$, $K_v = 2.0\text{mA/V} \cdot (W_g / 1\mu\text{m})$, $\Delta V = 100\text{mV}$, $1/\lambda$ =5 Volts, and a 0.25 V threshold. The PMOS FETs are the same, except have -0.25 V threshold. The PMOS have identical parameters, except, of course, V_{th} is negative. V_{DD} = +1 V, $-V_{SS}$ = -1 V, R_L=50 kOhm. All transistors have |Vgs|=0.30V, ***except for M7 and M15***, which have |Vgs|=0.35V.

M12,13 are biased at I_D=25 μA. M5,7,15 are biased at I_D=50 μA. M3,18,8,9,10,11 are biased at I_D=50 μA. (a) Find all FET gate widths (b) find the DC voltages at each circuit node. (c) Find the overall differential gain $/V_{out} / (V_{in}^+ - V_{in}^-)$. (d) Find the maximum output voltage swings due tothe knee voltages of M8,9,4, and 6.