# ECE 137 B: Notes Set 14
# Feedback loop compensation

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# Not just about transistor circuits

Negative feedback is used widely in transistor circuits.

Negative feeback is used far more widely than just in transistor circuits.
Home heating control (thermostat, etc)
Modern aircraft: electronic control of roll, pitch, yaw.
Cars: anti-lock braking, electronic stability enhancement, air/fuel mixture...
Robotics and machinery...

Most of the compenstation techniques discussed here can be used in
general feedback control systems.

Exception: pole-splitting is specific to transistor circuits

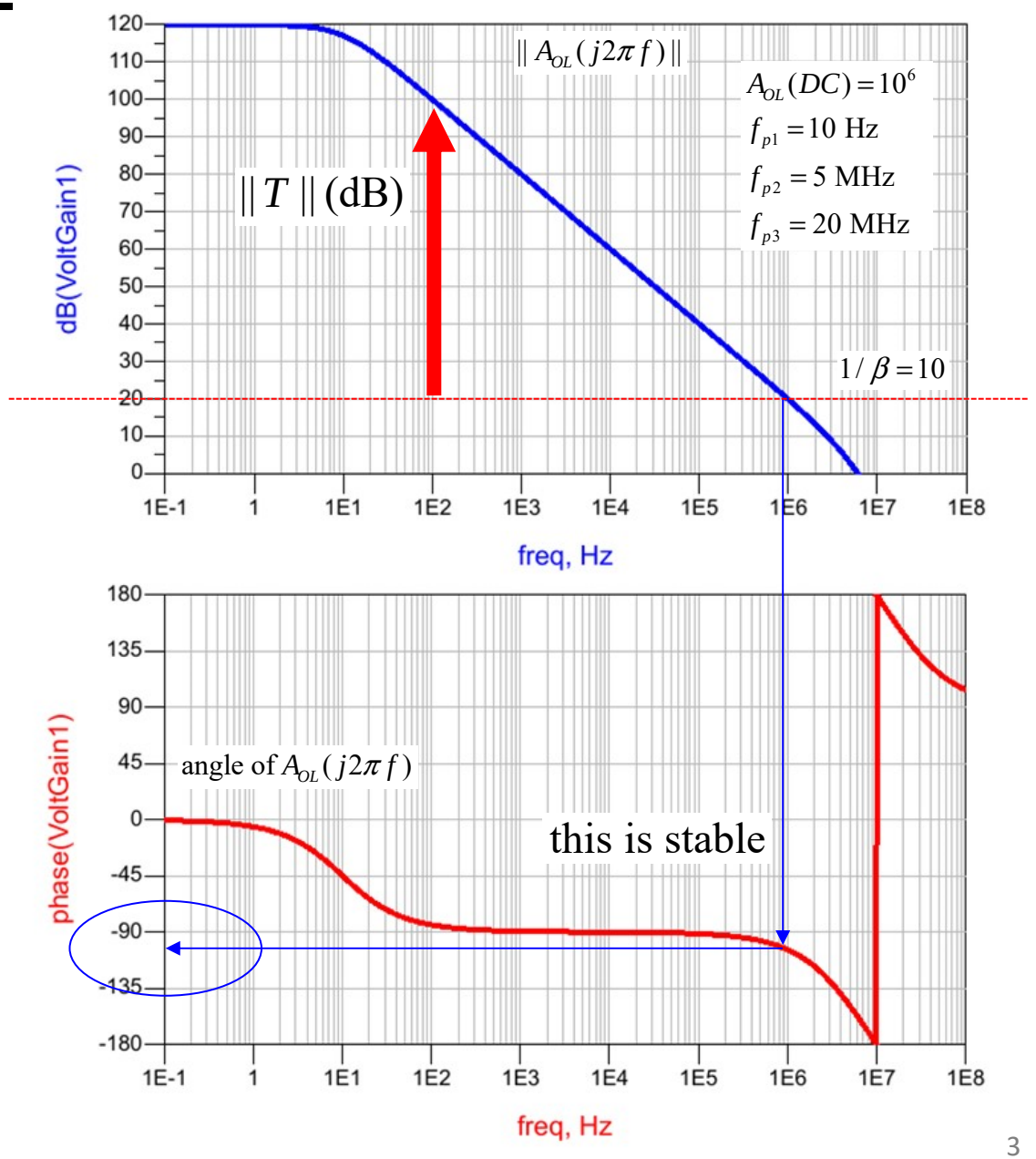
# One method of obtaining stability (1)

From the Bode criterion, once clear way to have adequate phase margin is for the 2nd, 3rd, and higher pole frequencies to all be well above $f_{loop}$, the loop bandwidth

This can be understood by recollecting that,
if the poles in $T(s)$ are real

$$\angle T(f_{loop}) = \arctan(f_{loop} / f_{z1}) + \arctan(f_{loop} / f_{z2}) + \ldots$$
$$- \arctan(f_{loop} / f_{p1}) - \arctan(f_{loop} / f_{p1}) - \ldots$$

So, if $f_{loop}$ is well below $f_{p2}$, $f_{p3}$,.... then each of these poles will contribute very little phase shift, while the term $-\arctan(f_{loop} / f_{p1})$ will contribute approximately $-90^0$ phase shift.



# One method of obtaining stability (2)

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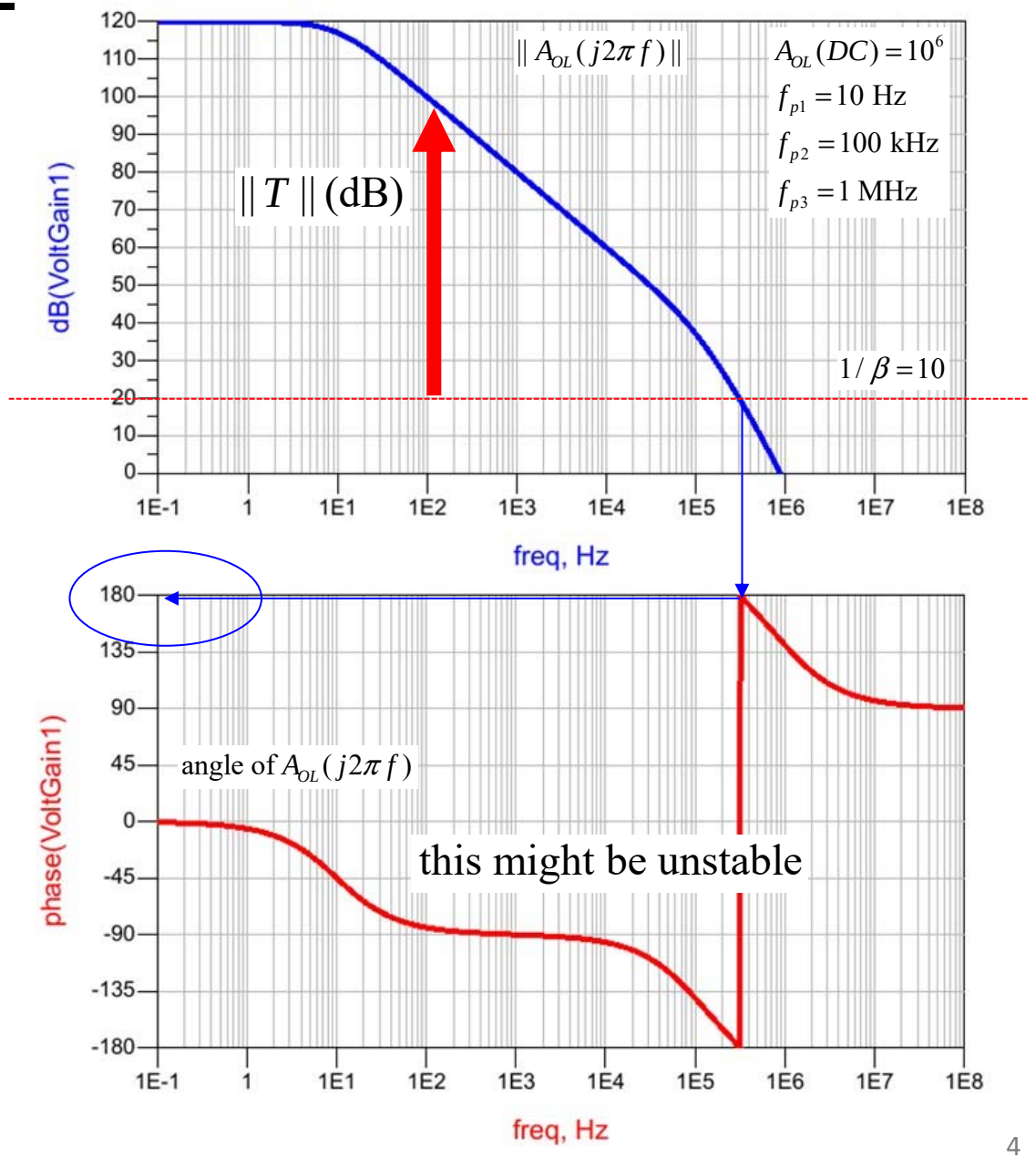
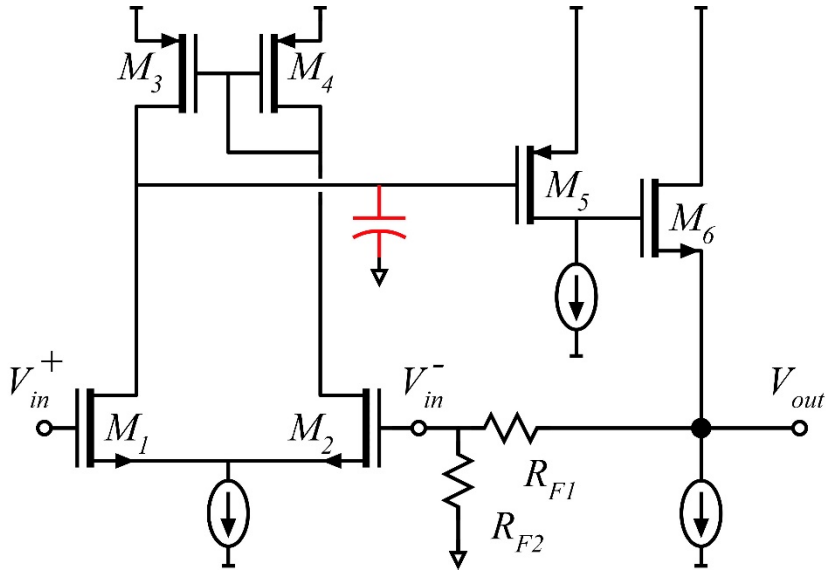


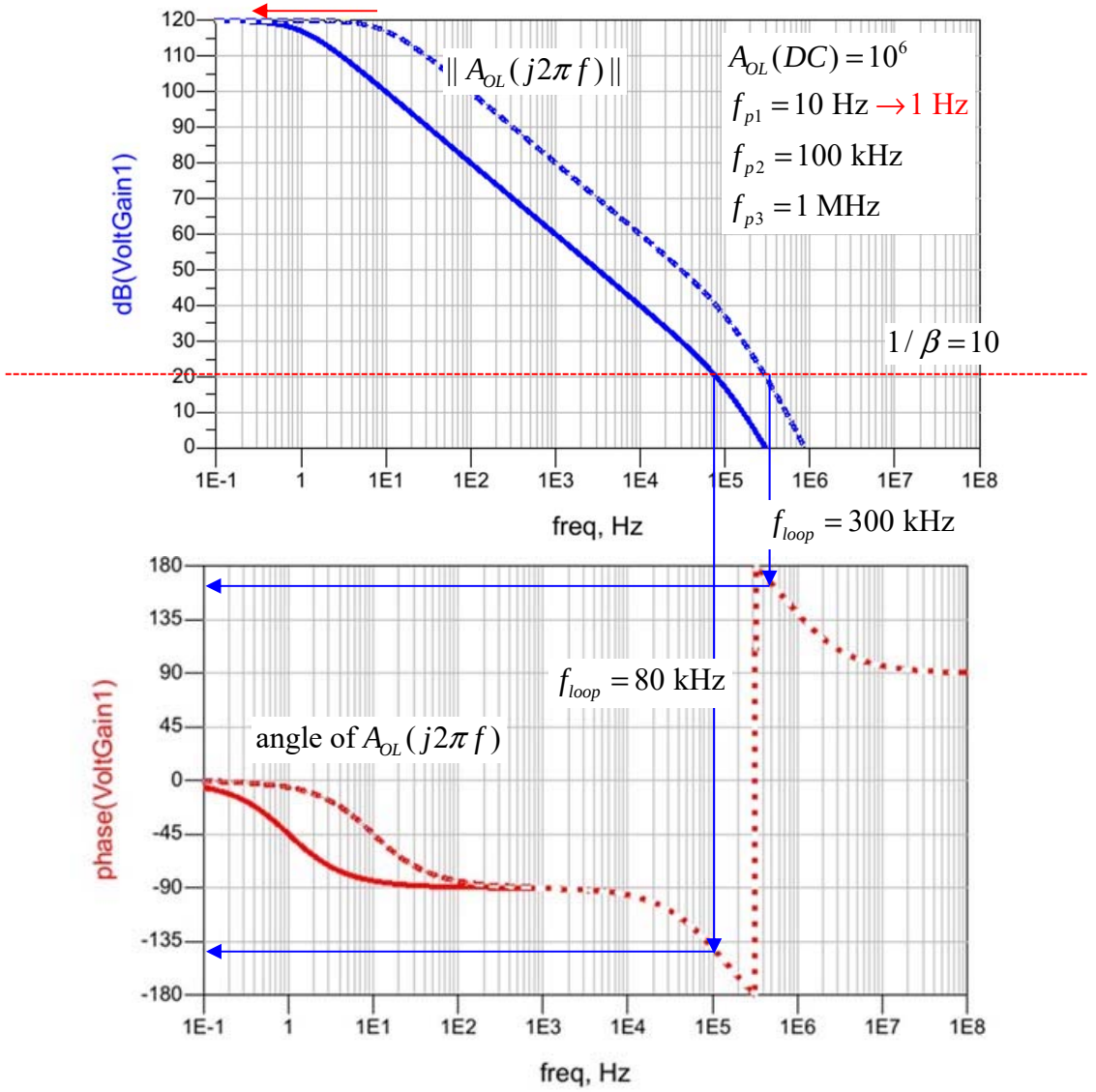
# Dominant pole compensation

Make $f_{p1}$ small enough that $f_{loop} = f_{p1}(1+T_0) << f_{p2}, f_{p3}, ....$

Then , at $f_{loop}$, the higher poles $f_{p2}, f_{p3}, ....$
will contribute very little phase shift,
while the first pole will contribute approximately -90$^0$ phase shift.

In the op-amp below, we do this by adding capacitance to the node that is already providing the lowest pole frequency $f_{p1}$.



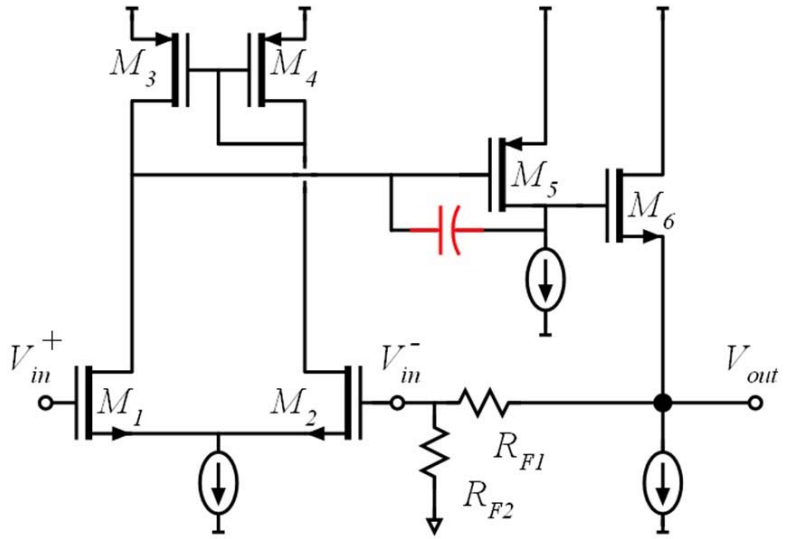



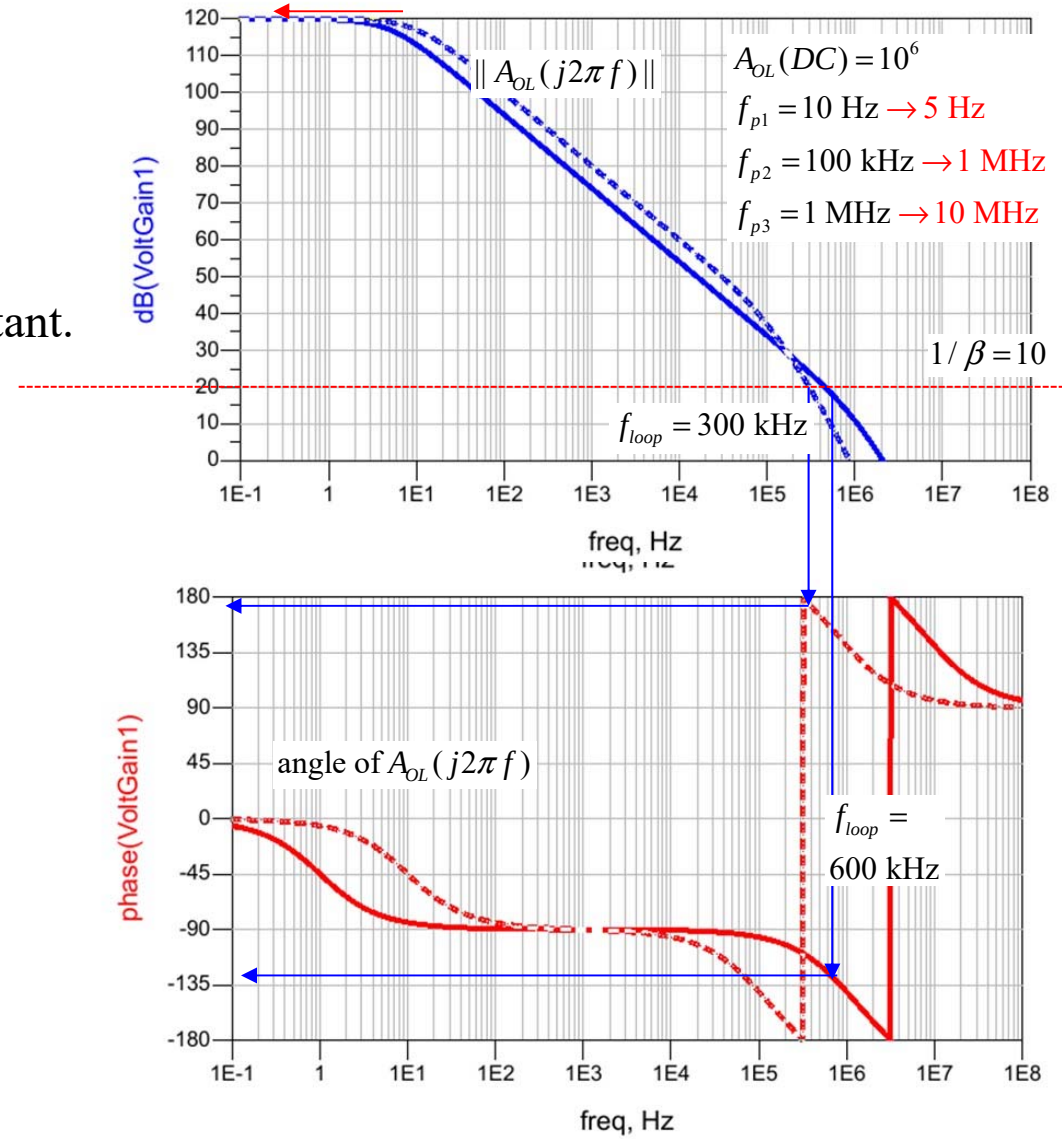
# Pole-splitting compensation (1)

We seek to make $f_{loop} < f_{p2}, f_{p3}, ....,$ so that the poles at $f_{p2}, f_{p3}$ don't contribute significant phase shift at $f_{loop}$.

If we could increase $f_{p2}, f_{p3}, ....,$ then we could not need to decrease $f_{p1}$ and $f_{loop}$ as much as would be needed if $f_{p2}, f_{p3}, ....,$ remained constant.

This can be done with a pole-splitting capacitor, as shown



# Pole-splitting compensation (2)

The common-source stage has

$$\frac{V_{D5}(s)}{I_i(s)} = \frac{V_{D5}}{I_i}\bigg|_{mid-band} \cdot \frac{1+b_1 s}{1+a_1 s+a_2 s^2}$$

where

$$a_1 = R_i C_{in} + R_{L,eq} C_{total} + R_{L,eq} C_L + R_i (1+g_m R_{L,eq}) C_{gd}$$

$$a_2 = R_i R_{Leq} \left( C_{gs} C_{total} + C_{gs} C_L + C_{total} C_L \right)$$

Where $C_{in}$ and $C_L$ include capacaitances from other transistors

Then, using the separated pole approximation:

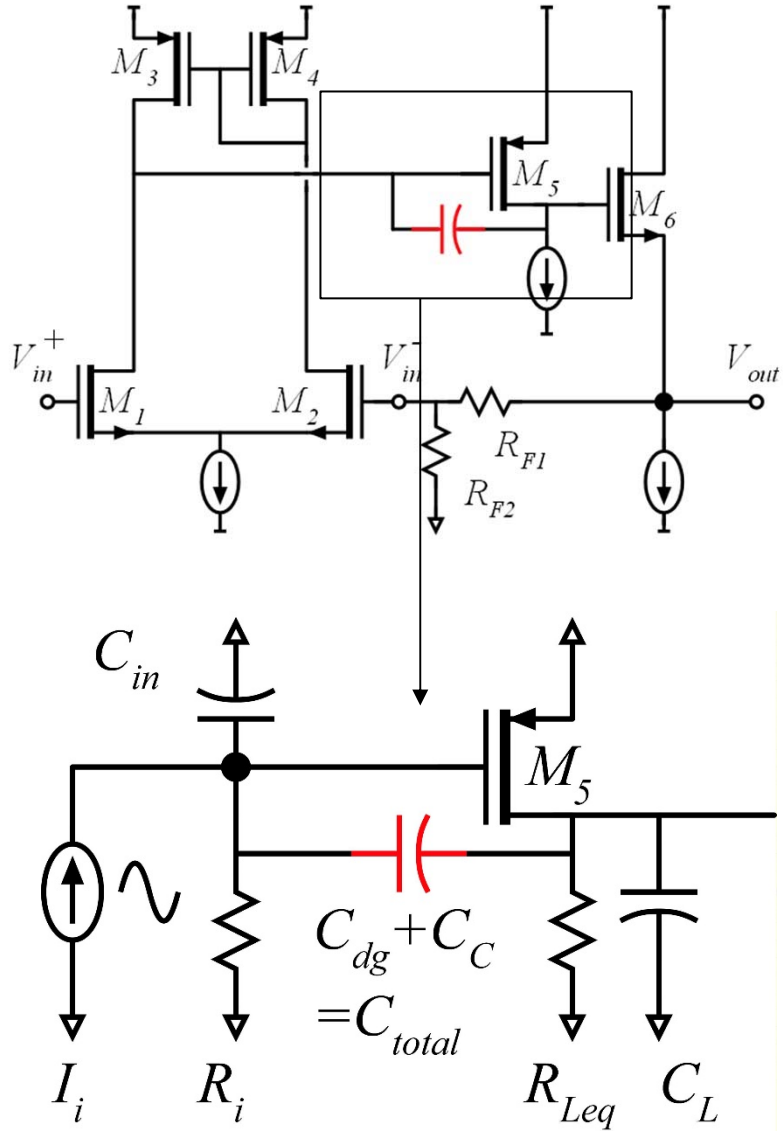
$$1/2\pi\, f_{p1} \cong a_1 = R_i C_{gs} + R_{L,eq} C_{gd} + R_{L,eq} C_L + R_i (1+g_m R_{L,eq}) C_{total}$$

$$1/2\pi\, f_{p2} \cong \frac{a_2}{a_1} = \frac{R_i R_{Leq} \left( C_{gs} C_{total} + C_{gs} C_L + C_{total} C_L \right)}{R_i C_{gs} + R_{L,eq} C_{total} + R_{L,eq} C_L + R_i (1+g_m R_{L,eq}) C_{total}}$$

As $C_{total}$ increases (and given that $g_m R_{L,eq} >> 1,\ g_m R_i >> 1$)

$$f_{p2} \rightarrow \frac{g_m}{2\pi (C_{gs} + C_L)}$$

The pole frequency associated with $C_L$ has increased.



# Pole-splitting compensation (3)

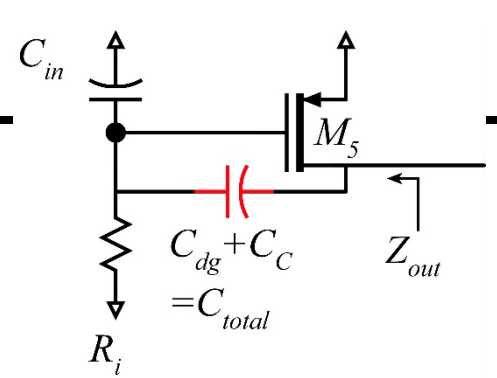
What, physically, is happening ?

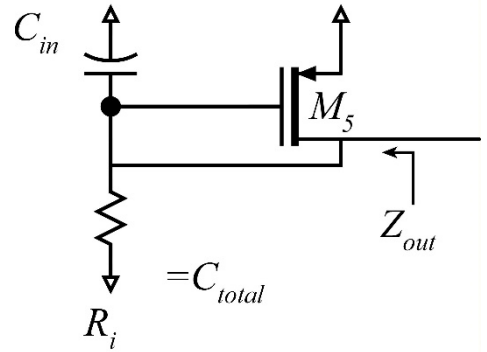
The amplifier has poles arising in part from the capacitances associated with $M_6$, together with $C_{DS5}$. These capacitances are charged through the output impedance of $M_5$.

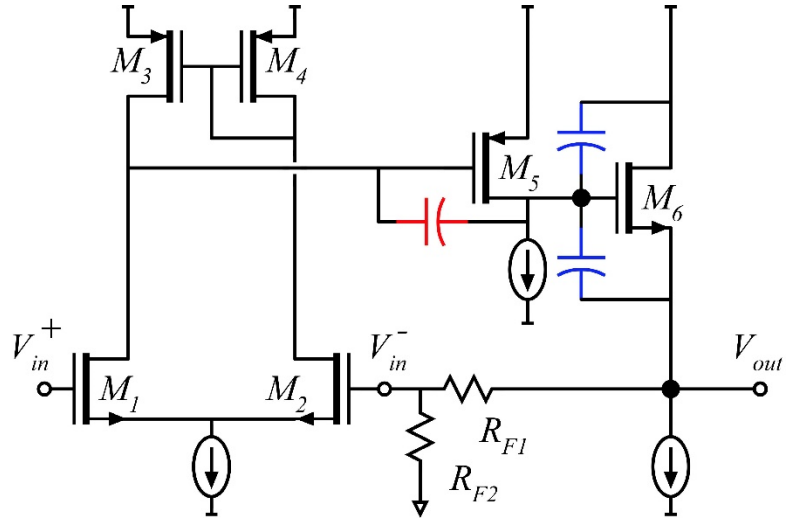
But, while $Z_{out5} = R_{DS5}$ at DC, as frequency increases, $(C_{dg5} + C_C)$ short-circuits together the gate and drain of $M5$. So, at high frequencies,

$$Z_{out5} = \left( R_{DS5} \,||\, R_i \,||\, \frac{1}{g_{m5}} \right) \cong 1/g_{m5}$$

Consequently, with a large $C_C$, we have one low pole frequency, but the pole associated with the output of $M_5$, and the poles associated with $M_6$, are driven to higher frequencies.



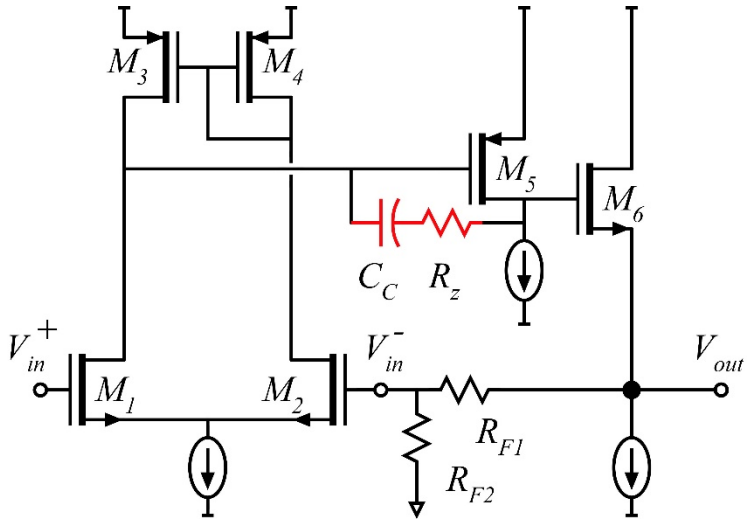
# Lead compensation in forward path

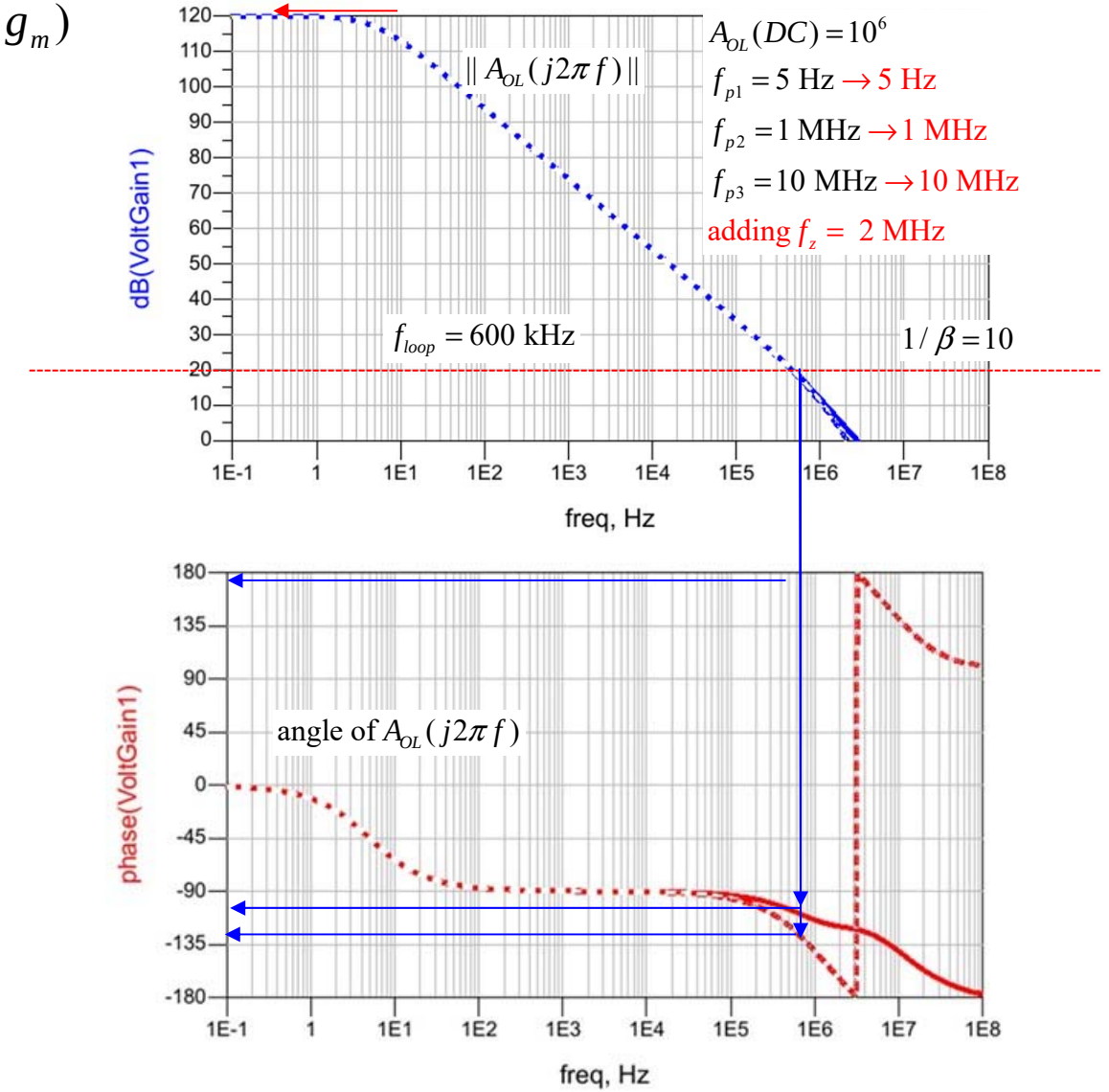
The resistor $R_z$ introduces a zero into $A_{OL}(s)$ with $s_{zero} = -1/C_C(R_z - 1/g_m)$

If $s_{zero}$ is negative (left half of $s$-plane) ,
then the zero adds postive phase shift.

We place $f_{zero}$ somewhat above $f_{loop}$.

Placing the zero carelessly can result in a large increase in $f_{loop}$, with consequent loop instability



# Lead compensation in feedback path (1)

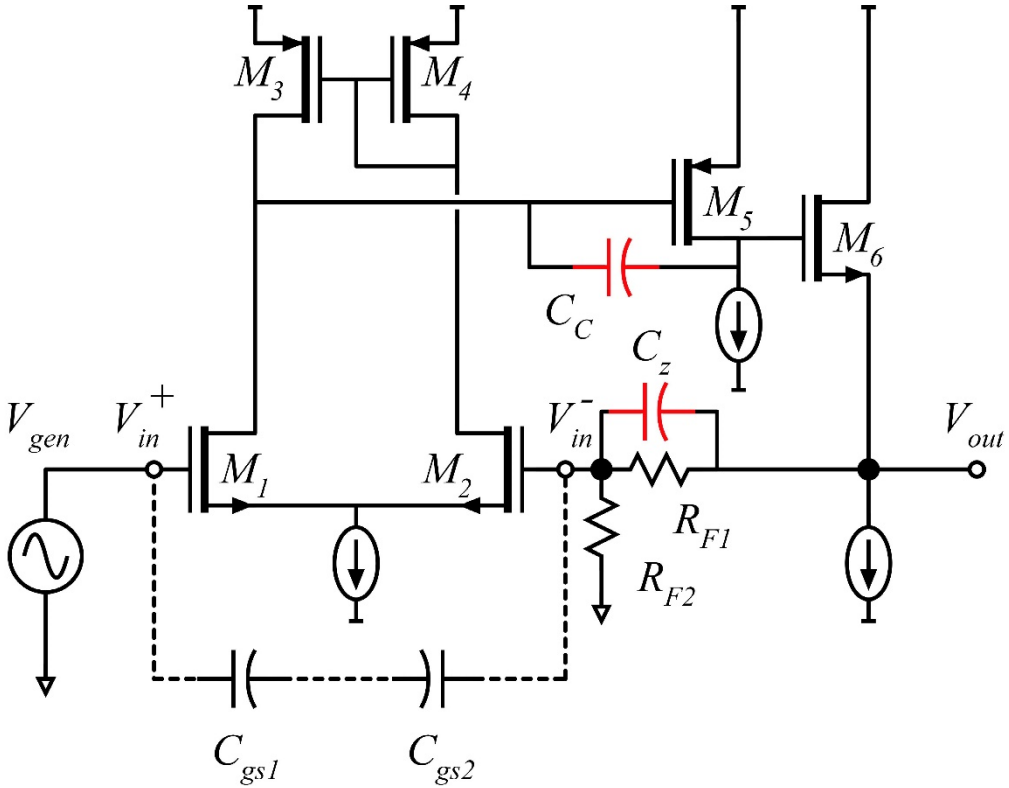
We can also introduce a zero into the feedback path $\beta(s)$ ,
using the capacitor $C_z$.

This will, however, force us to consider feedback theory more carefully.

We start with the relationship, valid (we will show later) if $Z_{out}$=0Ω :

$A_{CL}(s) = A_\infty \dfrac{T}{1+T}$ where $A_\infty$ is the gain if $V_{in}^+ = V_{in}^-$

and $T$ is the gain once around the loop



# Lead compensation in feedback path (2)

First find $A_\infty$ :

Use KCL at $V_{in}^-$

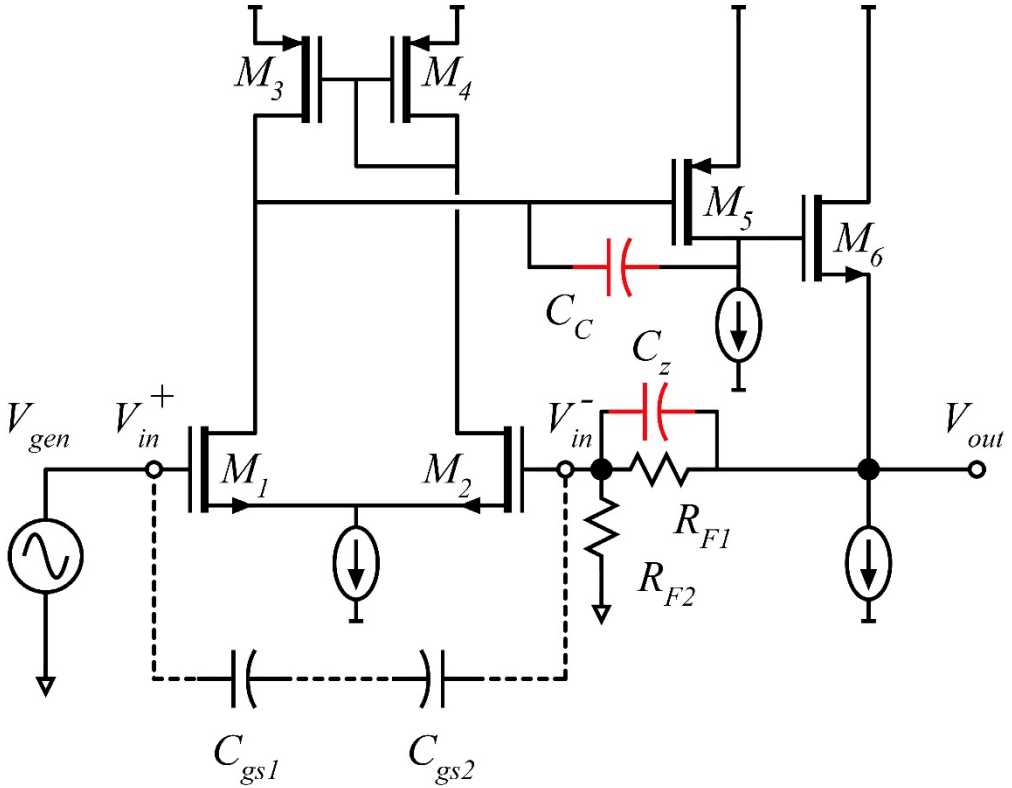
$$(V_{in}^- - V_{in}^+)sC_{gs1,2}/2 + V_{in}^- G_{F2} + (V_{in}^- - V_{out})(G_{F1} + sC_z) = 0$$

but $V_{in}^+ = V_{in}^- = V_{gen}$

$$V_{in}^+ G_{F2} + (V_{in}^+ - V_{out})(G_{F1} + sC_z) = 0$$

$$V_{gen}(G_{F1} + G_{F2} + sC_z) - V_{out}(G_{F1} + sC_z) = 0$$

$$\left.\frac{V_{out}}{V_{gen}}\right|_{\text{infinite op-amp gain}} = A_\infty = \frac{G_{F1} + G_{F2} + sC_z}{G_{F1} + sC_z} = \frac{R_{F1} + R_{F2}}{R_{F2}} \frac{1 + sC_z(R_{F1} \| R_{F2})}{1 + sC_z R_{F1}}$$



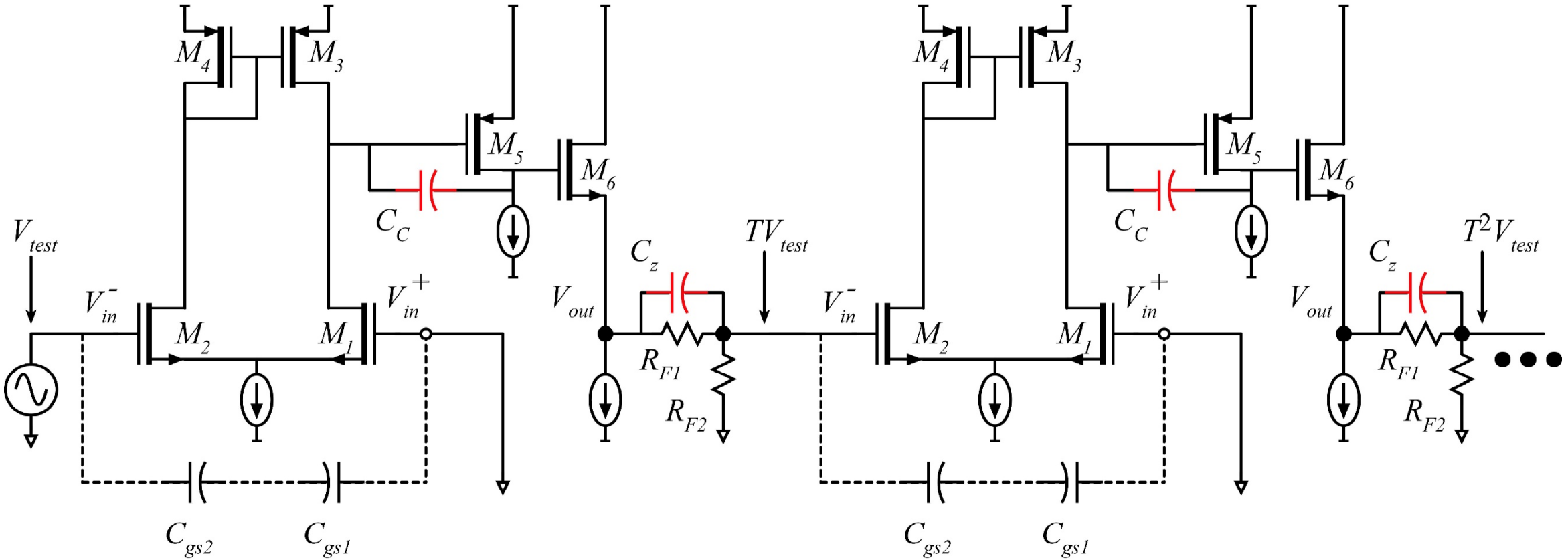

So, the frequency-dependent feedback has added a pole-zero pair to $A_\infty$.

# Lead compensation in feedback path (3)

Now find $T(s)$:

To do this, we *unwrap* the feedback loop, replacing it with an infinite chain of forward gain ($A_{OL}$) and feeback ($\beta$) elements. We insert a test voltage $V_{test}$, and compute the voltage that reaches the identical point after passing once through a forward gain ($A_{OL}$) element and once through a feeback ($\beta$) element. This keeps the loading impedance of each node unchanged.

(you will better avoid loading anomalies by comparing the points $TV_{test}$ and $T^2V_{test}$, but that requires more work).



# Lead compensation in feedback path (4)

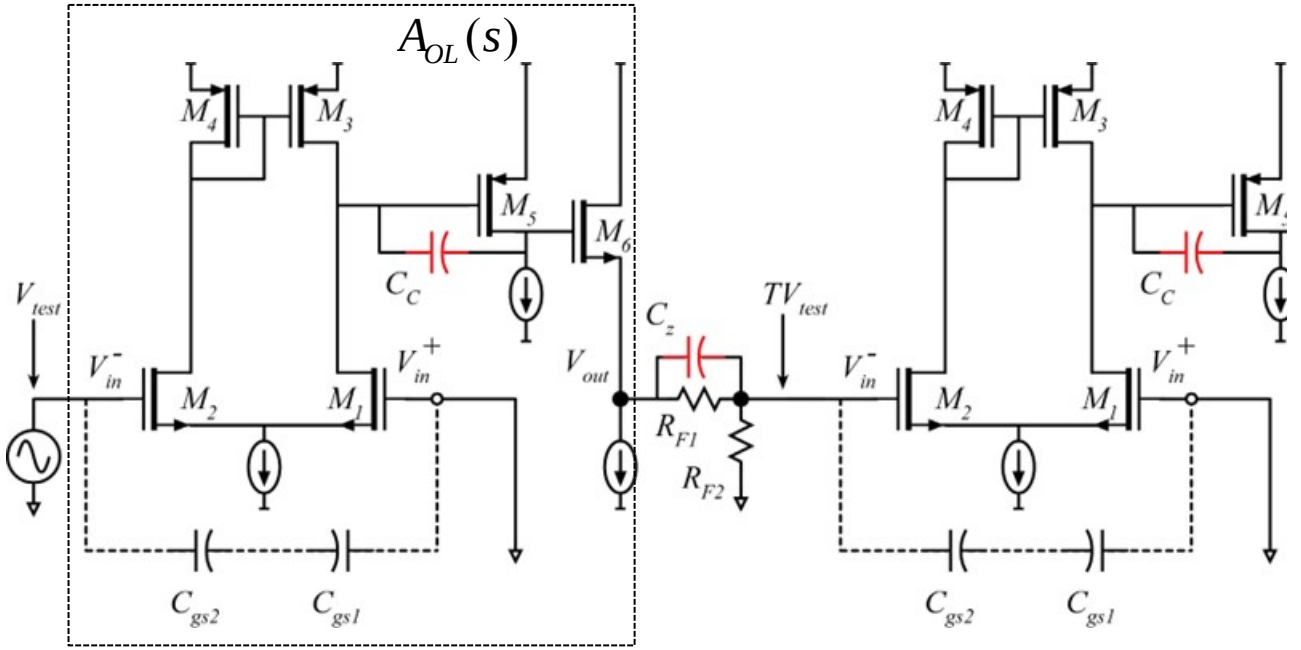
The loop transmission involves $A_{OL}(s)$,
including its poles, and the feedback network $\beta(s)$

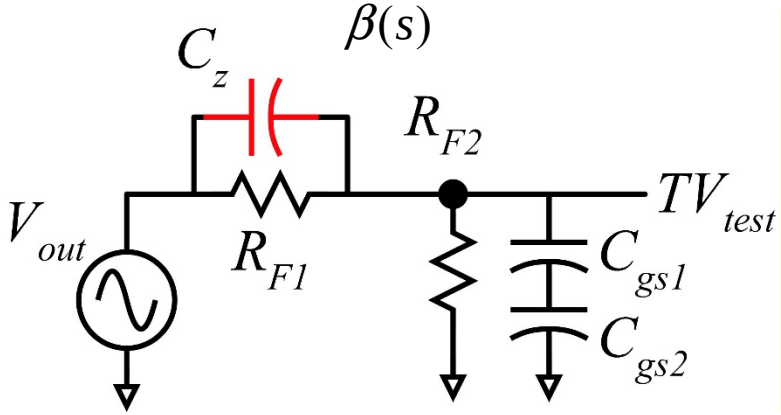
$\beta(s)$ involves a voltage divider between $R_{F2} \,||\, (C_{gs1,2}/2)$
and $R_{F1} \,||\, C_z$.

$$\beta(s) = \frac{R_{F2}}{R_{F1}+R_{F2}} \frac{1+sR_{F1}C_z}{1+s(R_{F1} \,||\, R_{F2})(C_z+C_{gs1,2}/2)}$$

$$T(s) = A_{OL}(s)\beta(s) = A_{OL}(s) \frac{R_{F2}}{R_{F1}+R_{F2}} \frac{1+sR_{F1}C_z}{1+s(R_{F1} \,||\, R_{F2})(C_z+C_{gs1,2}/2)}$$

We have introduced a zero ($s_z = -1/R_{F1}C_Z$) into $T(s)$, improving
the loop phase margin



# Lead compensation in feedback path (5)

$$A_{CL}(s) = A_\infty \frac{T(s)}{1+T(s)}$$

where

$$A_\infty = \frac{R_{F1}+R_{F2}}{R_{F2}} \frac{1+sC_z(R_{F1} \parallel R_{F2})}{1+sC_z R_{F1}}$$

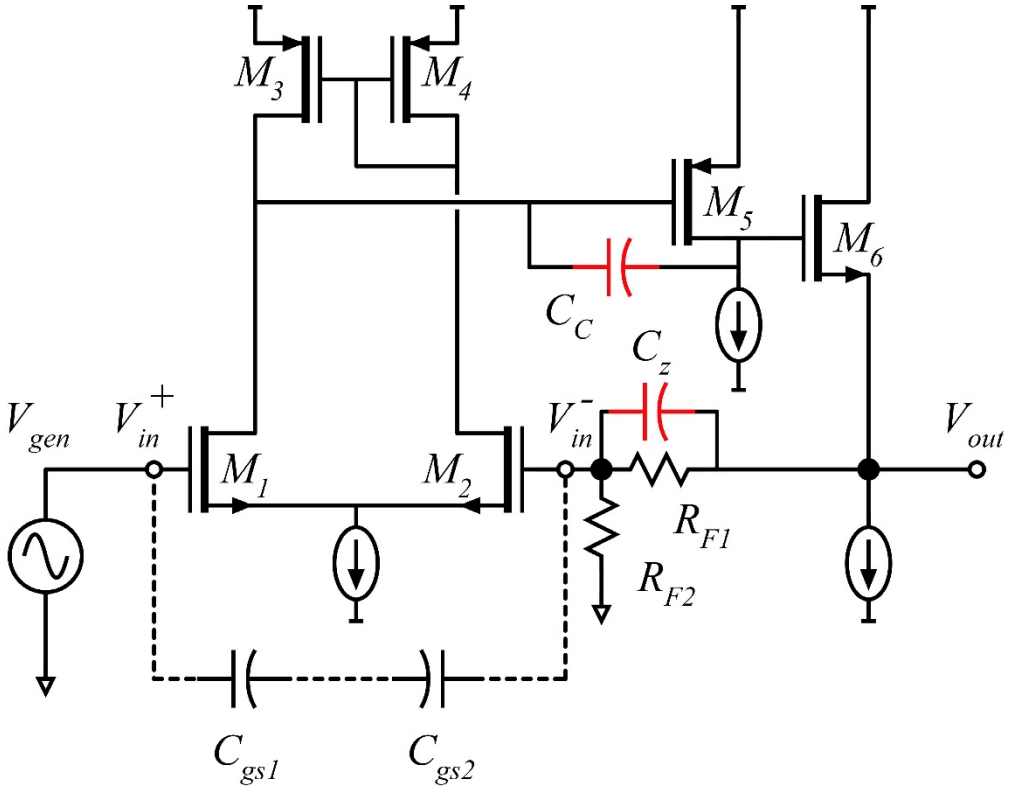
and

$$T(s) = A_{OL}(s)\beta(s) = A_{OL}(s) \frac{R_{F2}}{R_{F1}+R_{F2}} \frac{1+sR_{F1}C_z}{1+s(R_{F1} \parallel R_{F2})(C_z + C_{gs1,2}/2)}$$

The zero in the feedback path has

added a zero to $T(s)$, improving the phase margin,

but added a pole to $A_\infty$, which may or may not be desirable.




At higher frequencies, we have also added a pole to $T(s)$ and a zero to $A_\infty$.

Such feedback lead compensation is nevertheless very commonly used.

# Lag or Integral Compensation

We add a pole-zero pair to the amplifier while increasing its DC gain.

$A_{OL}(DC) = 10^6 \rightarrow 10^8$

$f_{p1} = 5\text{ Hz} \rightarrow 5\text{ Hz}$

$f_{p2} = 2\text{ MHz} \rightarrow 2\text{ MHz}$

$f_{p3} = 20\text{ MHz} \rightarrow 20\text{ MHz}$

added $f_{z1} = 100\text{ kHz}$

added $f_{p4} = 1\text{ kHz}$

Overall loop banwidth remains constant

Phase margin is decreased (not good)

Loop transmission, $T$, is greatly increased at low frequencies.

This provides greater loop precision, distortion suppression.