Switching circuits: basics and switching speed

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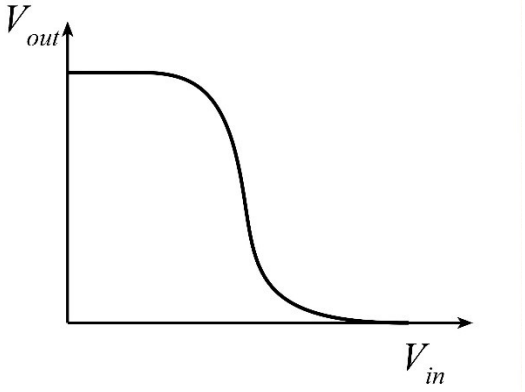
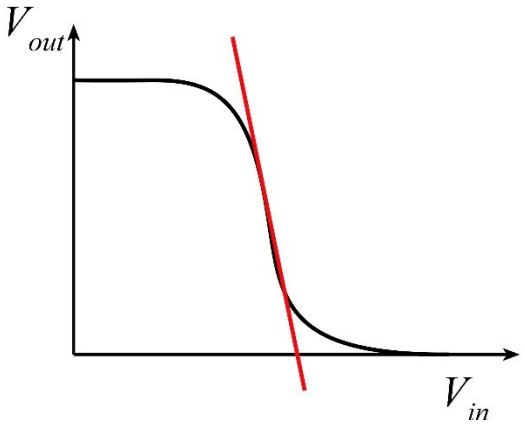
Amplifiers vs. switching circuits

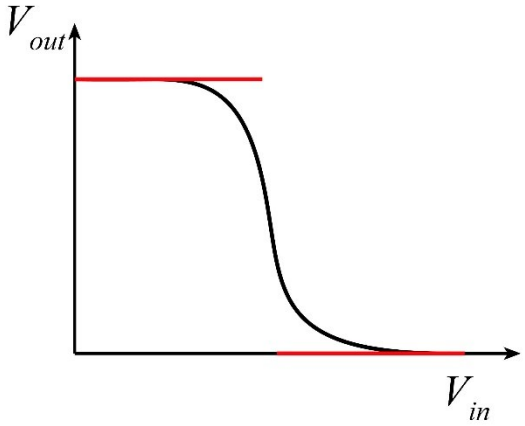
Some transistor circuit might have V_{in} vs. V_{out} characteristics like this:



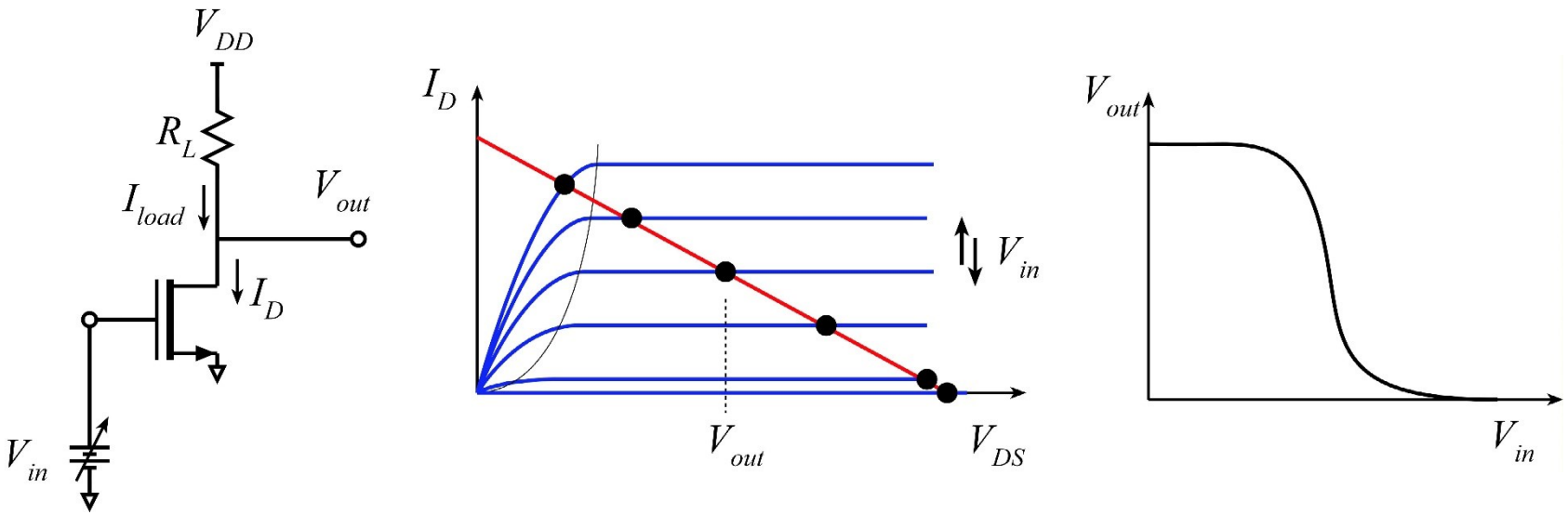
The characteristics have a nearly linear amplification region:



Plus limiting or clipping regions set by cutoff (minimum current) or "saturation" (minimum voltage)



Trivial example: CS stage with resistive load

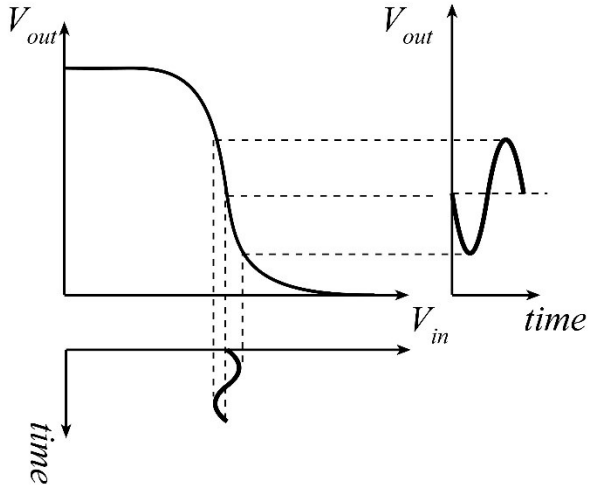


Here, the lower limit on V_{out} is set by saturation,

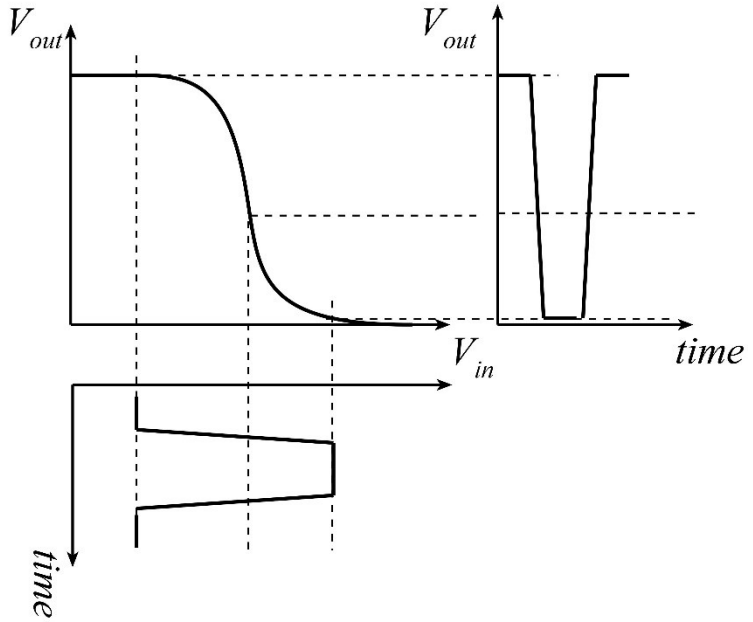
and the upper limit by cutoff

Amplifiers vs. switching circuits

Biased in the linear region,
and with a sufficiently small input,
the circuit is an *amplifier*



But, if the input is large, then the output switches between the clipping values.
This is a *switching circuit*

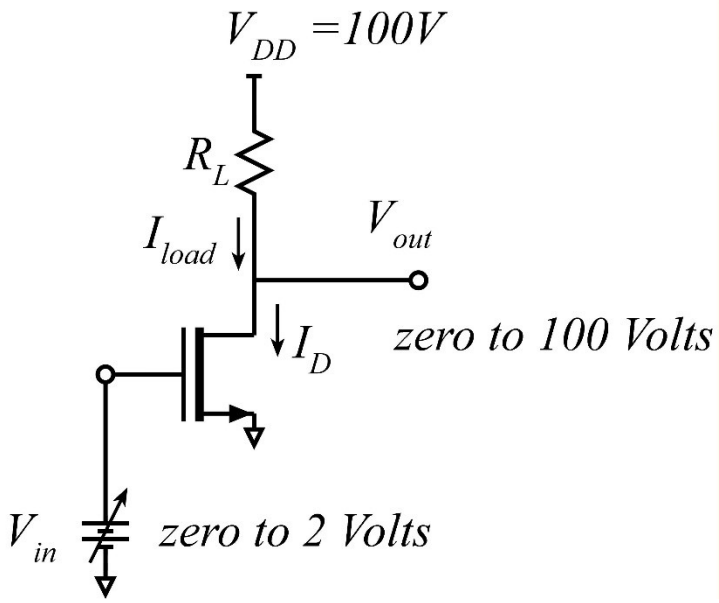


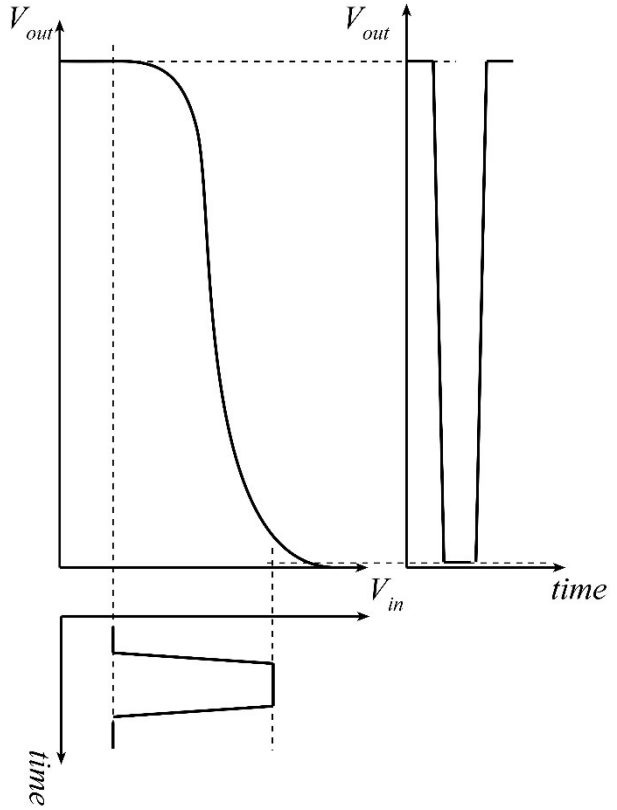
Switching circuits vs. logic gates

Logic gates are a particular *type* of switching circuit

A general switching cicuit might have a different range for V_{out} and V_{in}.

...and might not perform *logic*



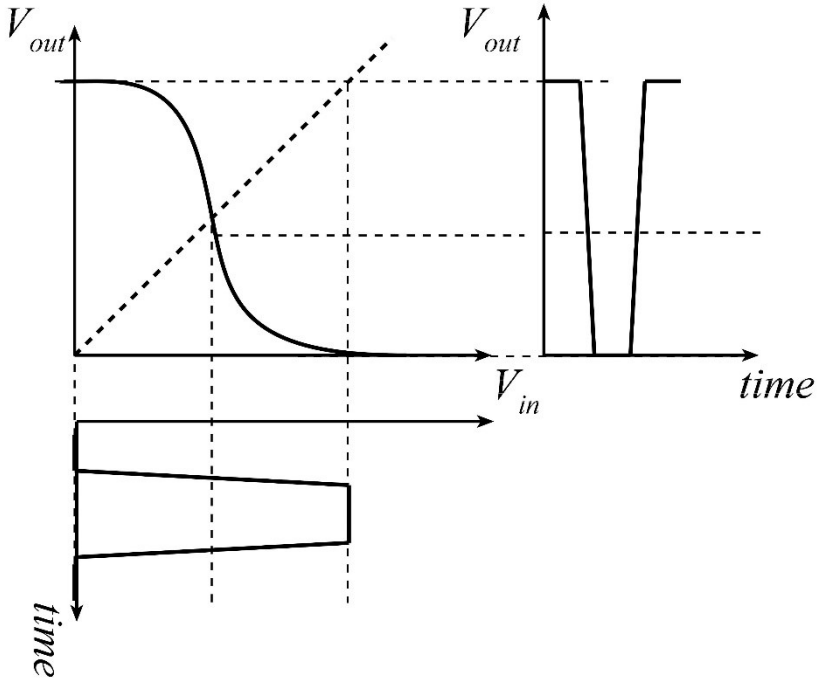


Switching circuits vs. logic gates

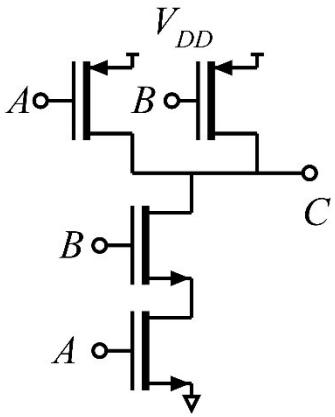
Logic gates are a particular *type* of switching circuit

A logic gate will have the same range for V_{out} and V_{in}.

...and usually has multiple inputs to perform Boolean operations



CMOS NAND gate:



Switching circuits vs. logic gates

Our focus here is on switching circuits, and on calculating

DC $V_{in} - V_{out}$ transfer characteristics

switching risetimes and falltimes

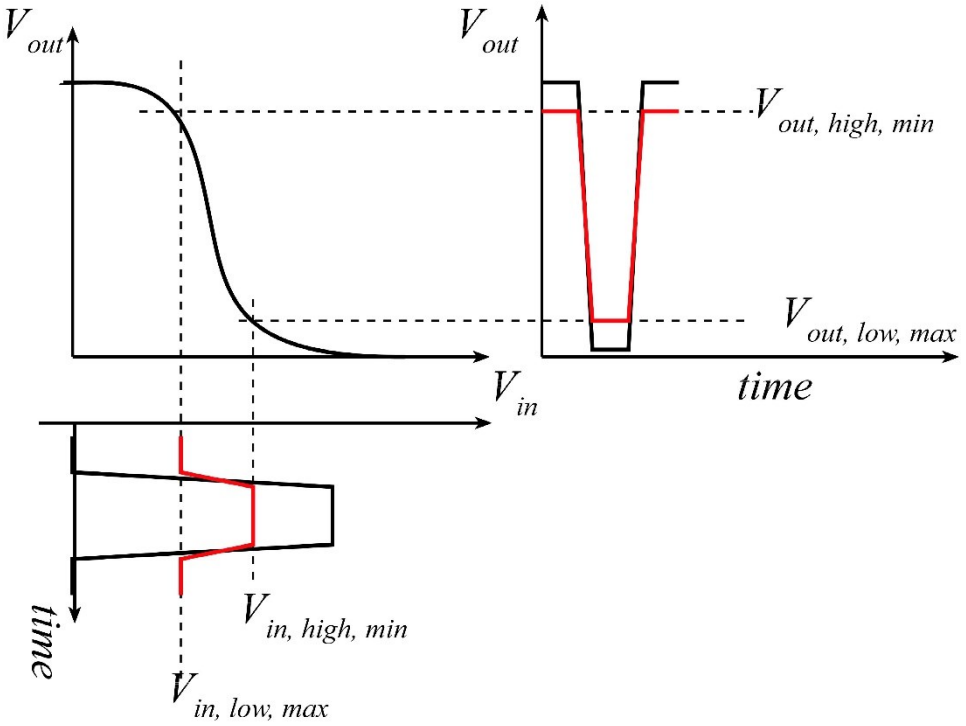
You should have , by now, studied basic logic gates

in other classes

Noise margins

"Noise" margins: tolerance for component variation, EMI

Input low level can vary over a considerable range, yet always produce nearly the same output "high" level

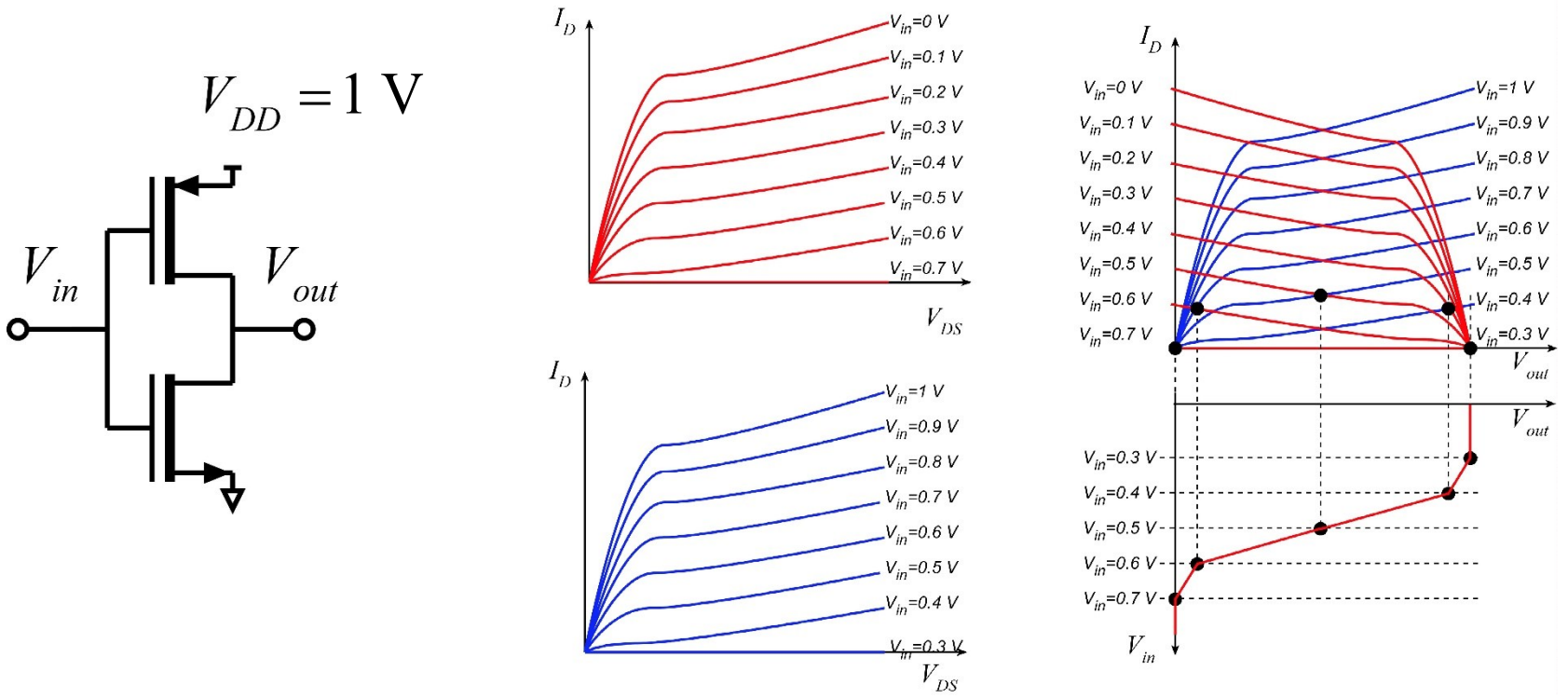


Input high level can vary over a considerable range, yet always produce nearly the same output "low" level

Defining margins precisely is difficult for general switching circuits.

....easier for logic

Another switching circuit: CMOS

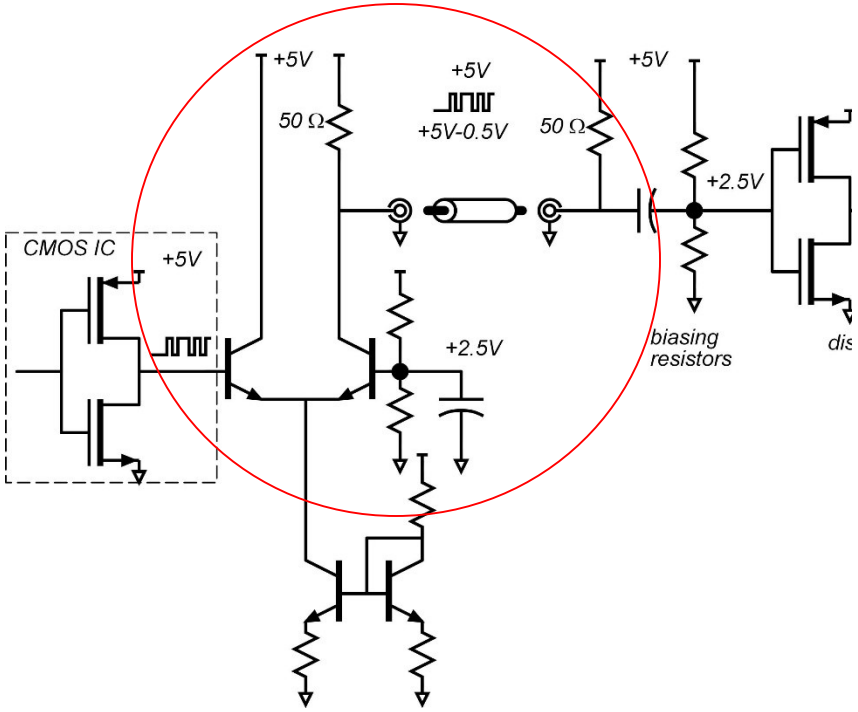


$I_{D,NFET} = I_{D,PFET}$ and $V_{DS,PFET} = V_{DD} - V_{DS,NFET}$

From these relationships, we obtain the loadline constructions above

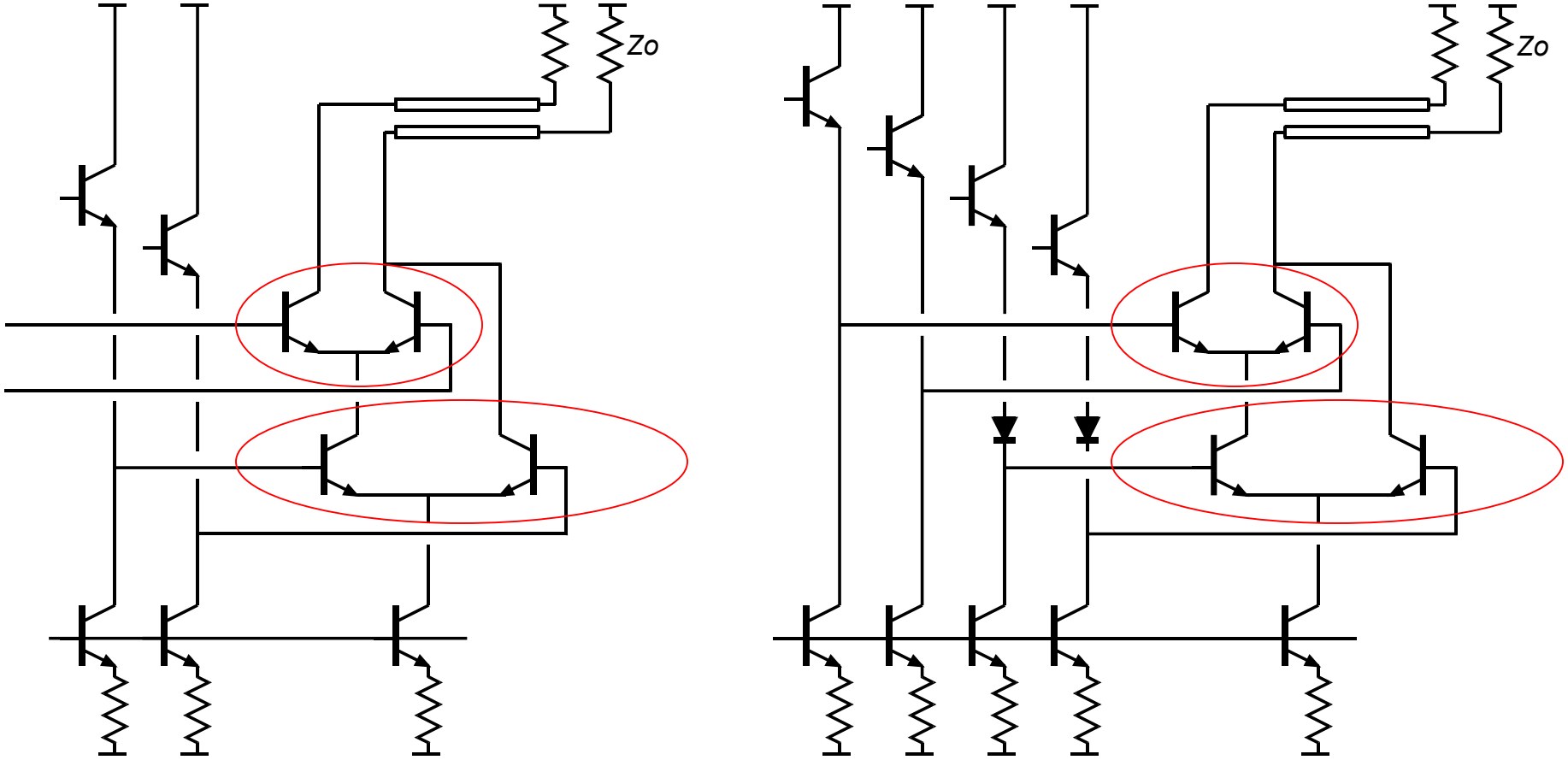
Both the positive and negative clipping limits, hence switched output voltage levels, are set by transistor saturation.

Another switch: emitter-coupled pair



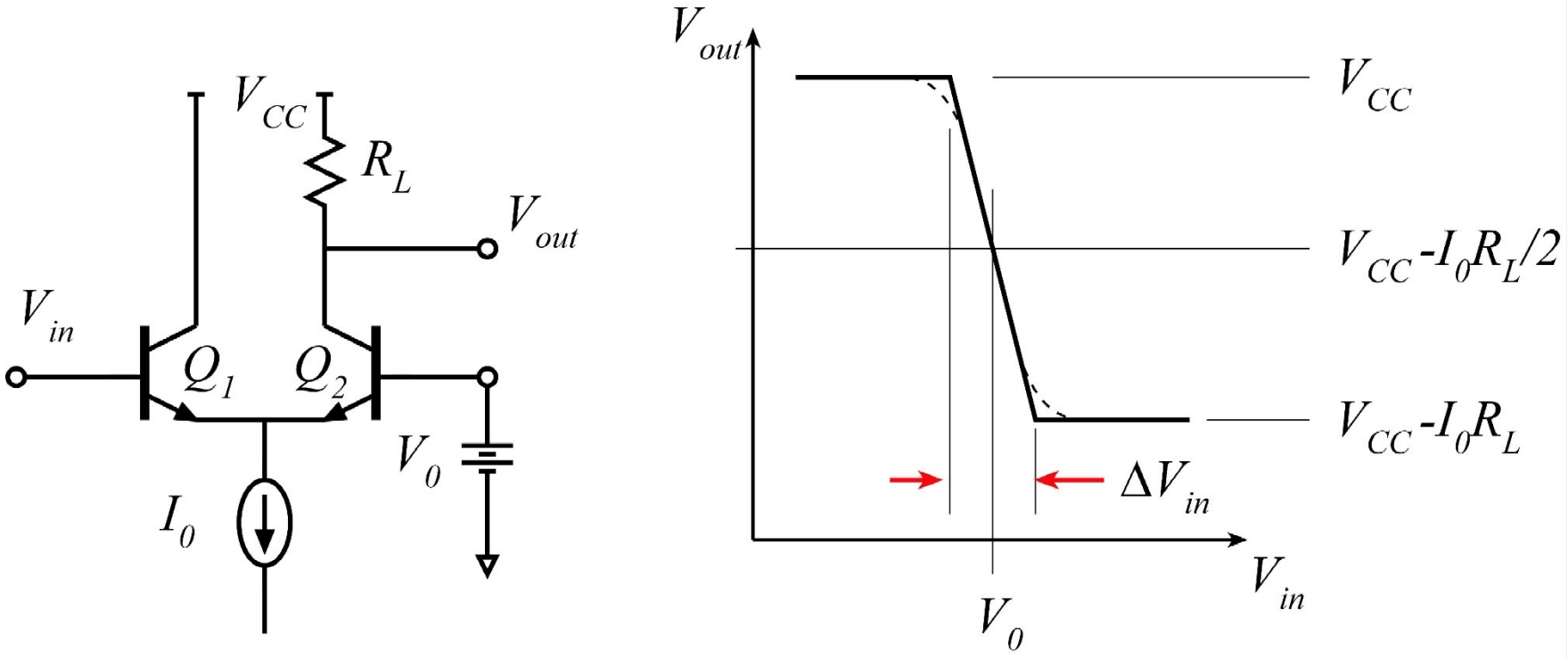
One example of this: the digital 50Ω coaxial cable interface between the PRBS pulse generator and the LED/laser driver in lab project choice #2.

Another switch: emitter-coupled pair



There are also logic families using bipolar differential pairs, current mode logic, left, and emitter coupled logic, right

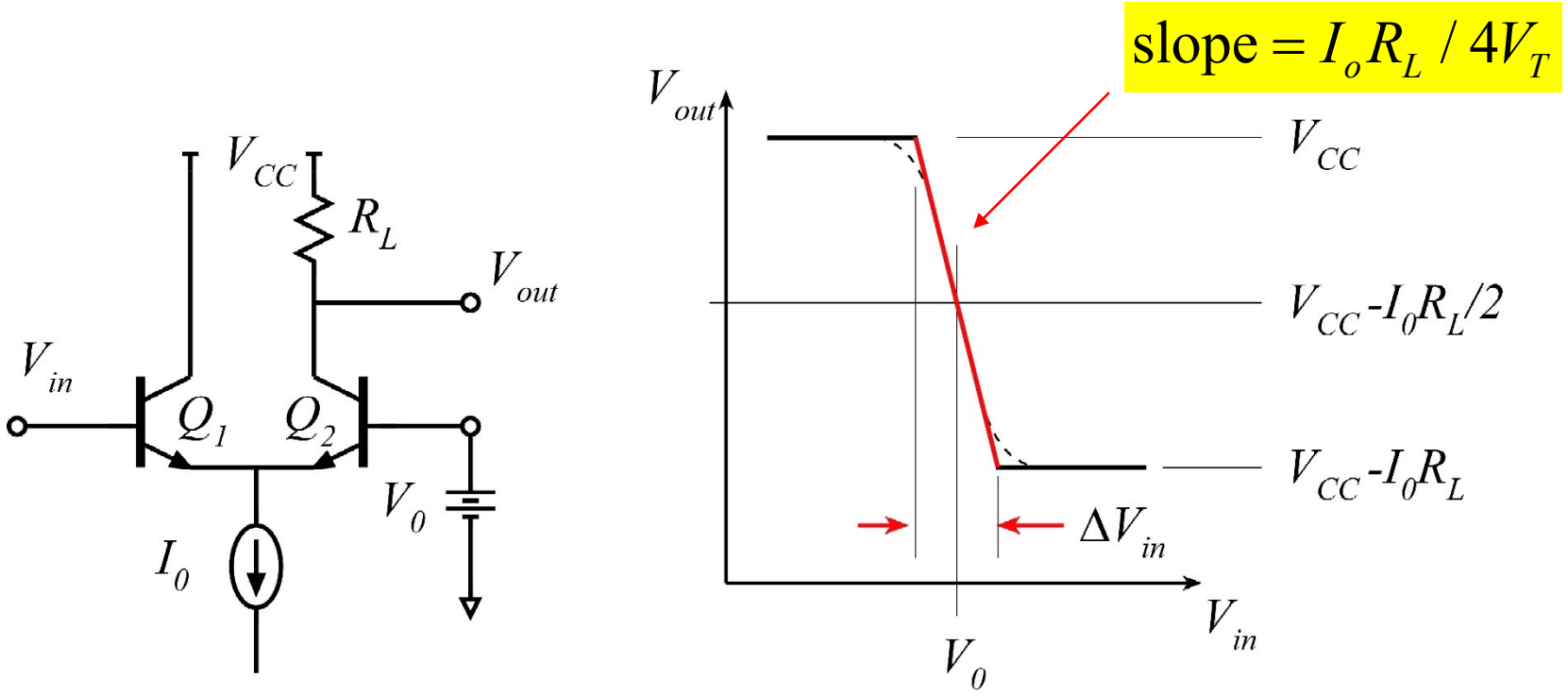
emitter-coupled pair transfer characteristics



The stated levels on the diagram are easily found.

But, how do we find ΔV_{in}?

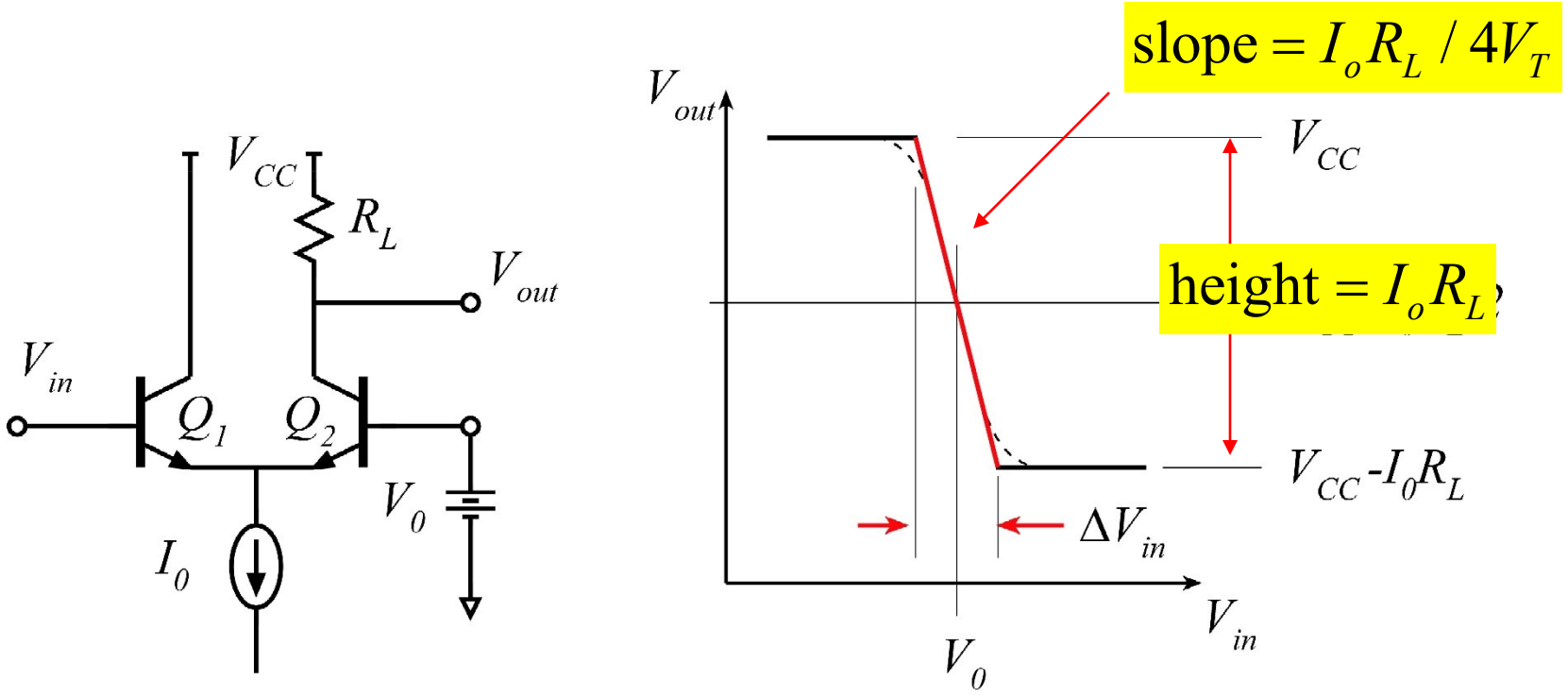
emitter-coupled pair transfer characteristics



DC bias V_{in} at zero Volts, then apply a small signal: what is the gain ?

$$g_m = g_{m1} = g_{m2} = I_o / 2V_T,\ A_v = \partial V_{out} / \partial V_{in} = g_m R_L / 2 = I_o R_L / 4V_T$$

emitter-coupled pair transfer characteristics



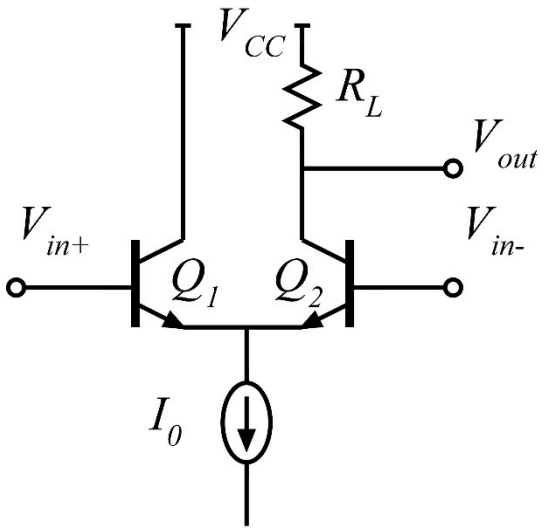
so, the slope of the switching region is $I_o R_L / 4V_T$,

while the output voltage swing is $I_o R_L$,

so the input voltage range must be the ratio of these:

$$\Delta V_{in} = (I_o R_L) / (I_o R_L / 4V_T) = 4V_T = 4kT / q$$

emitter-coupled pair: comments

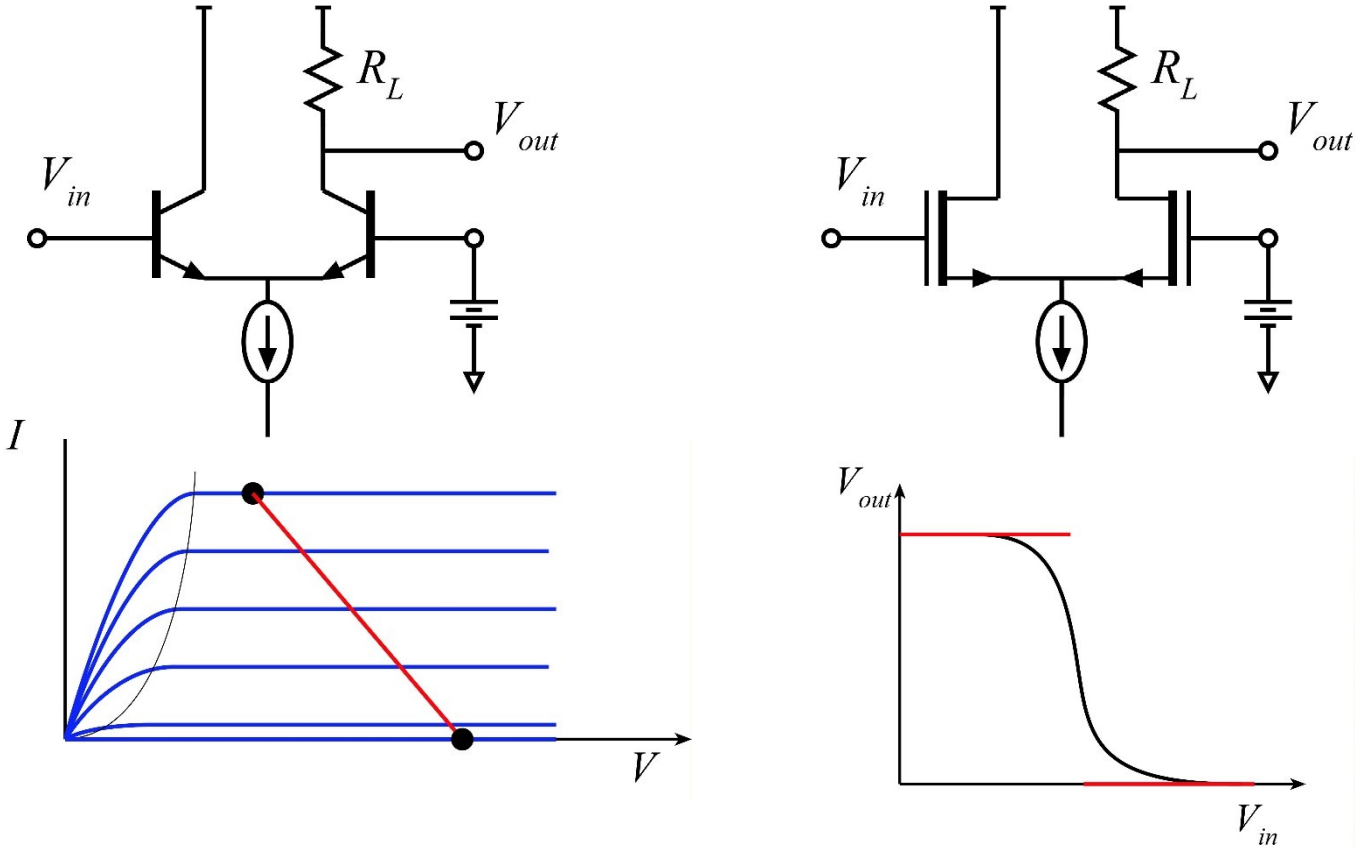


You can repeat this calculation for a differential input $\rightarrow$ different ΔV_{in}

We have assume that Q_1, Q_2 don't saturate over the logic swing.

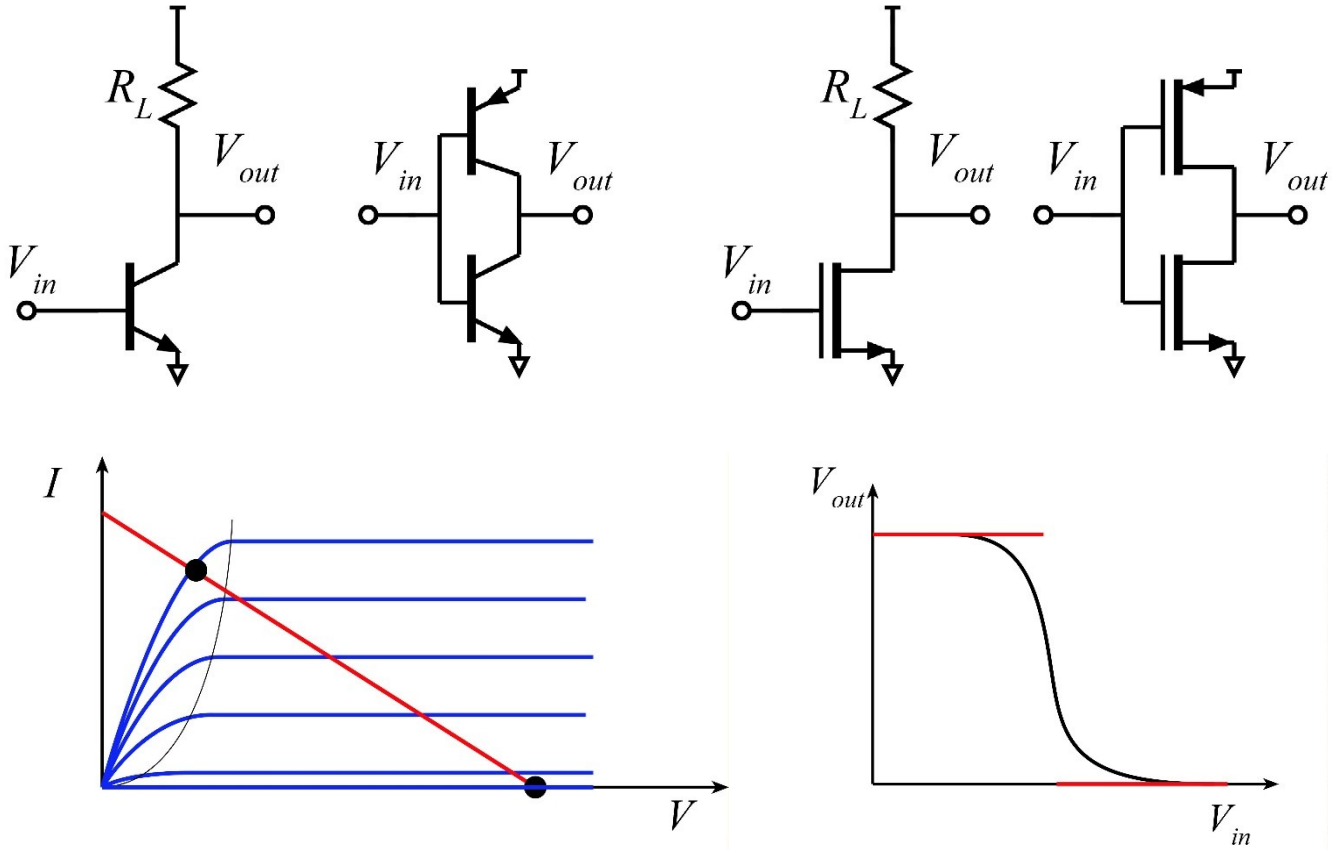
if they do, then this will change the $V_{in} - V_{out}$ characteristics

Limiting mechanisms: current-steering



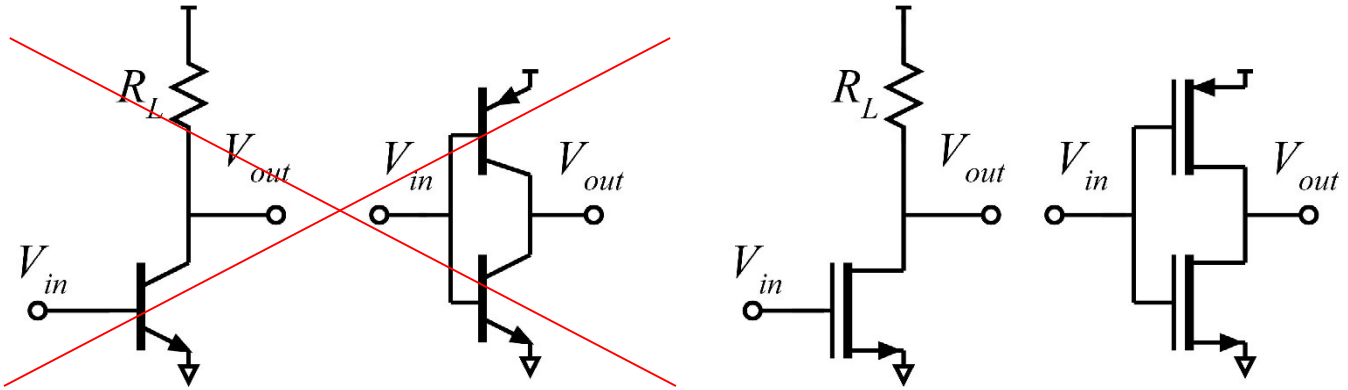
We can design differential current-steering circuits such that both $V_{out,high}$ and $V_{out,low}$ are set by cutoff.

Limiting mechanisms: CS or CE



In these common-source-like and common-emitter-like circuits either or both $V_{out,high}$ and $V_{out,low}$ are set by saturation.

Limiting mechanisms: CS or CE



When BJT's saturate,

they usually store large amounts of minority carrier change.

Switching speed is then very slow.

With a few exceptions,

saturation is avoided in bipolar switching circuits

Computing risetimes: charge control method

Charge control method: hand estimate switching circuit delay, risetime

-Compute total charge on all capacitors at high Q_{high} and low levels Q_{low}

-Compute voltage on node at high level V_{high} and low level V_{low}

-Compute change in charge $\Delta Q = Q_{high} - Q_{low}$ and voltage $\Delta V = V_{high} - V_{low}$

-If node is charged by constant current I, then charging is linear

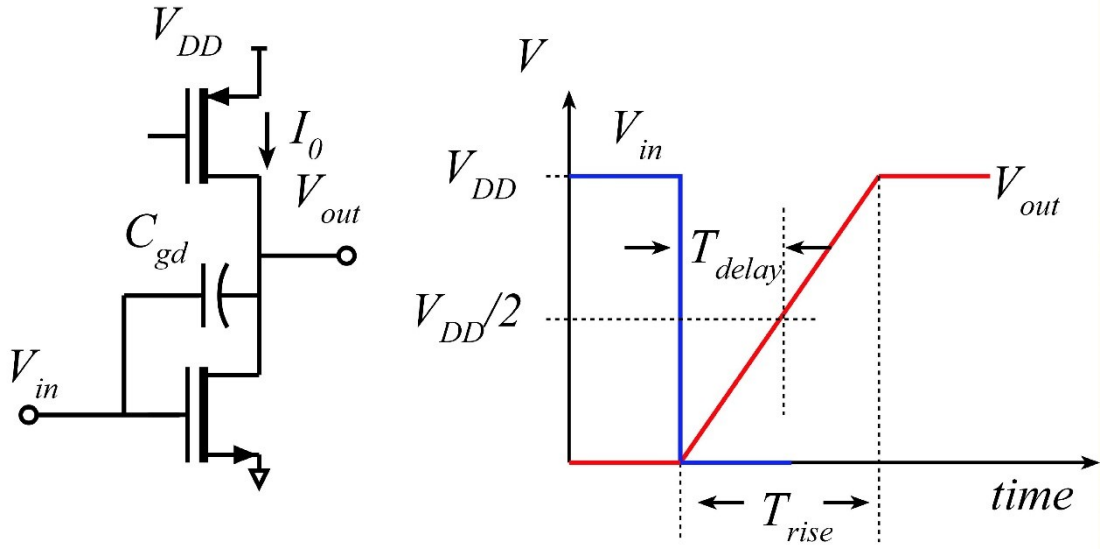
$$T_{rise/fall} = \Delta Q / I \text{ and } T_{delay} = T_{rise/fall} / 2$$

-If node is charged through resistance R, then charging is exponential

Equivalent capacitance $C = \Delta Q / \Delta V$, time constant $\tau = RC$

$$T_{rise/fall} = 2.2\tau \text{ and } T_{delay} = \tau \ln(2)$$

Charging through a current source



The input voltage falls suddenly, turning the FET off.

Let's ignore, just for now,

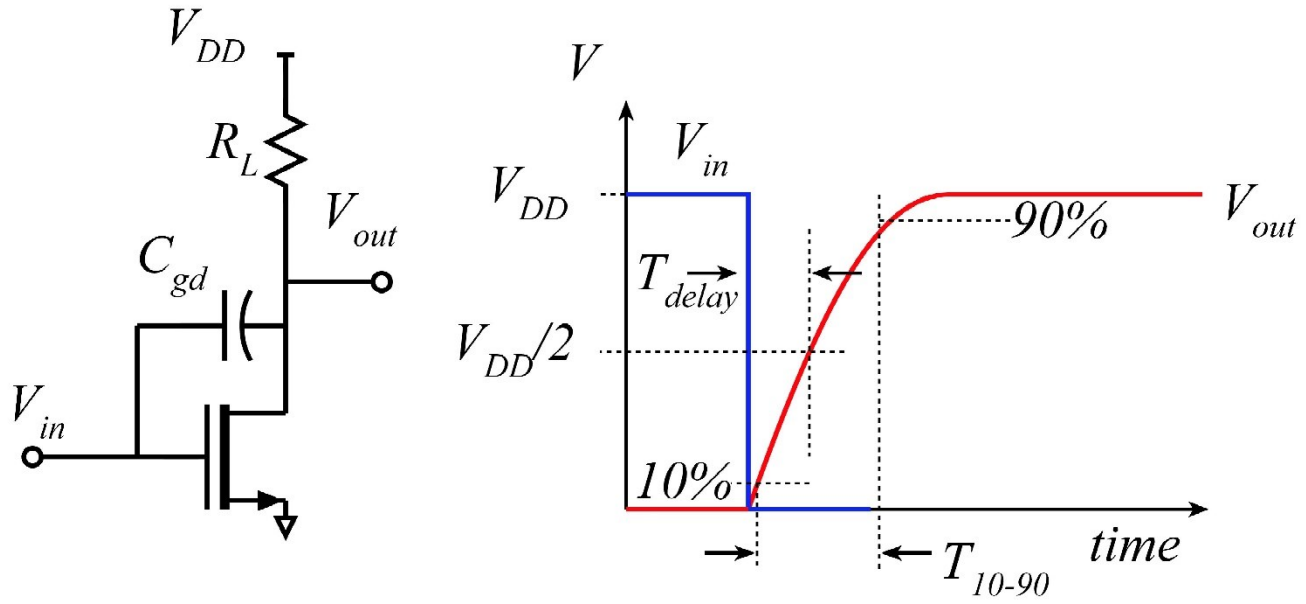
the PFET knee voltage; treat as current source.

Now, constant current charges capacitance.

Charging is linear

$$T_{rise/\,fall} = \Delta Q / I_0 \text{ and } T_{delay} = T_{rise/\,fall} / 2$$

Charging through a resistance



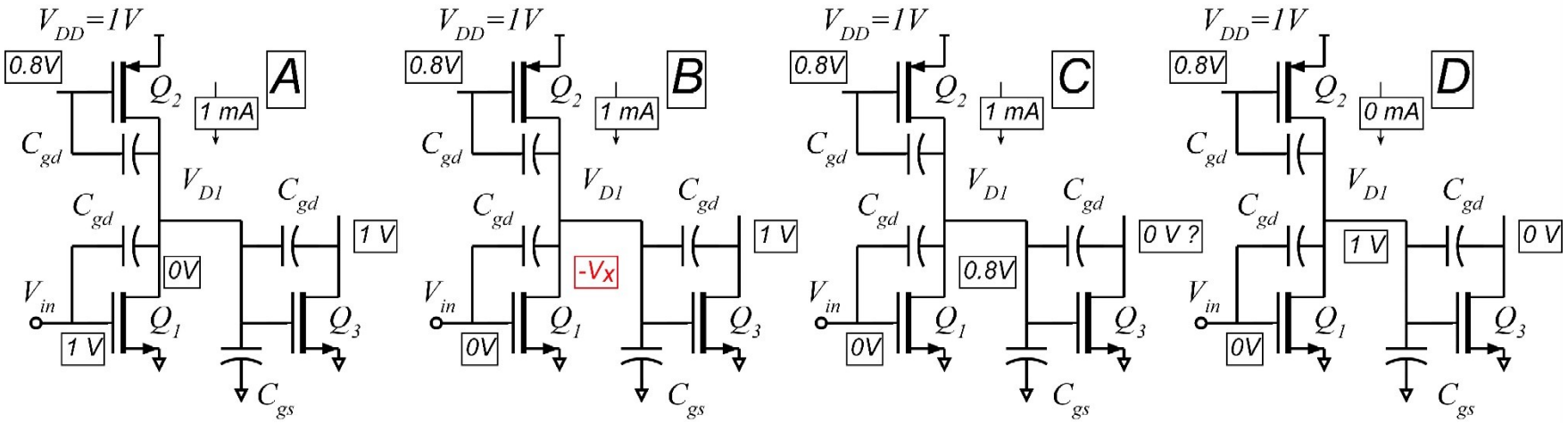
The input voltage falls suddenly, turning the FET off.

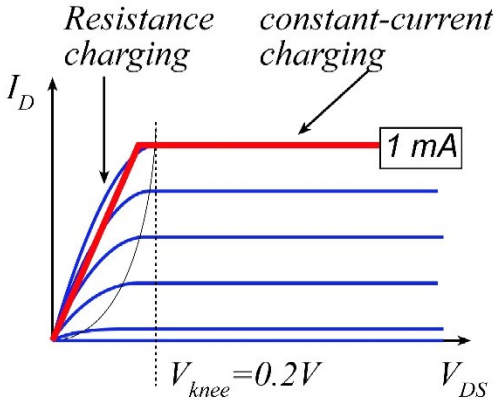
Node is charged through resistance R; charging is exponential

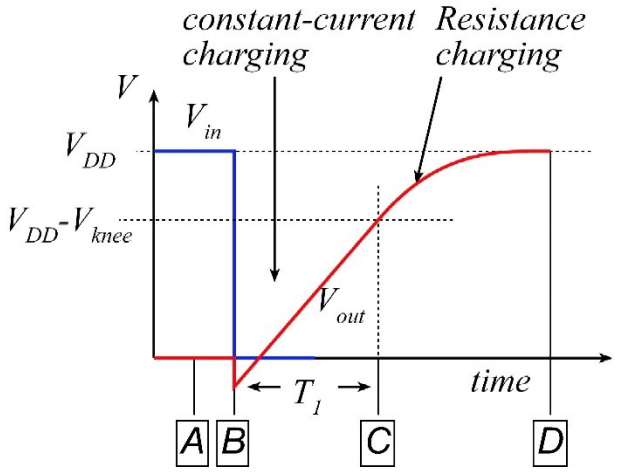
Equivalent capacitance $C = \Delta Q / \Delta V$, time constant $\tau = RC$

$T_{rise/fall} = 2.2\tau$ and $T_{delay} = \tau \ln(2)$

Example: Waveform at Q1 drain



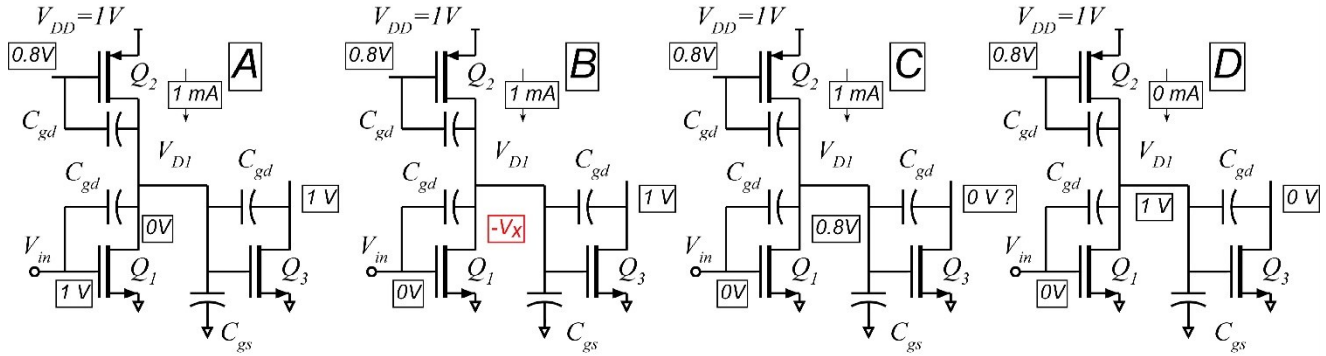


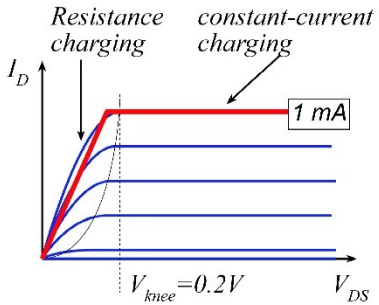


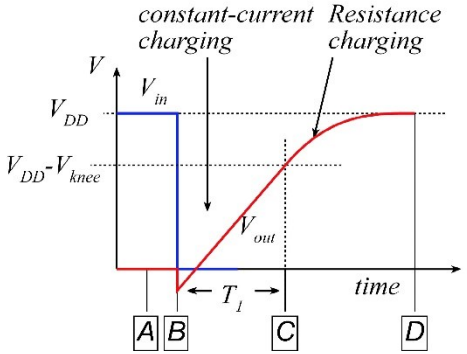
V_{in} switches at $t = 0$.

We will estimate $V_{D1}(t)$.

Example: Waveform at Q1 drain







Note:

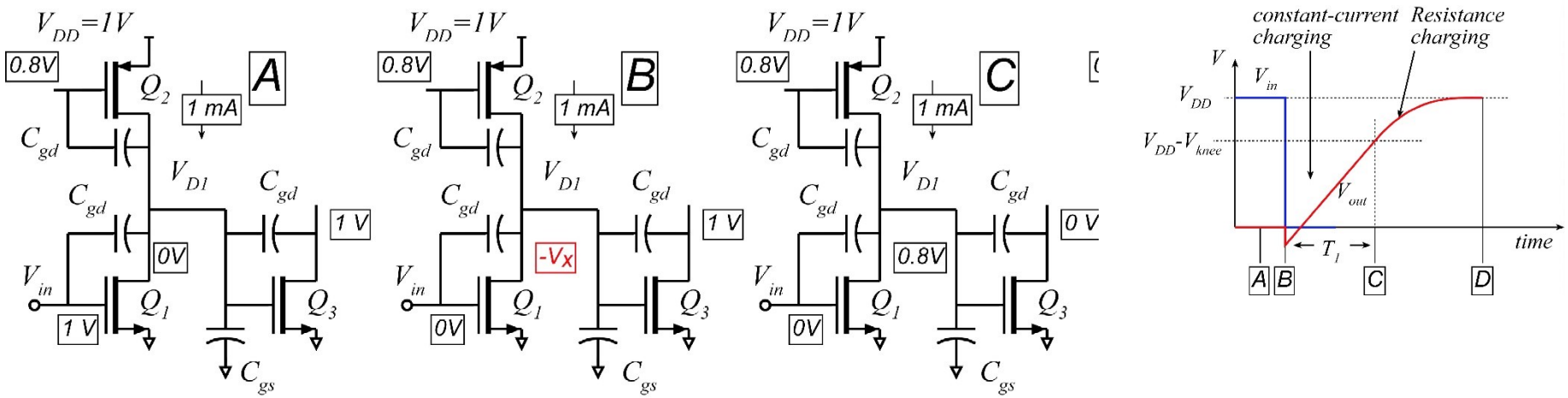
1) $V_{D1}(t)$ initially swings negative: $V_{in}(t)$ couples to $V_{D1}(t)$ though a capacitive voltage divider between C_{gd1} and $(C_{gd2}, C_{gd3}, C_{gs3})$

2)$V_{D1}(t)$ then charges towards +1V.

Between V_{D1}= 0V and 0.8V, Q_2 is a constant-current source

Between V_{D2}= 0.8V and 1V, Q_2 acts as a resistance (saturation)

Example: Waveform at Q1 drain



Switching time between A and C: 1st part: charging to 0.8V

change in charge in:

C_{gd1}: @ A: $Q = -1\text{V} \cdot C_{gd1}$, @ C: $Q = 0.8\text{V} \cdot C_{gd1}$, $\Delta Q = 1.8\text{V} \cdot C_{gd1}$

C_{gd2}: @ A: $Q = -0.8\text{V} \cdot C_{gd2}$, @ C: $Q = 0\text{V} \cdot C_{gd2}$, $\Delta Q = 0.8\text{V} \cdot C_{gd2}$

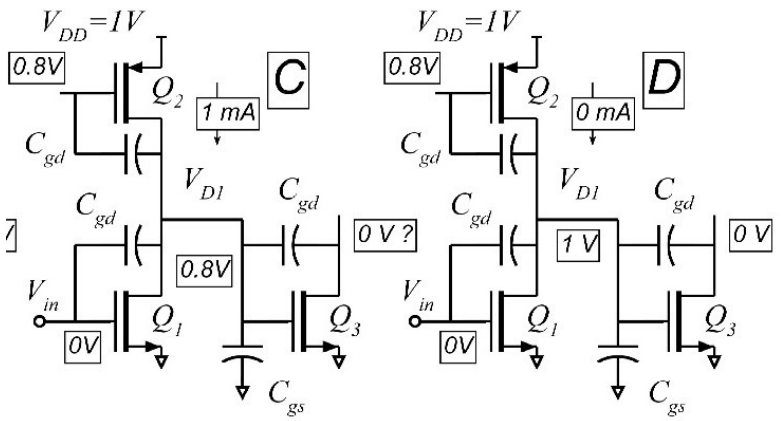
C_{gd3}: @ A: $Q = -1\text{V} \cdot C_{gd3}$, @C $Q = 0.8\text{V} \cdot C_{gd3}$, $\Delta Q = 1.8\text{V} \cdot C_{gd3}$

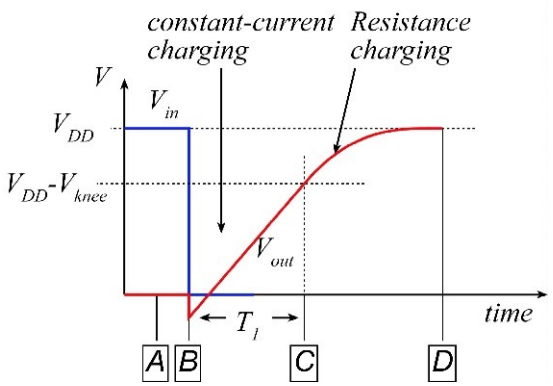
C_{gs3}: @ A: $Q = 0\text{V} \cdot C_{gs3}$, @ C: $Q = 0.8\text{V} \cdot C_{gs3}$, $\Delta Q = 0.8\text{V} \cdot C_{gd3}$

Time for drain of Q1 to charge to 0.8V:

$$T_1 = \left(1.8\text{V} \cdot C_{gd1} + 0.8\text{V} \cdot C_{gd2} + 1.8\text{V} \cdot C_{gd3} + 0.8\text{V} \cdot C_{gd3}\right) / 1\text{mA}$$

Example: Waveform at Q1 drain





Switching time between C and D: 2nd part: charging from 0.8V towards 1V

C_{gd1}: @ C: $Q = 0.8 \cdot C_{gd1}$, @ D: $Q = 1\text{V} \cdot C_{gd1}$, $\Delta Q = 0.2\text{V} \cdot C_{gd1}$

C_{gd2}: @ C: $Q = 0\text{V} \cdot C_{gd2}$, @ D: $Q = 0.2\text{V} \cdot C_{gd2}$, $\Delta Q = 0.2\text{V} \cdot C_{gd2}$

C_{gd3}: @ C: $Q = 0.8\text{V} \cdot C_{gd3}$, @ D: $Q = 1\text{V} \cdot C_{gd3}$, $\Delta Q = 0.2\text{V} \cdot C_{gd3}$

C_{gs3}: @ C: $Q = 0.8\text{V} \cdot C_{gs3}$, @ D: $Q = 1\text{V} \cdot C_{gs3}$, $\Delta Q = 0.2\text{V} \cdot C_{gd3}$

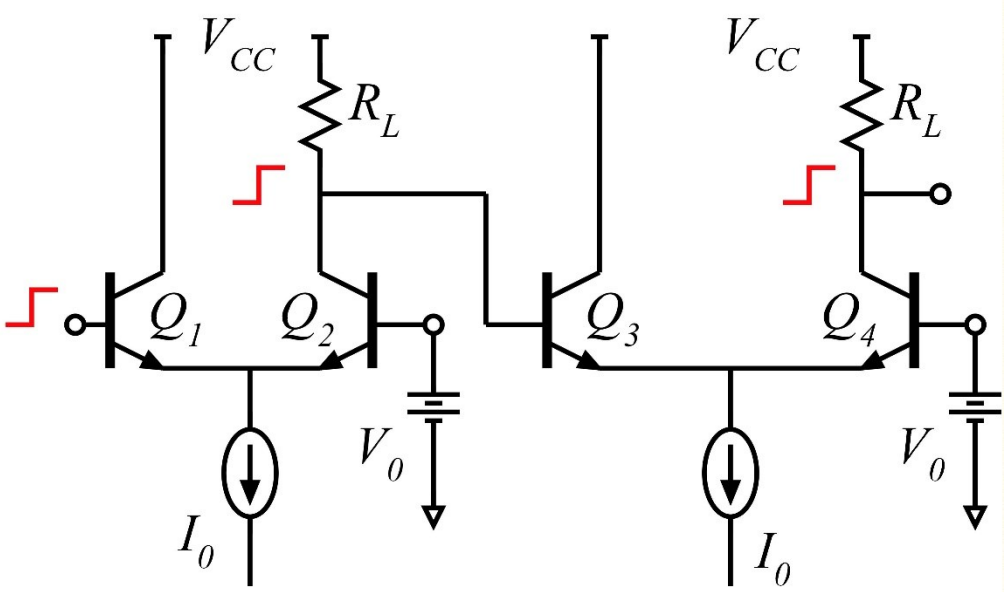
Effective capacitance :

$$C_{eff} = \left(0.2\text{V} \cdot C_{gd1} + 0.2\text{V} \cdot C_{gd2} + 0.2\text{V} \cdot C_{gd3} + 0.2\text{V} \cdot C_{gd3}\right) \Big/ 0.2\text{V} = \ldots$$

Time constant $\tau = R_{DS,sat} C_{eff} = R_{DS,sat}\left(C_{gd1} + C_{gd2} + C_{gd3} + C_{gd3}\right)$

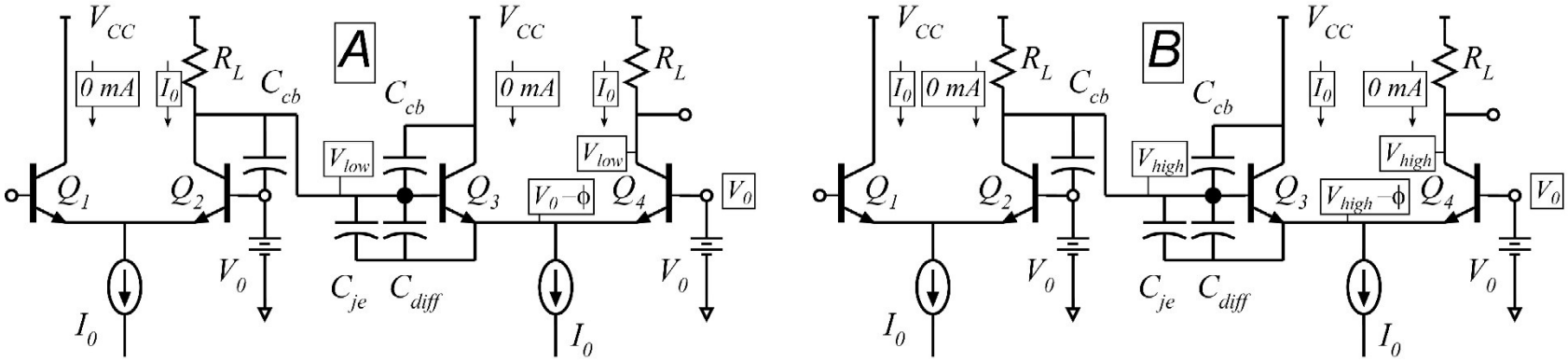
Exponential charging: $V_{D1}(t) = 0.8\text{V} + (1\text{V} - 0.8\text{V})(1 - \exp((t - T_1)/\tau))$

Example: bipolar differential switch



Let us calculate the risetime at the base of Q3

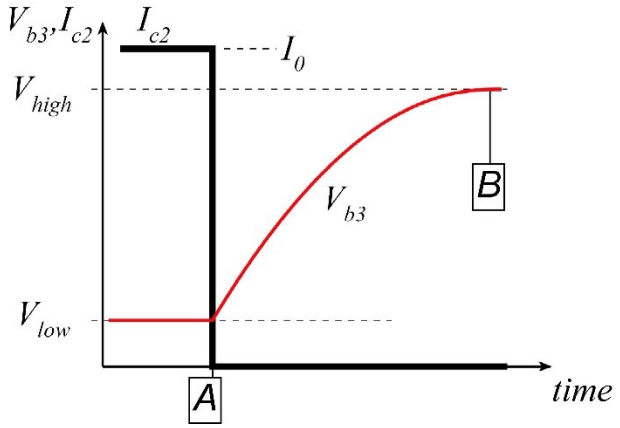
Example: bipolar differential switch



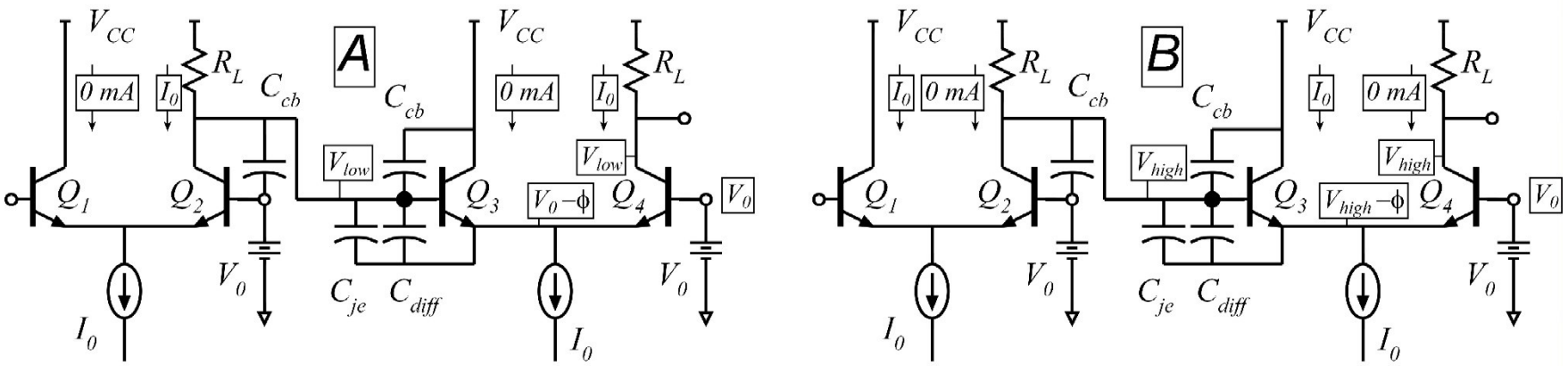
Let us calculate the risetime at the base of Q3

Times are relative to the time at which

the collector current of Q2 switches to zero.



Example: bipolar differential switch



Switching time between A and B:

change in charge in:

C_{cb2}: @ A: $Q = V_{low} \cdot C_{cb2}$, @ B: $Q = V_{high} \cdot C_{cb2}, \Delta Q = (V_{high} - V_{low}) \cdot C_{cb2}$

C_{cb3}: @ A: $Q = (V_{low} - V_{CC}) \cdot C_{cb3}$, @ B: $Q = (V_{high} - V_{CC}) \cdot C_{cb3}, \Delta Q = (V_{high} - V_{low}) \cdot C_{cb3}$

C_{je2}: @ A: $Q = (V_{low} - V_0 + \phi) \cdot C_{je2}$, @ B: $Q = (V_{high} - V_{high} + \phi) \cdot C_{je2}, \Delta Q = (V_0 - V_{low}) \cdot C_{je2}$

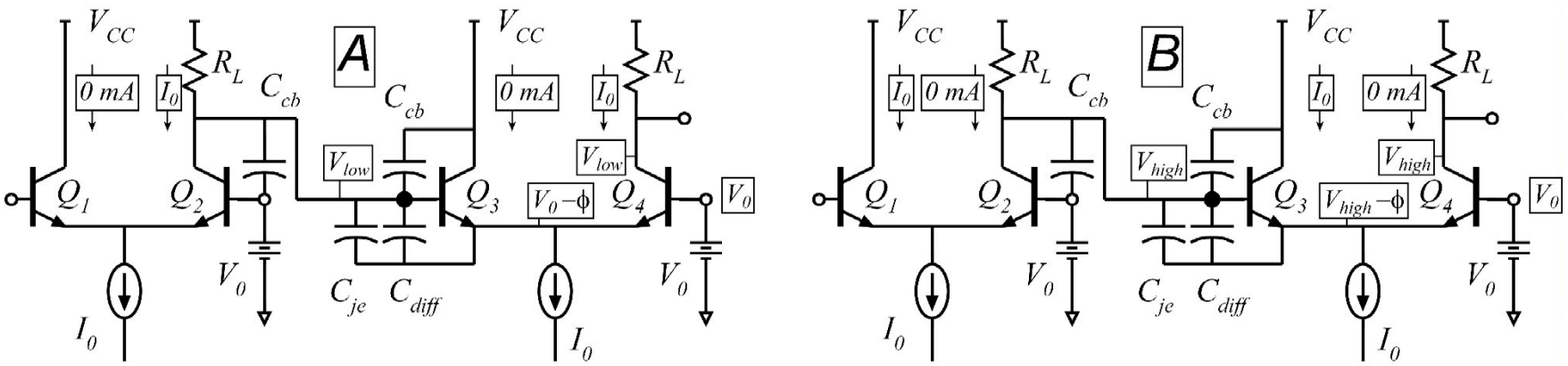
$C_{diff\,2}$: @ A: $Q = 0\ \text{mA} \cdot \tau_{f2}$, @ B: $Q = I_0 \cdot \tau_{f2}, \Delta Q = I_0 \cdot \tau_{f2}$

Effective capacitance:

$$C_{eff} = \Delta Q / (V_{high} - V_{low})$$

$$= \left((V_{high} - V_{low}) \cdot C_{cb2} + (V_{high} - V_{low}) \cdot C_{cb3} + (V_0 - V_{low}) \cdot C_{je2} + I_0 \cdot \tau_{f2} \right) \Big/ (V_{high} - V_{low})$$

Example: bipolar differential switch



Effective capacitance:

$$C_{eff} = C_{cb2} + C_{cb3} + C_{je2}\frac{V_0 - V_{low}}{V_{high} - V_{low}} + \frac{I_0 \cdot \tau_{f2}}{V_{high} - V_{low}} \quad \text{but } V_{high} - V_{low} = I_0 R_L$$

Charging time constant:

$$\tau_{\text{charge}} = R_L C_{eff} = R_L C_{cb2} + R_L C_{cb3} + R_L C_{je2}\frac{V_0 - V_{low}}{V_{high} - V_{low}} + \tau_{f2}$$

Voltage waveform:

$$V_{b3}(t) = V_{low} + (V_{high} - V_{low})(1 - \exp(-t / \tau_{\text{charge}}))$$

Limitations of charge control

1) the method is very approximate

2) We do not predict the detailed shape of the switching waveform
More detailed analysis can find secondary switching transients at one or move points within the overall waveform. In some cases, spikes are produced. This is more advanced material