A Gallery of Amplifier Circuits

ECE137A, March 2, 1995

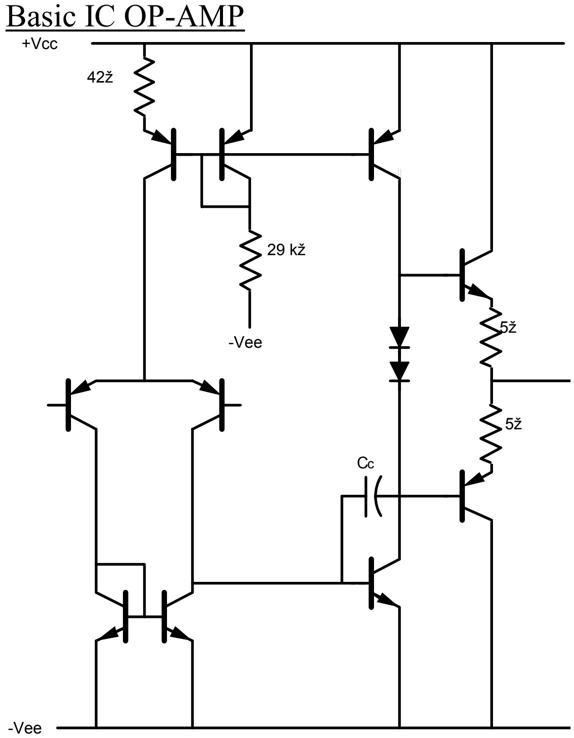
The text is a good complement to the lecture notes, but has one major weakness: most of the circuits in the text are very simple, on a quite tutorial level. One can learn a lot by looking through a catalog of IC designs for various purposes, looking at the structure of real solid-state circuits. The old National Semiconductor Linear Applications Handbooks are great for this purpose, if you can find them (you might ask the electronics shop for a hint on this). In the same spirit, below are a bunch of circuits taken from ECE137A/B problem sets over the years. <u>This is not an assignment, you dont need to work the problems</u>...but the listing might be a good study guide for the final, and is certainly intended as a list of hints and tricks for the lab assignment.

<u>IC-like Operational Amplifiers</u>

The circuits in this section are true op-amps, having the following important parameters. High or very high DC voltage gain. High common-mode rejection ratio. Low or very low output impedance. Big maximum peak-peak output voltage swings, within 1-2 volts of the power supply voltage. Operation over a wide range of DC power supply voltages with only moderate changes in circuit characteristics.

It would be instructive to work out the voltage gain, CMRR, and maximum signal swing for these circuits

<u>Basic IC OP-AMP</u>



In the op-amp circuit to the right, all NPN transistors have ß=100 and Va=100 Volts. All PNP devices have ß=50 and Va=75 Volts.

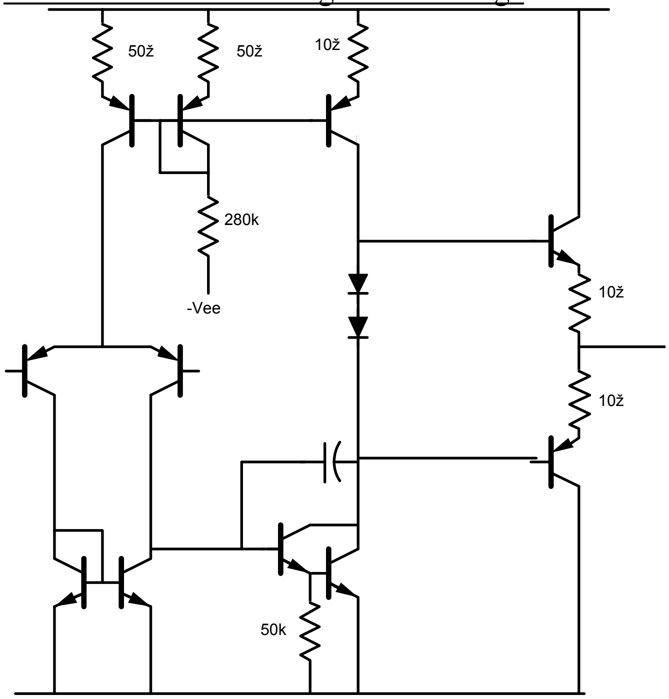
Load resistance of ≈ 1000Ω,

The power supplies are ±15 Volts.

The compensation capacitor is quite important: see other notes.

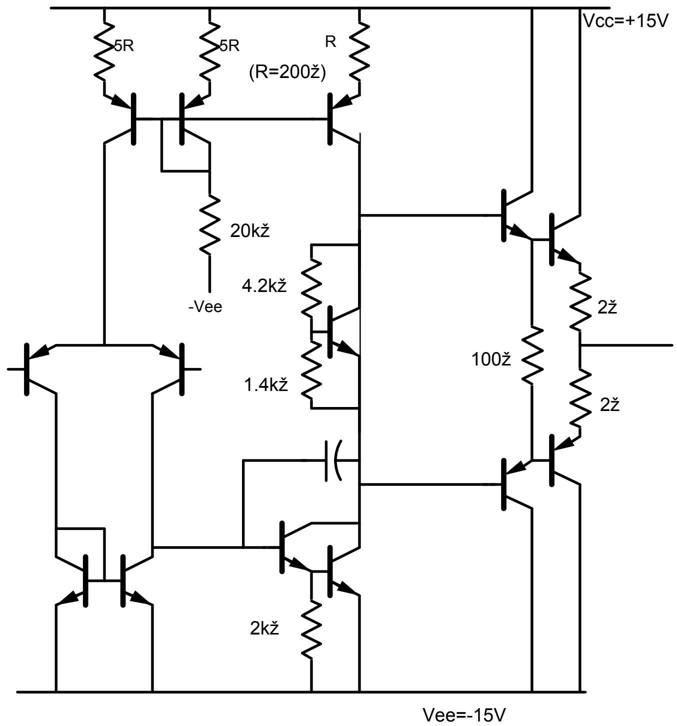
As in all high-gain amplifiers intended for use with negative feedback, bias analysis can be a little tricky. Work from assumption that the DC output voltage (bias condition) is zero volts: this is generally what the negative feeback network will force.

IC OP-AMP with Darlington Gain Stage



Same transistor parameters as above. The darlington stage (e.g. the added emitter follower) increases the equivalent load impedance for the first (differential) stage, increasing its voltage gain.

IC OP-AMP with Darlington Gain Stage and Darlington Output Stage



This operational amplifier is considerably more complex, more like a real one. With changes in element values, this is also what a typical audio power amplifier looks like

All ß=75, V_A=150V.

Again, the common-emitter stage now uses a darlington, which increases its input impedance, thereby increasing the voltage gain of the first (differential) stage.

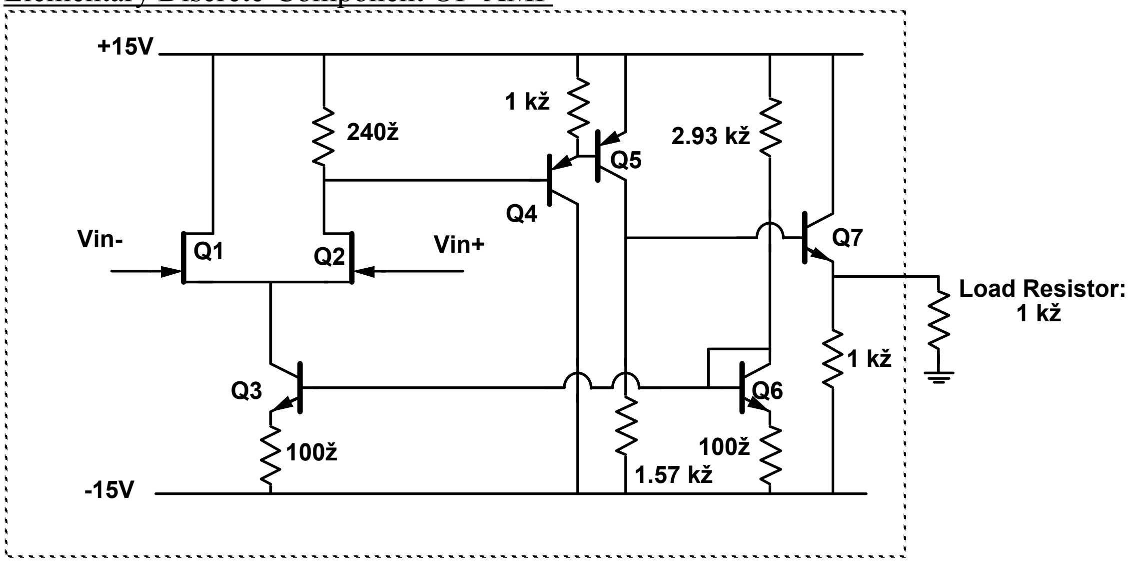
Additionally the ouput stage also uses a push-pull darlington, thereby increasing the load impedance on the common-emitter stage, increasing its gain.

The output stage bias is set by a "Vbe multiplier", which could be adjustable by making the resistor (4.2kΩ) a trimpot.

Elementary Operational Amplifiers

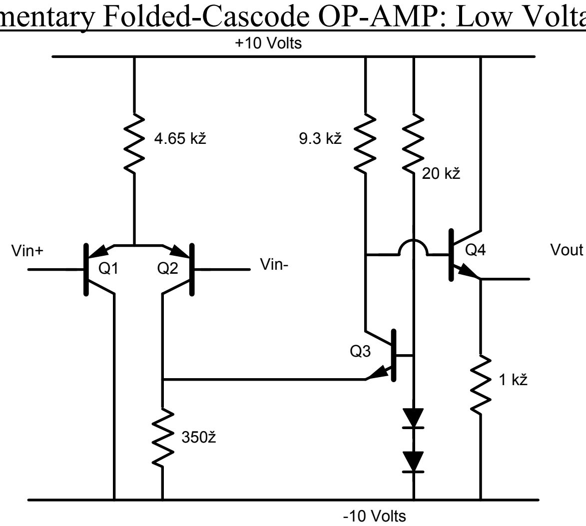
The circuits in this section are differential ampifiers with reasonably large DC voltage gains, intended for use with negative feedback. In the aim of simplifying the circuit, one or more of the desired op-amp parameters listed in the previous section has been sacrificed

Elementary Discrete-Component OP-AMP



In the above circuit, an operational amplifier, the two JFETs have Idss=40mA and Vp=-3 Volts. The bipolars all have ß=50 and V_A=50 Volts.

Elementary Folded-Cascode OP-AMP: Low Voltage Gain



This is a very simple (and not terribly high gain) operational-amplifier. All transistors have $V_A=\infty$ and ß=500.

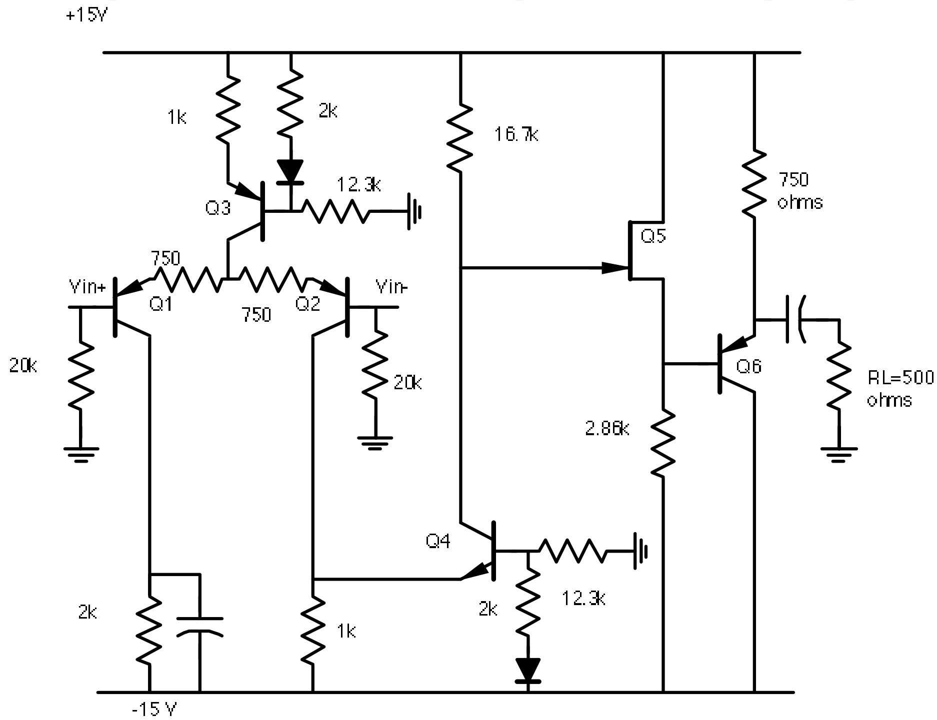
As in all high-gain amplifiers, bias analysis can be a little tricky. Work from assumption that the DC output voltage (bias condition) is zero volts.

Output drive is limited by the class-A output stage (why?). Base Bias on Q3 is quite close to the negative rail for output swing considerations (why?).

Differential Amplifiers

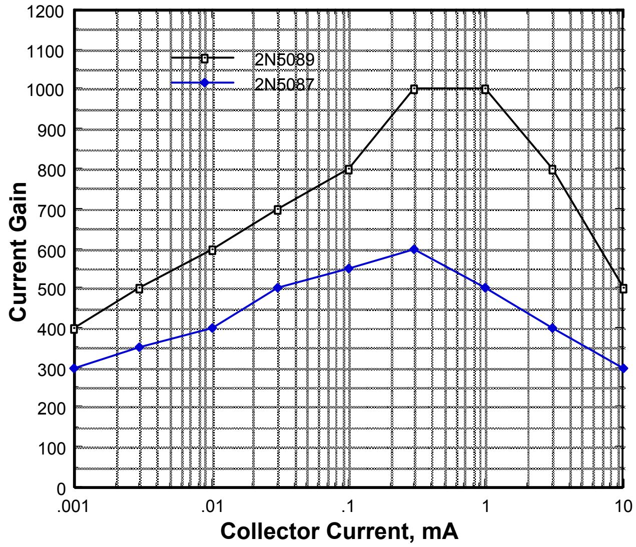
These are not op-amps, being designed for use without negative feeback. In some cases, the circuits are quite high-performance in their own right; others are just "problem set" circuits included here to show various circuit tricks.

AC-Coupled Low-Gain Differential Ampifier with Low output impedance

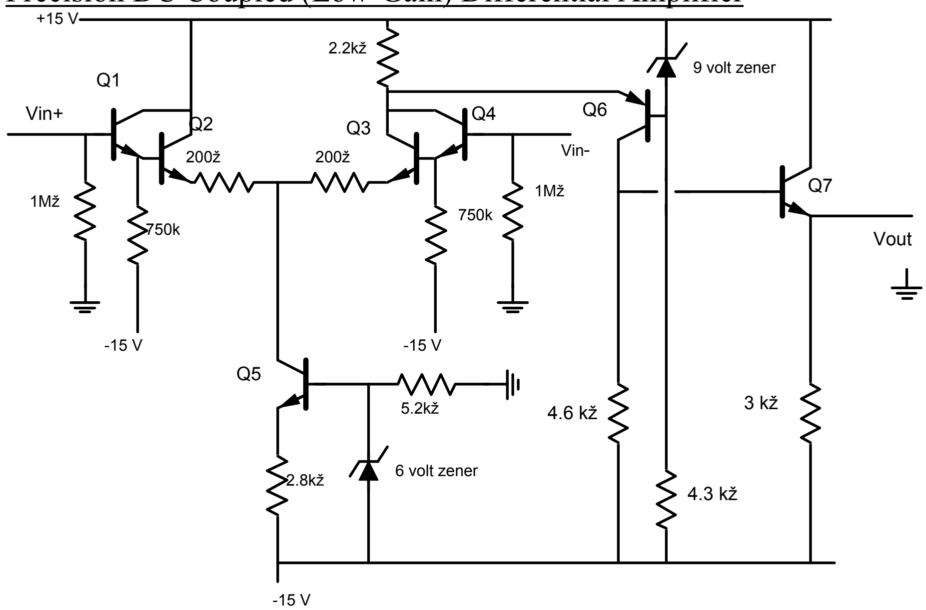


Transistors: Q4 is 2N5089; Q8 is a 2N3906, and Q1,Q2 and Q3 are 2N5087. Assume all transistors are well-matched. The FET has Idss=10mA and Vp=-3 Volts. All bipolar transistors have $V_{be(on)}$=0.7 V.

This amplifier is a differential stage with a folded cascode and a buffer. The differential input is useful for DC coupling or for applications needing rejection of common-mode signals. The folded cascode (Q4) really has no impact on the voltage gain, but its level shifting greatly improves the amplifier's maximum peak-peak output swing. Q5 and Q6 are buffer stages providing a large current gain, so that low impeances can be driven.



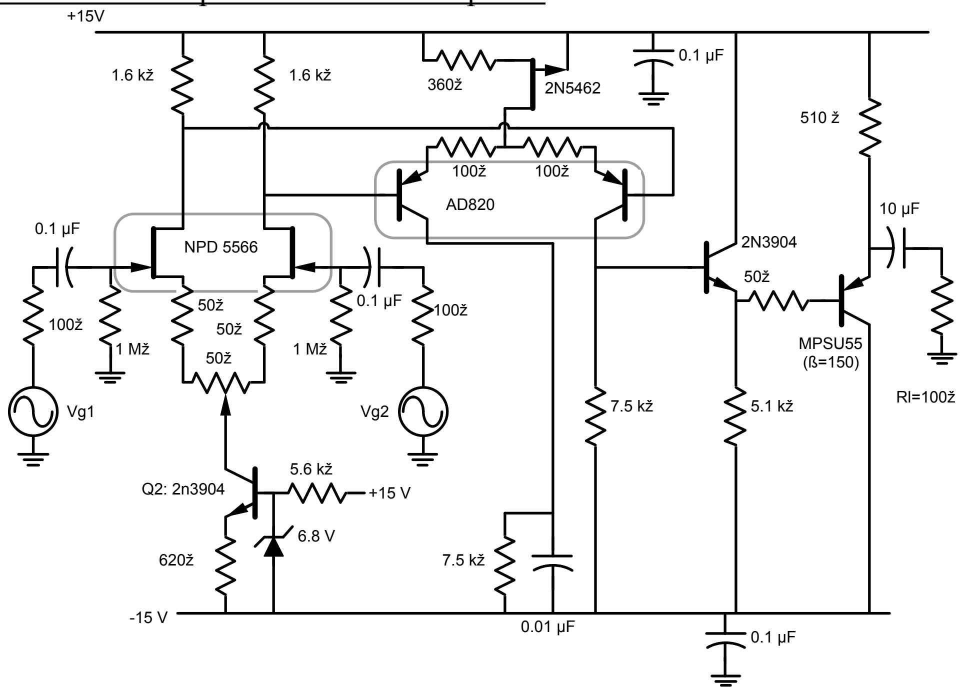
Precision DC Coupled (Low-Gain) Differential Amplifier



Transistors: Q1-Q5 are 2N5089; Q6 is 2N5087. Assume all transistors are well-matched. All transistors have $V_{be(on)}$=0.65 V. V_A=100 V(NPN), 80 V (PNP).

Circuit design issues are quite similar to the previous amplifier. The differential stage in this case has very high input impedance. Q6, in the folded cascode configuration, provides level-shifting in order to improve the peak-peak drive capability, and Q7 is a buffer. The voltage gain is about 10 being approximately 4.6kΩ/(200Ω+200Ω+Re2+Re3). Can you see this without doing detailed circuit analysis?

High-Gain AC-Coupled Differential Amplifier

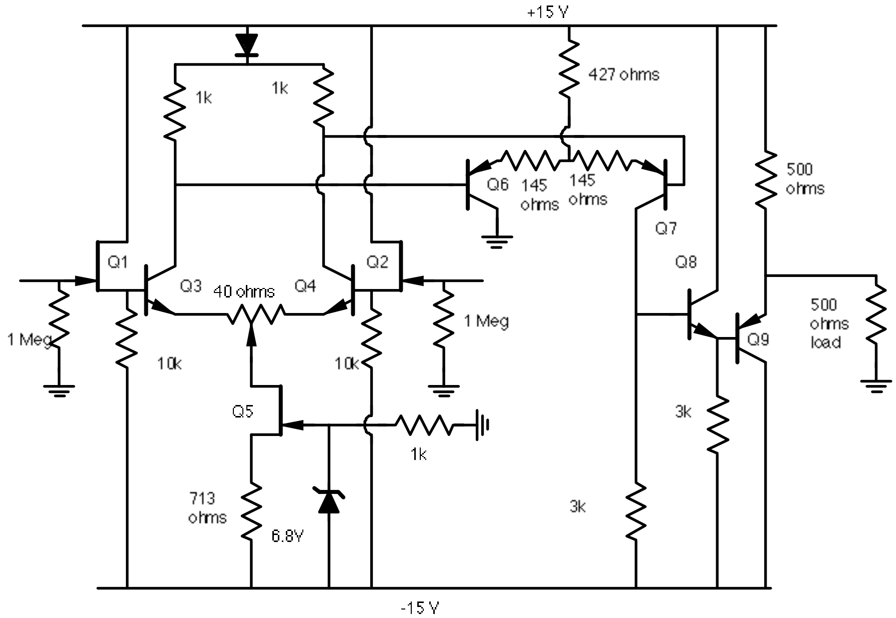


AD820 Matched pair: ß=75
NPD5566: Idss=15 mA, Vp=1.8 Volt, V_A=100 V
2N5462: |Idss|=10 mA, |Vp|=4 volt, $|V_A|$=80V
All NPNs: Va=100 V; All PNPs: Va=80 V.
Use the datasheet values for the 2N3904's.

The 50Ω potentiometer is set so that the currents are balanced in the AD820 matched pair.

This is a fairly high-gain differential amplifier. Use of cascaded differential pairs, combined with the constant current sources, leads to a very high common-mode rejection ratio.

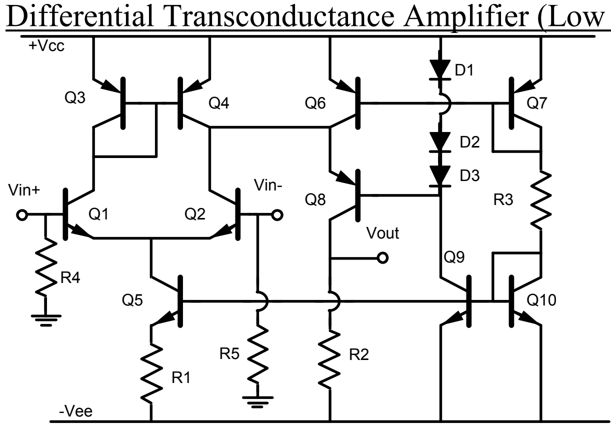
Another High-Gain DC-Coupled Differential Amplifier



The 50Ω potentiometer is set so that the currents are balanced in the differential pair.
Q1 Q2 Q5: Idss=15 mA, Vp=1.8 Volt, V_A=100 V
Q3, Q4,Q6,Q7: 2n5087 or 2n5089 (depending whether PNP or NPN), Curves of ß vs collector current were given in above. Remaining transistors are 2n3904 or 2n3906.

This is another differential amplifier with moderately high gain, but not really designed for use as a feedback amplifier. Q1 and Q2 give a high input impedance. The complementary darlinton output stage gives a low output impedance (can drive a low-impedance load). Cascaded diffential stages give a high CMRR.

Differential Transconductance Amplifier (Low Voltage Gain, High Output Resistance



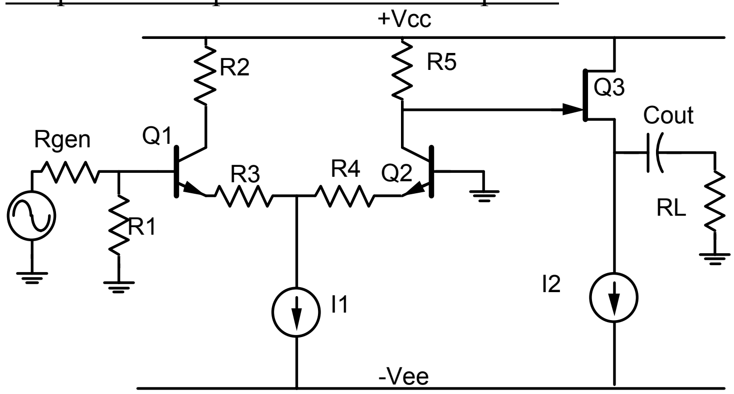
All PNP transistors are matched, as are all NPN transistors. All have ß=750 and V_A=200 V.

R3 is picked so that the collector current of Q10 is 1 mA. R1 is picked so that the collector current of Q5 is 100 µA. R2 is picked so that Vout=0V when Vin^+=Vin^-=0V

Vcc=15V, -Vee=–15V, R1=R2= 50kΩ

This is not a very practical amplifier as drawn, as the voltage gain is quite low and the output impedance quite high. It does illustrate how one might bias a folded-cascode on an IC.

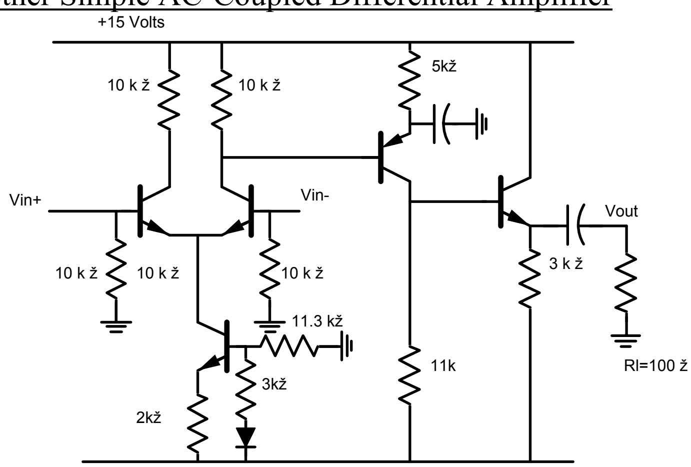
Simple AC-Coupled Differential Amplifier



In the circuit at left:
R2=R5=1 kΩ
R3=R4=0Ω
R1=1kΩ
Rgen=100Ω
RL=500Ω
I1=I2=10mA
The power supplies are ±10V
Q1,Q2: ß=100, $V_A=\infty$
Q3: Idss=20 mA, Vp=-2V

Just a Tutorial circuit.

Another Simple AC-Coupled Differential Amplifier

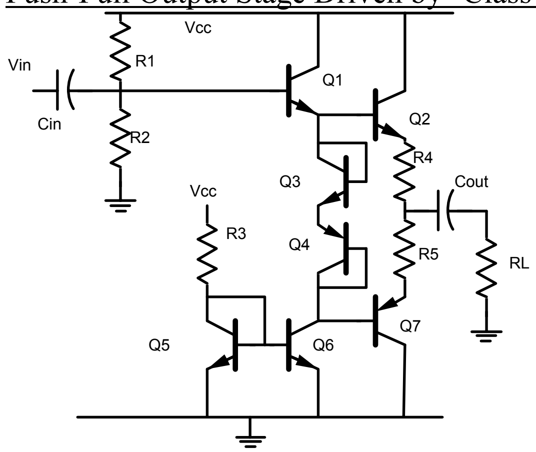


The NPNs and PNPs are 2N3904's and 2n3906's

Tutorial circuit perhaps. Definitely AC coupled. Very high gain. Might be useful in an application where high AC gains are required but precise gain control is not important (why?).

Other Circuits

Push-Pull Output Stage Driven by "Class A" (not-push-pull) emitter follower



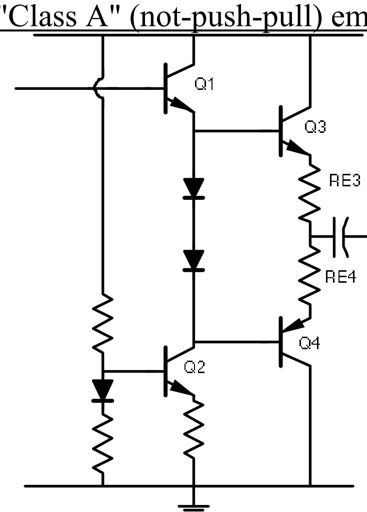
This is more or less the output stage of lab 2. Vcc=+15 V. All transistors have ß=100 and $V_A=\infty$.
$I_{s1}=I_{s3}=I_{s4}=I_{s6}=I_{s5}=I_{s2}/10=I_{s3}/10$
R1=R2=10kΩ. RL=10Ω
Pick R3 so that Ic5=10 mA.
Setting R4=R5, choose R4 and R5 so that Ic2=Ic7=30mA.

Cout and Cin have negligible capacitive reactance at the frequencies of operation.

This is an exercise in finding the bias currents in a push-pull output stage by current-mirror methods.

Another Push-Pull Output Stage Driven by "Class A" (not-push-pull) emitter follower

Q3 and Q4, together with the 2 diodes are a push-pull emitter follower Q1 is another emitter follower, whose pull-down is a current source (Q2) rather than a resistor.



RE3 and RE4 are to provide some stabization of the bias current.

Saturation of Q2 can limit the output swing, so its bias must be chose carefully. Its quiescent current limits the maximum drive current to the output stage...