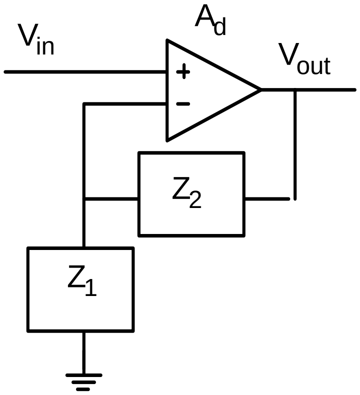
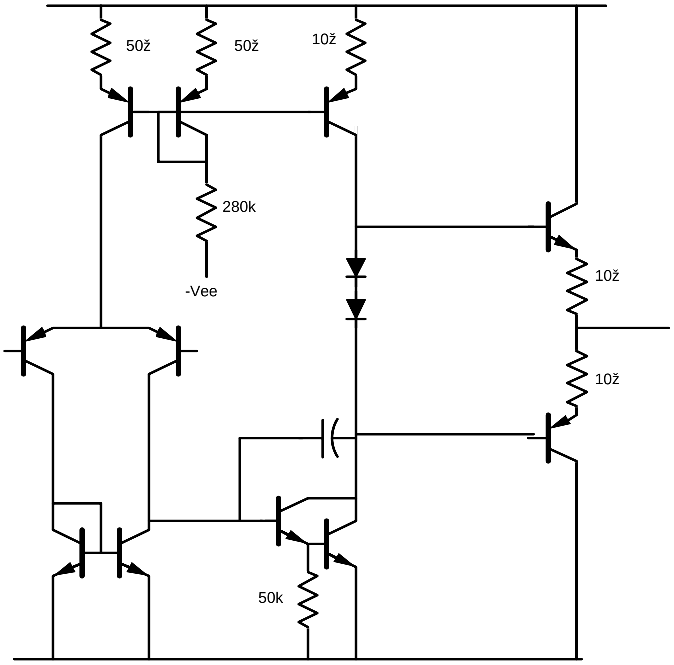


$$V_{out} / V_{in} = \frac{Z_1 + Z_2}{Z_1} \times \frac{A_d Z_1 / (Z_1 + Z_2)}{1 + A_d Z_1 / (Z_1 + Z_2)_1}$$

If the amplifier gain is reasonably large, so that $A_d Z_1 / (Z_1 + Z_2) >> 1$, then

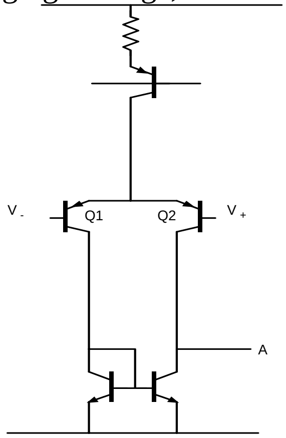
$V_{out} / V_{in} \cong \frac{Z_1 + Z_2}{Z_1}$, which is the desired mode of operation.

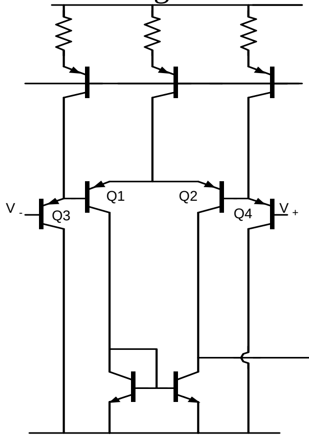
Negative feedback can become positive if there is 180° phase shift in the amplifier. This can and will happen at sufficiently high frequencies because of the amplifiers' high-frequency rolloff (due to transistor capacitances). If the feedback is positive and of magnitude greater than 1, then the feedback circuit will oscillate. To avoid this, the op-amp high-frequency response must be tailored so that the gain of the feedback loop decreases gracefully to below unity before the phase shifts add up to more than 180°. This is called compensation.

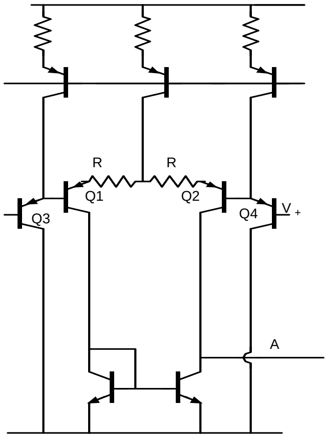


Above is one op-amp circuit. Several more are shown in a related hand-out.

Most op-amps can be broken down into three parts: A differential input stage, a second voltage-gain stage, and an output buffer stage.

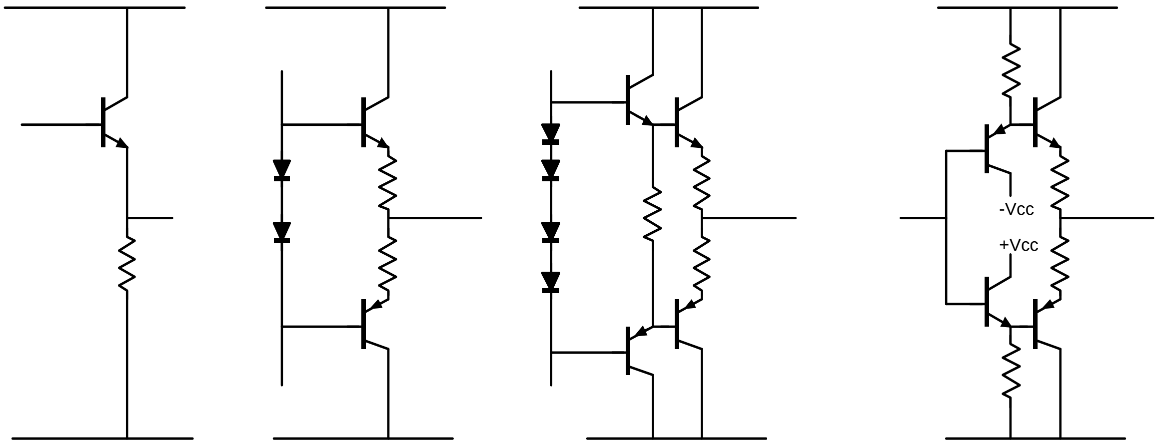




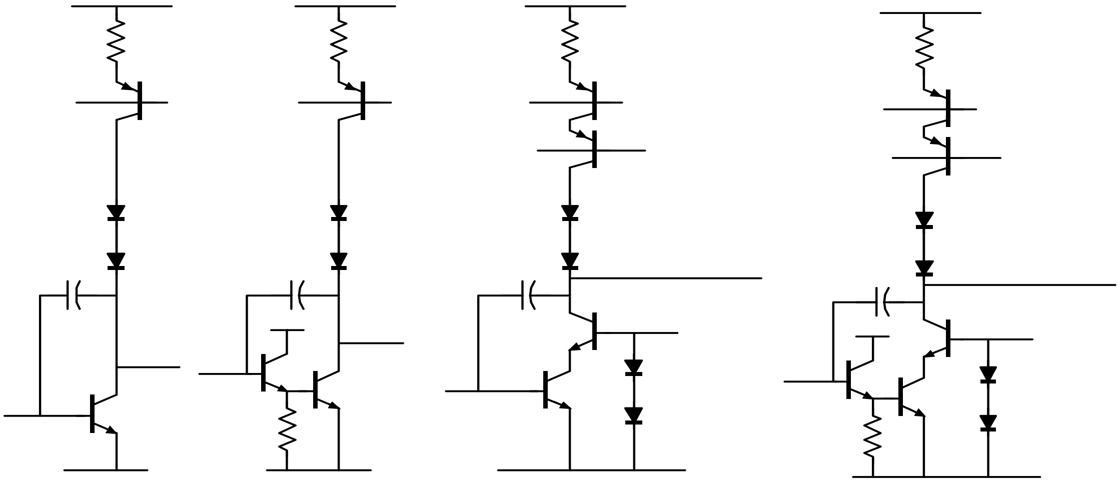


The input stage might look like any of the above 3 examples (or none of them). If we apply symmetry, so that re1=re2, and the emitter-follower buffers have identical voltage gains Av3=Av4, then the overall voltage gains of these three input stage examples are: Av=Rleq/re1 (first example), Av=Av3(Rleq/re1) (second example), and Av=Av3(Rleq)/(R+re1) (third example). You get the picture, and can generalize to any input stage design you like. (The factor of 1/2 has vanished in the gain expressions because of the current-mirror load: read the notes...).

In general, from the above, we can always write the voltage gain of the input stage to be $A_{v,input} = g_{m,input} R_{leq}$, where $g_{m,input}$ is some number (1/re1, Av3/re1, and Av3/(R+re1) in the 3 examples above.



The third stage, the output stage, is almost always some kind of compound emitter follower stage. A few are illustrated above. In general, the output stage simply has some voltage gain slightly less than, unity, which we will call $A_{v,output}$



In between these two stages is a voltage-gain stage, usually a common-emitter stage with perhaps an emitter-follower buffer and/or a cascode connection. One can find its gain at low frequencies by the usual methods. This stage, however, almost always has a compensation capacitor connected between its input and output, as shown. Skipping the analysis (you can ask me...), the overall differential gain of the op-amp, at higher frequencies is given by:

$$A_d(f) \cong \frac{g_{m,input}}{j2\pi fC} A_{v,output}$$

So, in you lab design, choose C such that the differential gain has a magnitude of 1 at a frequency somewhere between 100 kHz and 1 MHz.