ECE 145A/218A, Lab Project #1b: Transistor Measurement.

September 24, 2023

Overview

Goals:
(a) Learning how to measure S-parameters of active devices, including reference plane offset techniques

(b) Obtaining data which you can use for later lab projects !

Safety Precautions:
(a) Observe static precautions when working with the network analyzer. Wear the wrist strap.

(b) Never connect a network analyzer directly to a circuit carrying dc. Make sure your circuit is dc blocked, or you will destroy the NA.

Reading:
Refer to HP 8751A Network Analyzer User's Guide (RBR and in lab - do not remove!)

Transistor RF Characterization.

Use either an MRF901 or MRF951 bipolar transistor for this lab; as of 2023, we have a larger stock of MRF901's. Please note that the MRF901 is available in either a micro-cross or a surface-mount package. The ADS model is available only for the surface-mount package; the models will differ slightly because the internal bond-wires are shorter for the surface mount package. But, the micro-cross package has larger contacts and hence it is much easier to solder by hand to the micro-cross package. I suggest that you use the micro-cross package version of the MRF901, and simulate circuits using the ADS model of the surface mount version. The model inaccuracy is probably smaller than that due to unmodelled PCB assembly parasitics.

DC bias circuits

To provide gain, transistors must be provided DC bias currents and voltages. These bias circuits are built into normal amplifier designs. To simplify transistor measurements, and to prevent the bias circuits from corrupting the measurements, NWAs have internal bias networks (bias Tees) for transistor biasing. If you use the NWA's internal bias Tees, and accidentally apply a short-circuit, or apply excess voltage, you will damage or destroy the instrument. ***So, we will not use the NWA bias Tees in this class***. Instead, we will use the bias network of Figure 1.

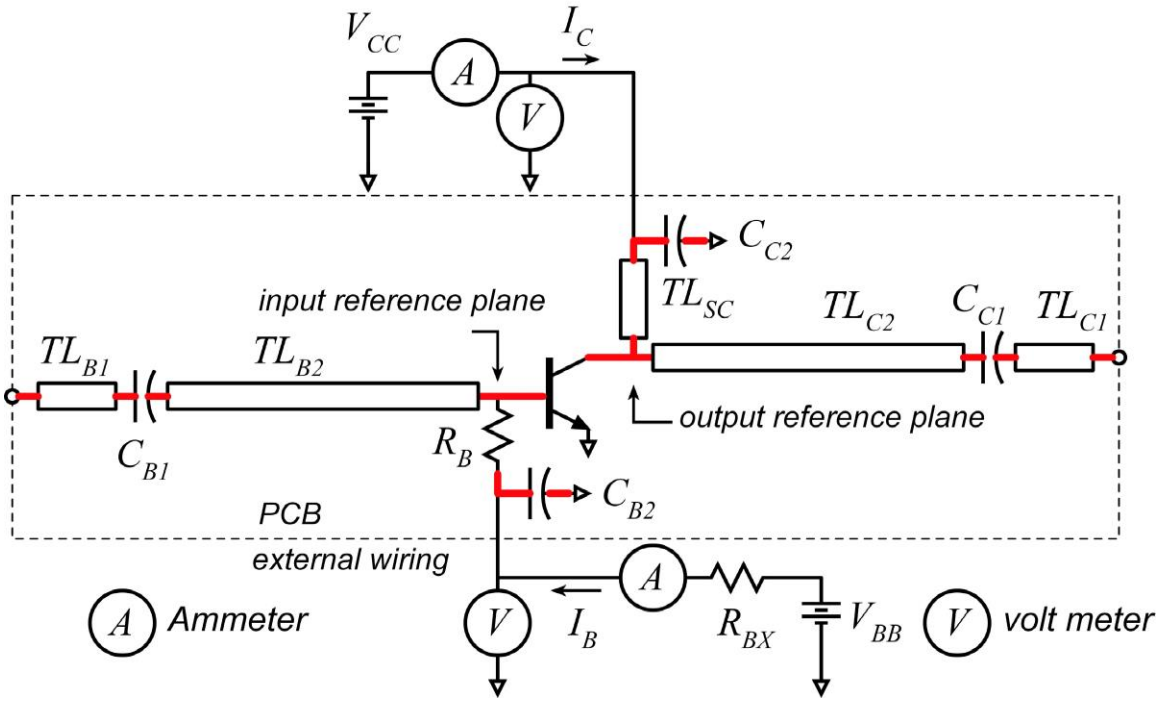

Figure 1: Circuit Diagram for BJT biasing. The red conductor should be a short as possible; certainly less than 2 mm length, and preferably shorter still. All transmission-lines have $Z_0 = 50\ \Omega$; the shunt stub lines TL_{SC} is one-quarter of a transmission-line wavelength at the design frequency you have chosen.

In Figure 1, the base is biased with a large voltage V_{BB}, chosen much larger than the base-emitter turn-on voltage ϕ, ~0.7-1.0 Volts, through the bias resistors R_B and R_{bX}, setting up a base current $I_B = (V_{BB} - \varphi) / (R_B + R_{BX})$. The collector current is $I_C = \beta I_B$. The collector voltage is $V_{CE} = V_{CC}$.

You will bias the transistor with I_C = 5 mA and V_{CE} = 10 V. Given that the transistor DC current gain is c.a. 50-200, the base current might be 25 to 100 μA. Set R_B = 10 kΩ, and choose a value of R_{bx} such that I_b does not vary too rapidly as you vary V_{bb}. With R_B = 10 kΩ, the shunt RF loading of this resistance will only negligibly decrease the transistor RF gain.

Caution: this base-current bias method is simple and easy for laboratory testing. Because production BJTs have highly variable β, base-current-biasing provides poor control of the collector current and is almost never used in production circuits. More on this in lectures !

There will be a target frequency for your measurements. This will later become the choice of design frequency for your amplifier in lab project #3. ***This frequency will be announced in lectures, with different frequencies for ece145A and ece218A lab projects***. The length of the transmission-line sections TL_{SC} must be set to be one-quarter of a *transmission-line* wavelength at the design frequency you have chosen. This will decouple the transistor collector from the DC supply at the design frequency. Though you can use ADS to determine this length, the simulated and measured transmission-line velocities will differ because of the adhesive on the back of the copper tape: it may be wise to check your simulations against the measurements of lab 1a.

Test fixture construction

<u>reference plane offset measurement</u>

Once again, we must measure the reference plane offsets as part of the procedure. First (Figure 2) construct a 50 Ohm microstrip line on a board. At the exact center of the board, drill a small hole. This hole should no larger than the minimum needed to mount the transistor. The metal line should then be cut, separating ports 1 and 2. If done well, the metal lines reach up to the edge of the hole with zero gap whatsoever. If done well, the hole is exactly the size of the transistor package.

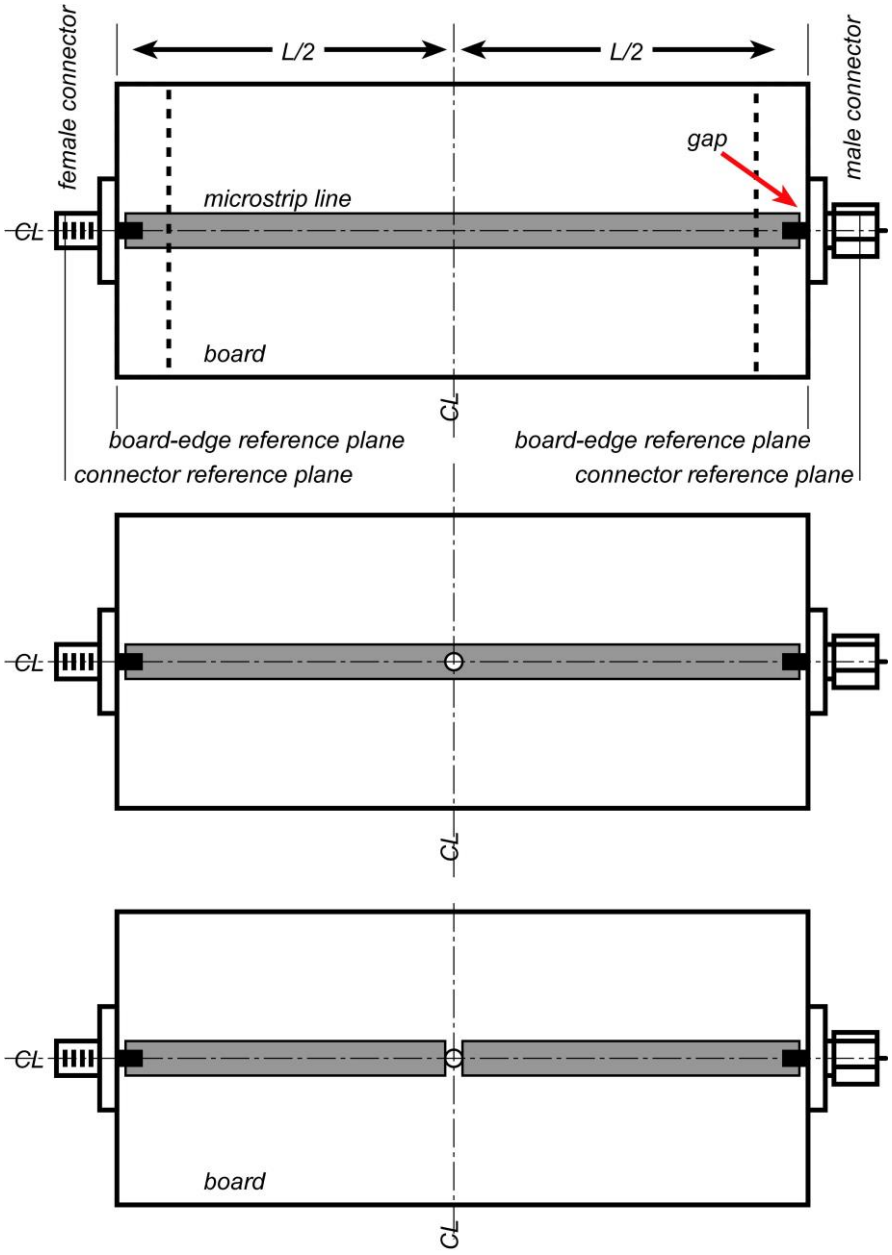

Figure 2: First steps in fixture construction. Through line (top), after drilling a hole (center) and after cutting the lines (bottom)

We now must measure the reference plane offset. To do this, calibrate the network analyzer, measure the board's S-parameters, and adjust the port 1 and port 2 reference plane offsets until you have nearly a perfect open-circuit on ports 1 and 2. Record the values of these offsets.

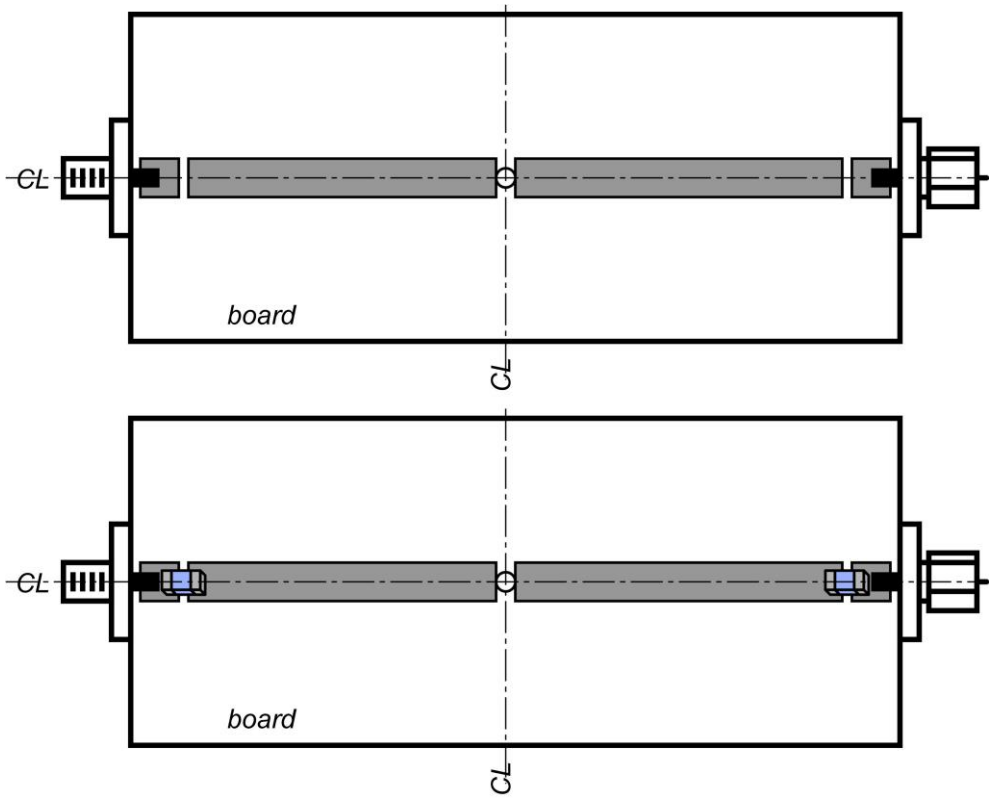

Figure 3: mounting the DC blocking capacitors

Then (Figure 3), make small (1 mm or less) cuts in the signal conductors, very close to ports 1 and 2, and solder in place 1 microfarad DC blocking capacitors. Again, precise work is critical here.

Fixture construction

Figure 4 shows details of fixture construction. Mount the *leaded* (not chip) base resistor vertically as shown. By mounting it vertically, centered in the microstrip line, capacitive loading from the resistor body to the ground plane is minimized. The long vertical wire lead, raised far above the ground plane, on the "cold" (no RF) side of the resistor adds series inductance, further reducing the resistive loading. The cold side of the resistor is grounded with a chip capacitor, copper pad, and via made by drilling a narrow hold in the board, running a wire through (think: inductance) and soldering it in place.

Figure 4 also shows transistor mounting. Emitter (or source) lead inductance should be made very small, so the hole is the board is very small, the transistor is mounted close to the ground plane side, and the leads are bent and soldered in place.

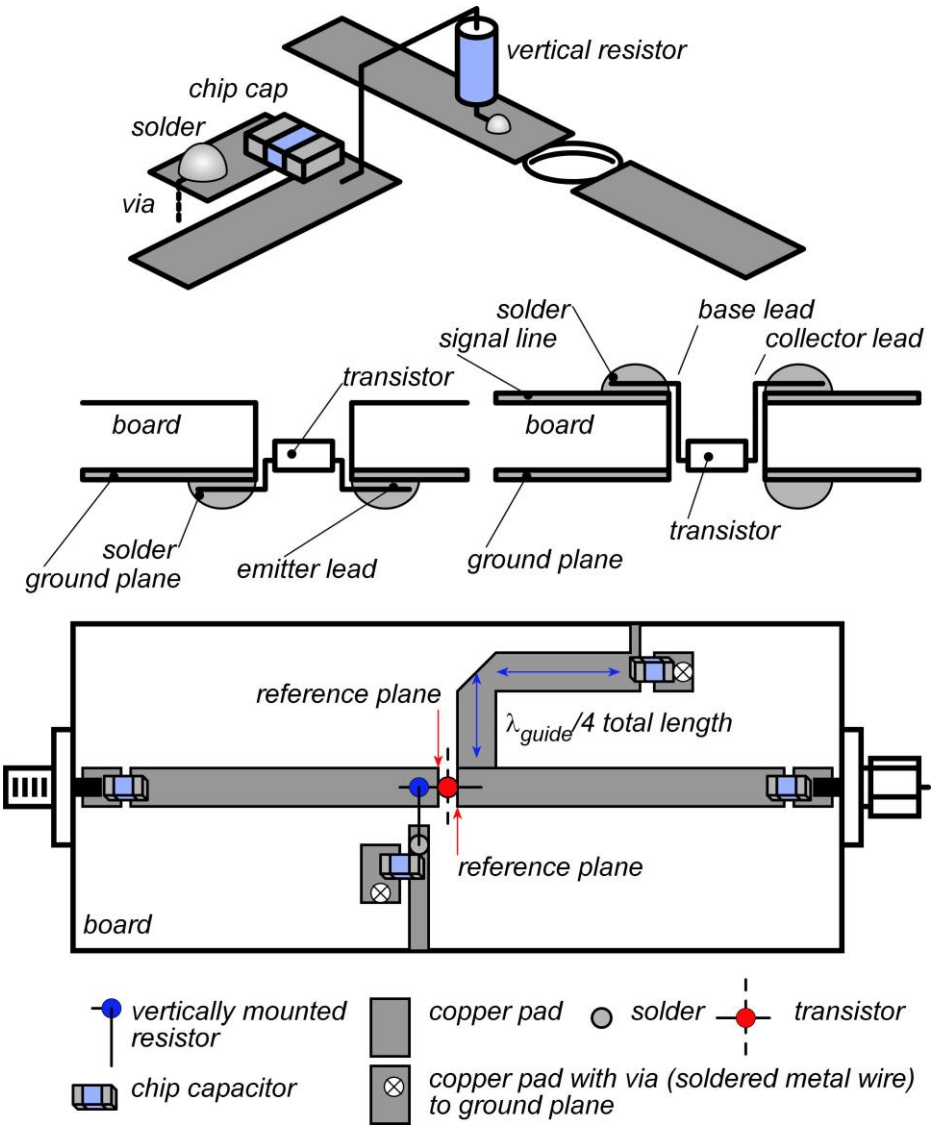

Figure 4: Details of fixture construction

The key is again tight control of dimensions. In the signal path (the microstrip lines, the transistor leads, the DC blocking capacitances, the launcher tabs) we need keep lead lengths between microstrip lines less than 1 mm. In the resistor paths, we are trying to create large series inductance (hence the elevated "cold" leads to the resistors) and are trying to minimize shunt capacitive loading from the resistor bodies to the ground plane, hence the vertical resistor mounting which keeps the resistor body far from the ground plane.

Note also (Figure 5), that the bias networks should be as close to the transistor as possible. In particular, the collector bias feed line should be less than 1/8 inch of the transistor end of the microstrip. If this is not done, your measurements from this lab will not be useful for the next lab project, and you will have to re-do your measurements later.

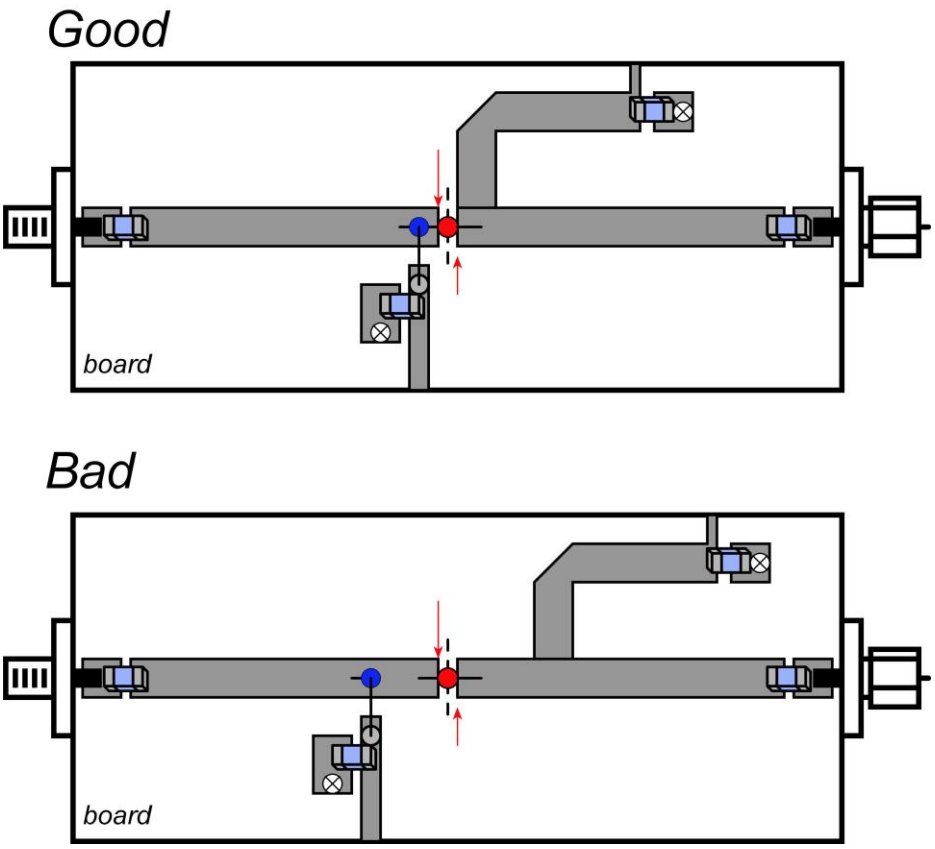

Figure 5: The bias networks should be as close to the transistor as possible.

Note that for resistors in series with (as opposed to in shunt to) the RF signal path, the series inductance must be minimized. In that case we would use leadless chip resistors mounted flush to the PC board, soldered across a narrow gap in the microstrip line.

Assignment

You must construct the above fixture, mounting the transistor MRF-901, and choosing resistor values appropriate to bias the transistor at 5 mA collector current and 10 Volts collector-emitter voltage.

Calibrate the instrument (reference plane offsets must be zero when you do this), dial in the reference plane offsets, and measure and store the resulting S-parameters for future use in lab 3. Care in taking measurements in lab 1b will save time later when you work on lab 3. Make a Bode plot (dB magnitude vs. log frequency) of the maximum available/ maximum stable gain. Make a similar plot of 20*log10(||H21||) vs. log frequency, manually entering the 20log10 expression rather than using the dB function, as ADS will in error use 10*log10(||H21||) if you ask for its dB magnitude. From this, attempt to determine the current-gain and power-gain cutoff frequencies.

You should now compare your measurement with the available transistor data. Simulate the combination of the transistor, base bias network, and collector bias network.

Use the ADS model of the surface mount version of your transistor. Compare your measurements to these models.

Keep your measured S-parameters, and your board: you will use it for later for lab project 3.