ECE 145A / 218 C, notes set xx: Class A power amplifiers

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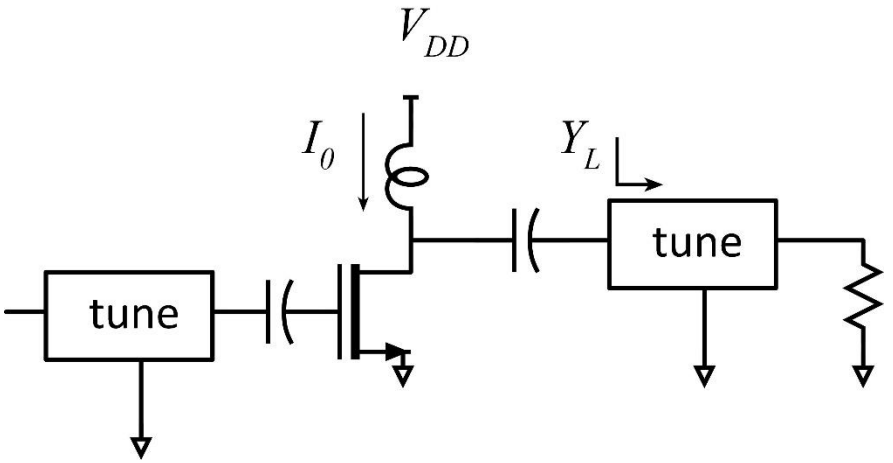
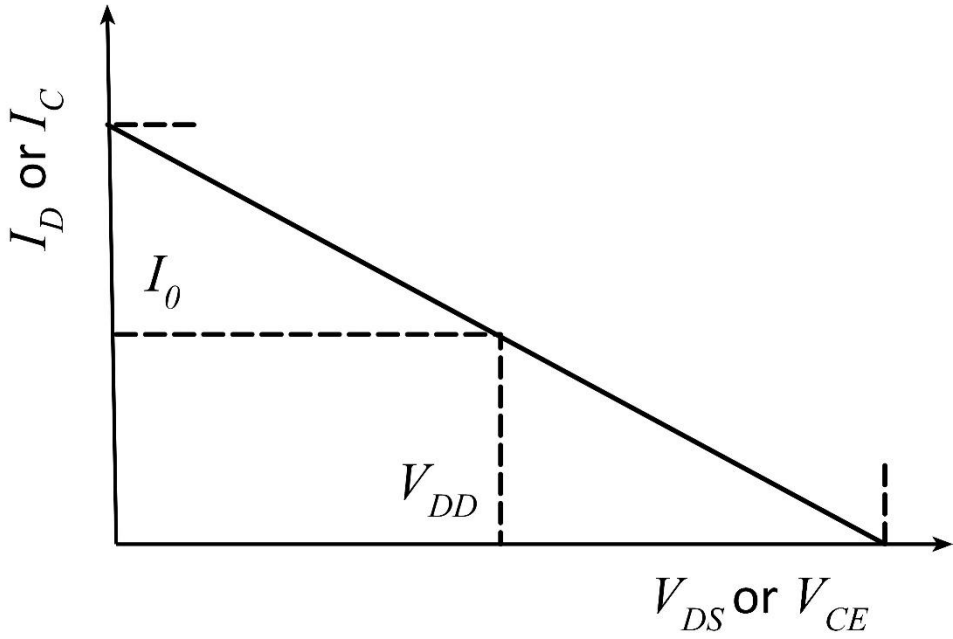
Class A power amplifier: what do we mean ?

PA has input, output tuning

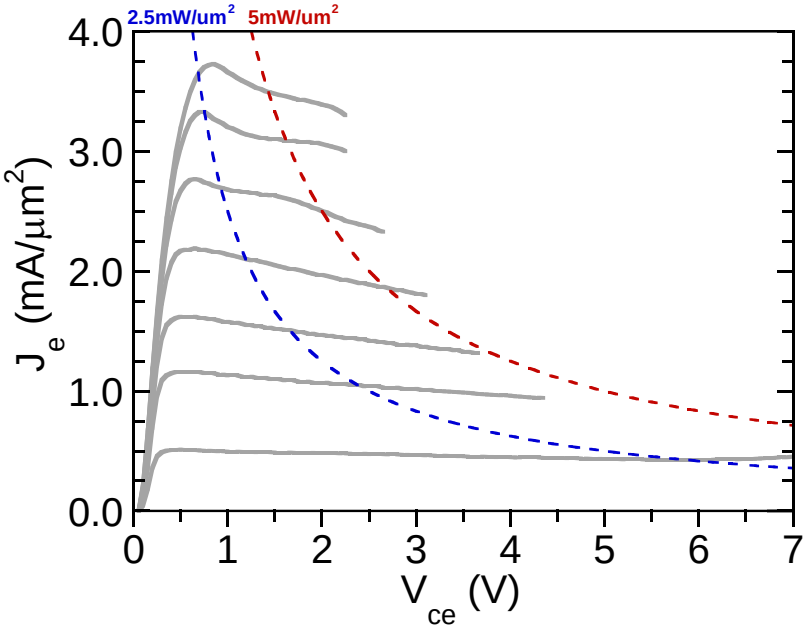


loadline would be as so

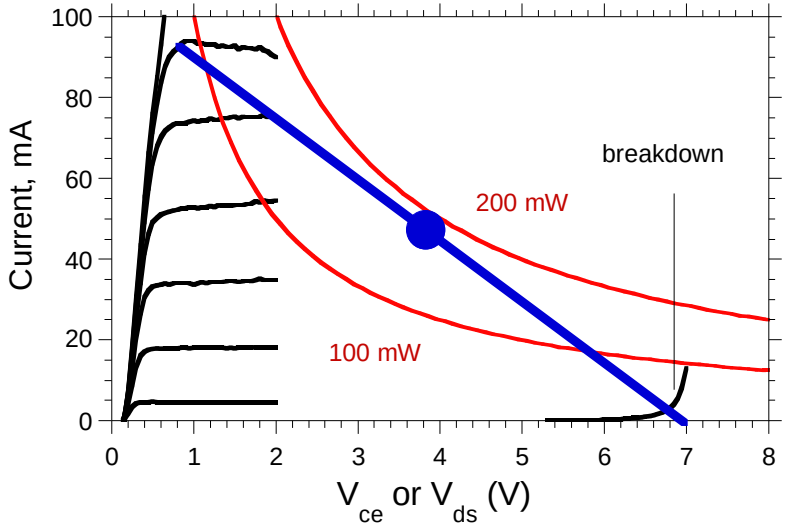


Transistor Output Characteristics: Real

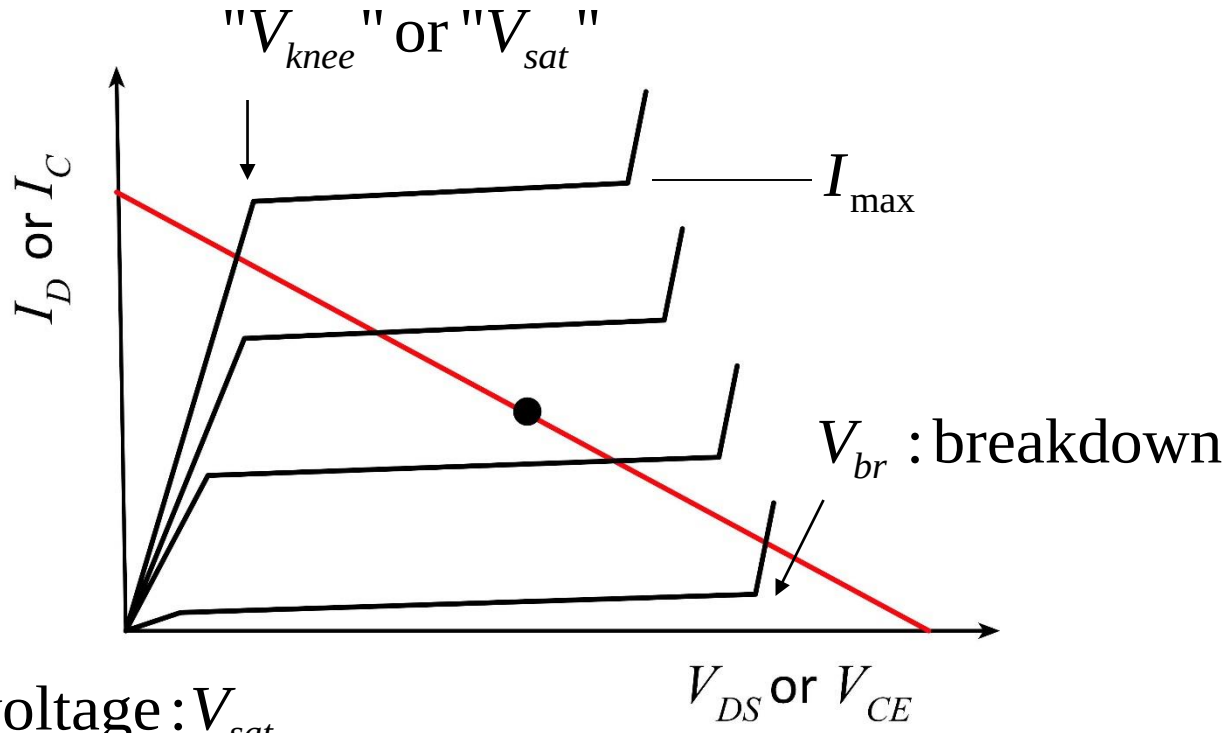
250nm InP HBT



500nm InP HBT



Transistor Output Characteristics: Idealized



Minimum voltage : V_{sat}

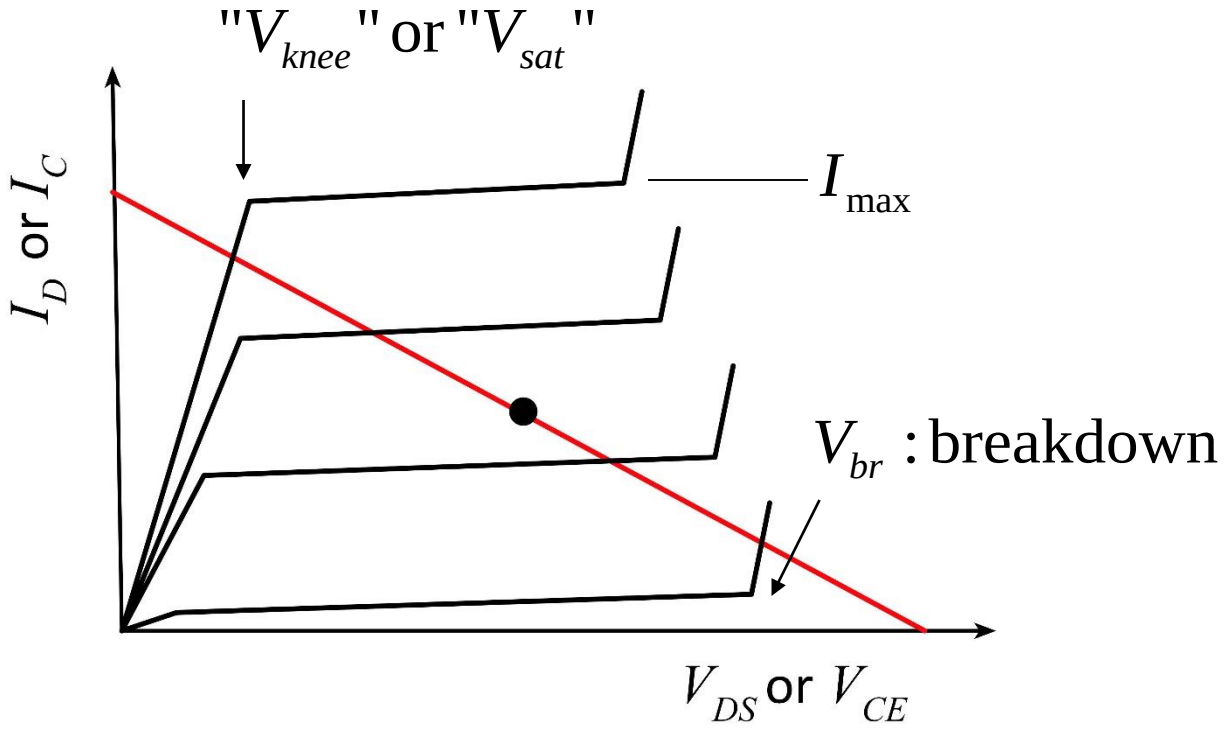
Maximum voltage : V_{br}

Maximum current : $I_{\max}$

FETs : $I_{\max} \propto W_g$, # gate fingers

bipolars : $I_{\max} \propto L_e$, # emitter fingers

Transistor Output Characteristics: Real



V_{br} varies with current

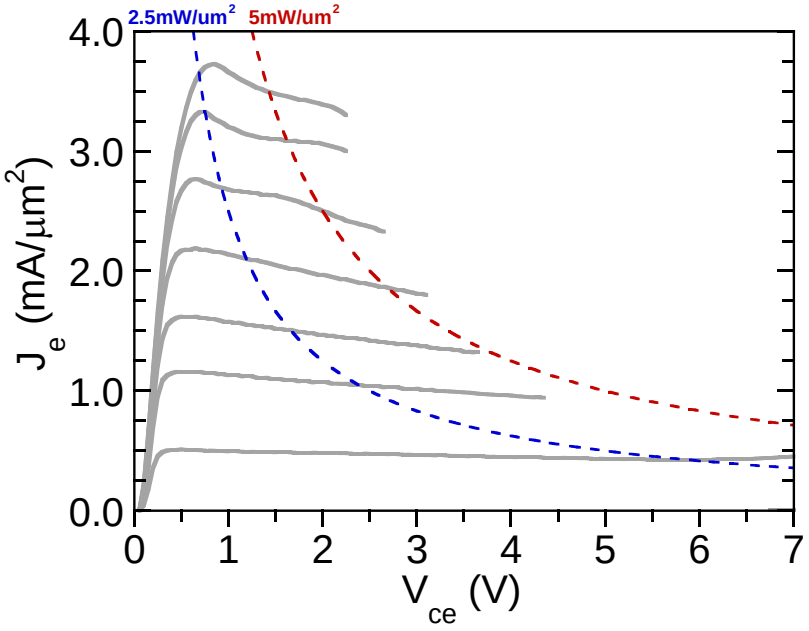
V_{sat} varies with current

Subsequent lecture notes are therefore somewhat idealized

Transistor Output Characteristics: Power

Transistor power $= V_{ce} I_c$ or $V_{DS} I_D$

Constant power : hyperbola on I_{out}, V_{out} plane



Case 1 : low - frequency power amp

frequency << (thermal time constant)$^{-1}$

$\rightarrow$ loadline must lie below maximum power density curve

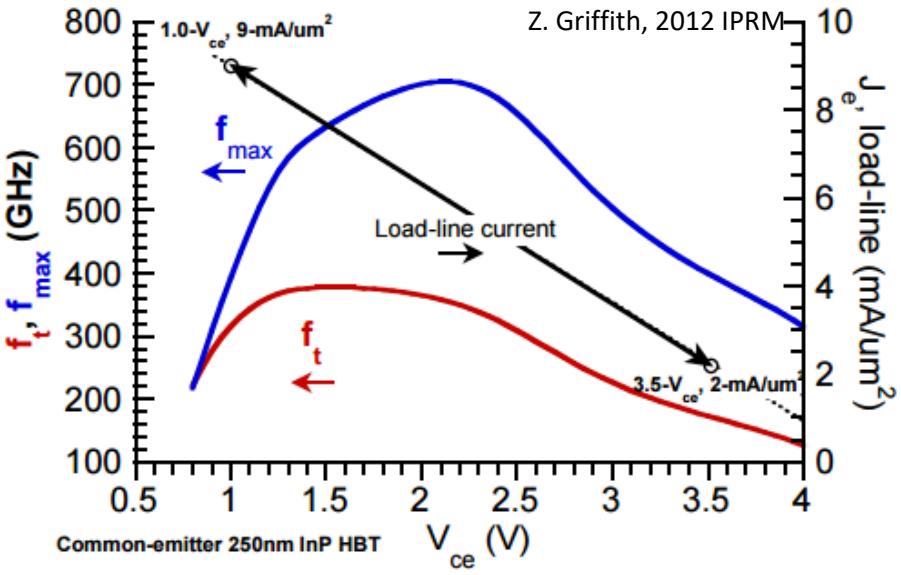
Case 2 : high - frequency power amp

frequency >> (thermal time constant)$^{-1}$

$\rightarrow$ *bias point * must lie below maximum power density curve

Device Bandwidth vs Operating Point

bipolar transistors :



Low voltage, high current :

"Kirk effect" = space - charge - limited current

reduction in ft, increase in Ccb $\rightarrow$ reduced bandwidth

High voltage :

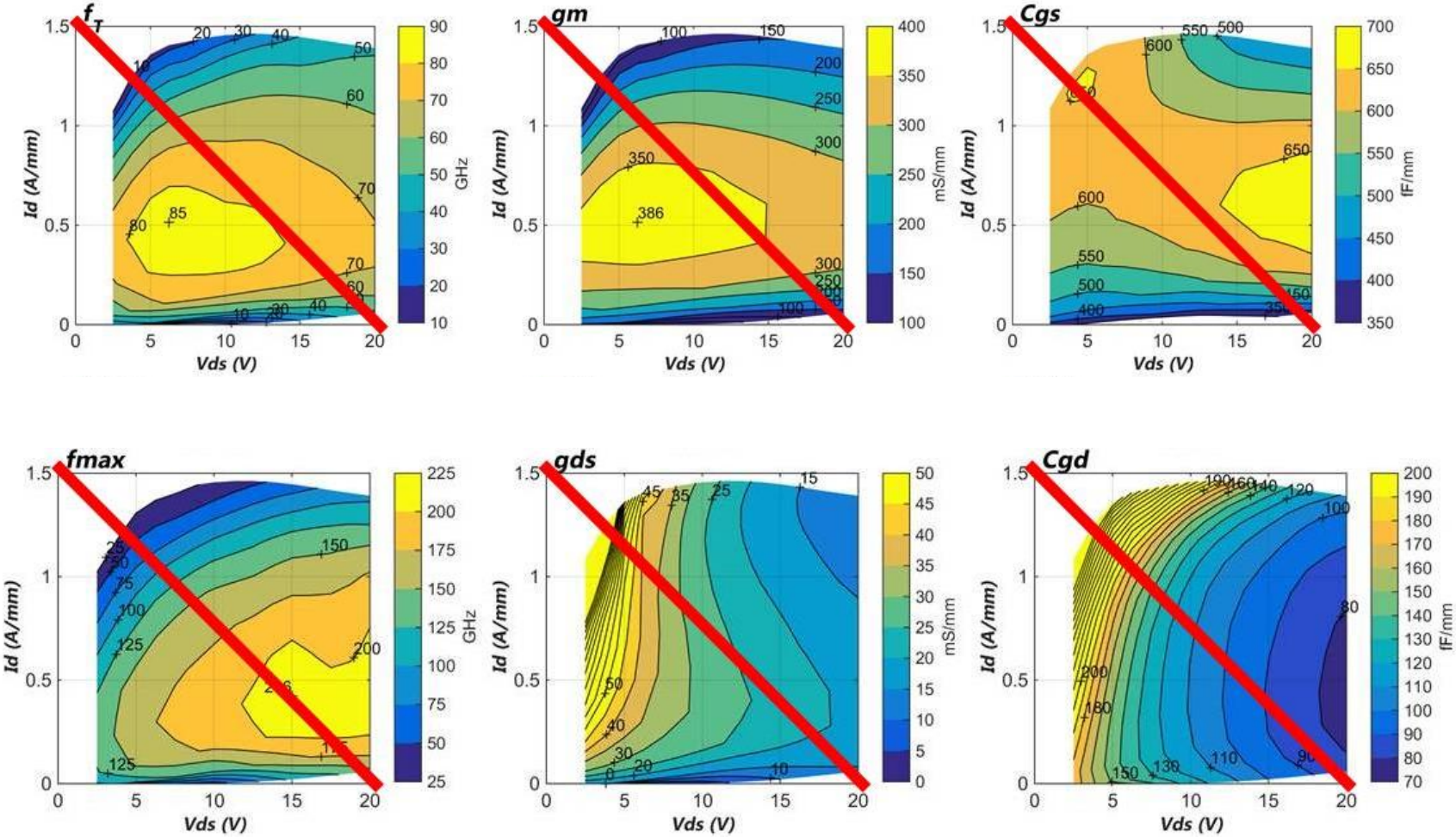
all semiconductors : push - out of collector depletion region

III - V semiconductors : reduction of electron velocity in collectror

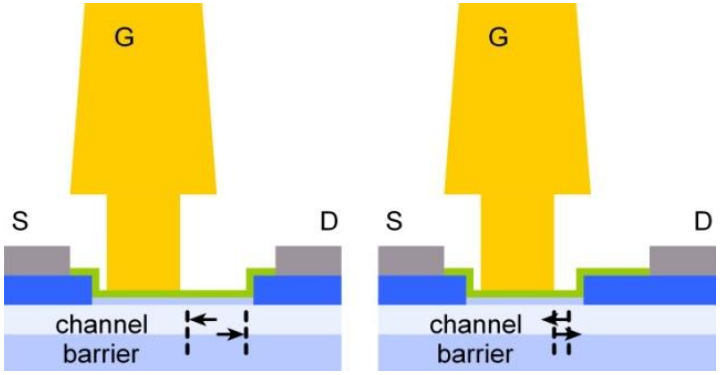
reduction in ft, * de * crease in Ccb $\rightarrow$ reduced bandwidth

Device Bandwidth vs Operating Point: FETs

Variations of g_m, C_{gs}, f_τ, over loadline.



Device Bandwidth vs Operating Point: FETs

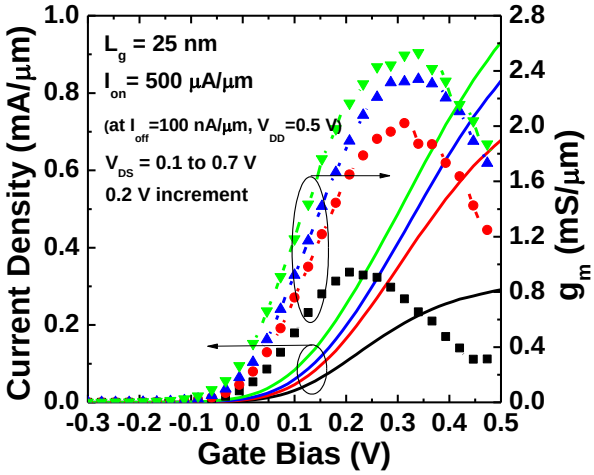


Increased drain bias $\rightarrow$ increased drain depletion

$\rightarrow$ increased transit time, decreased C_{gd} , decreased G_{ds}

Also : variation of g_m with current.

Low at both low currents and high currents



Operating areas

Safe operating area

standard terminology

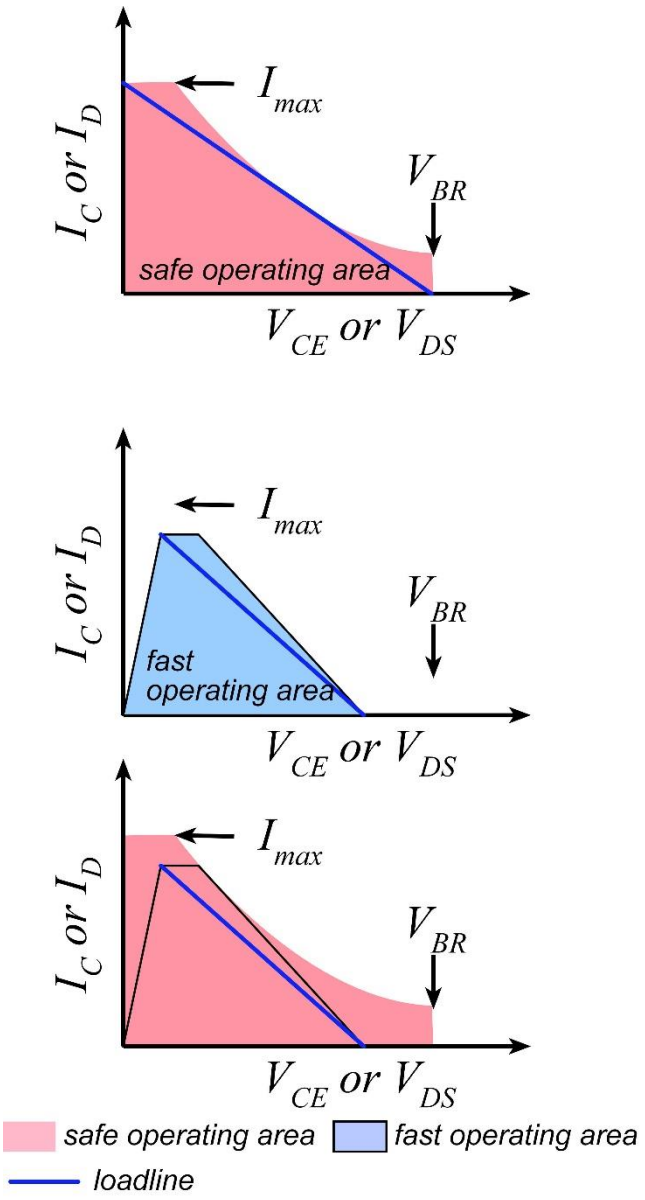
region bounded by power, V_{br}, $I_{\max}$

fast operating area

not standard terminology

region with adequately high f_t, $f_{\max}$

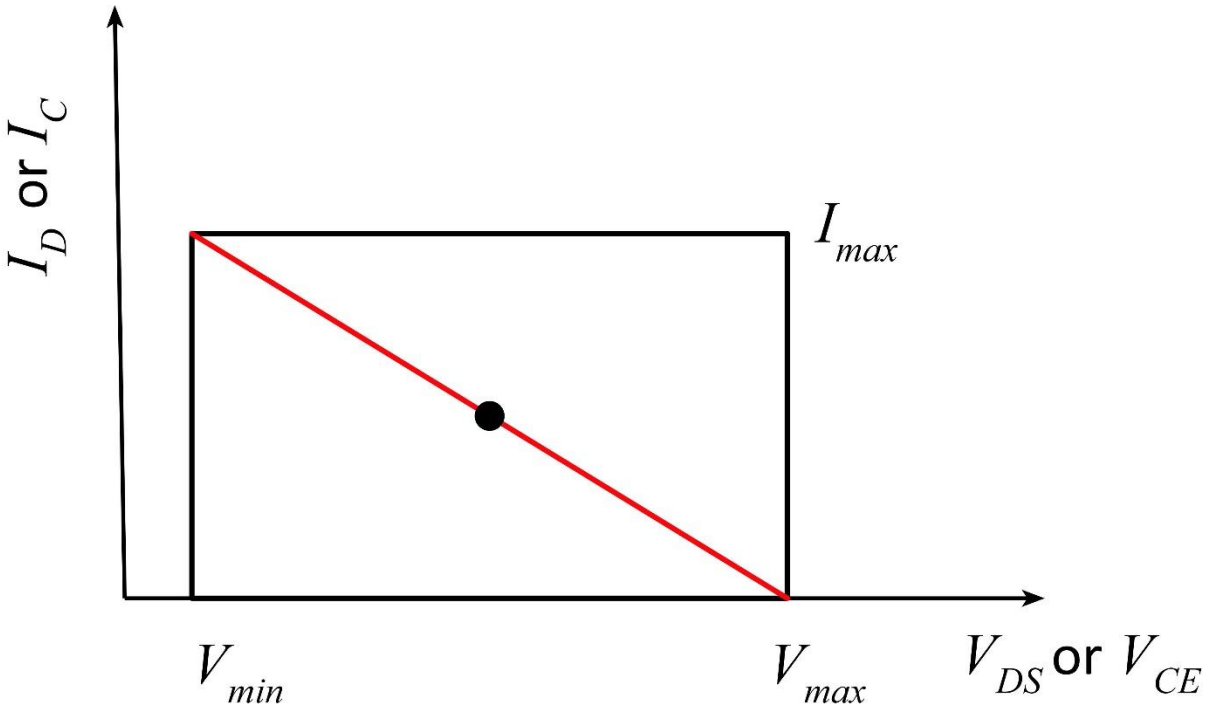
Loadline must lie within both



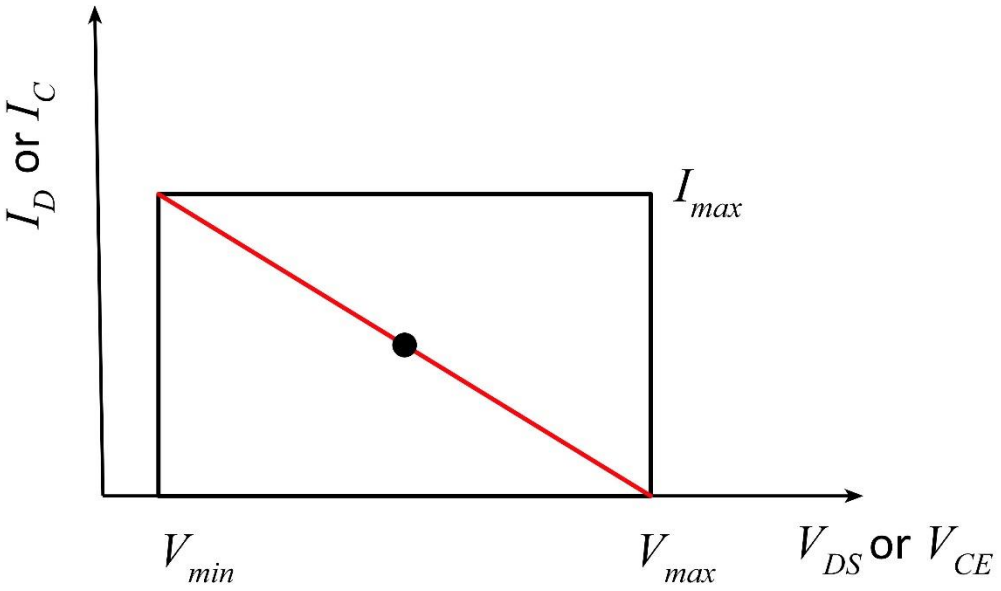
Oversimplified SOA/FOA; for class

Maximum, minimum voltages

Maximum current $\propto W_g$ or L_E



Simple class A power analysis



Bias point in center of rectangle.

Loadline reaches corners of rectangle

$$Z_L = (V_{\max} - V_{\min}) / I_{\max}$$

$$P_{DC} = V_{DC} I_{DC} = (V_{\max} + V_{\min}) I_{\max} / 4$$

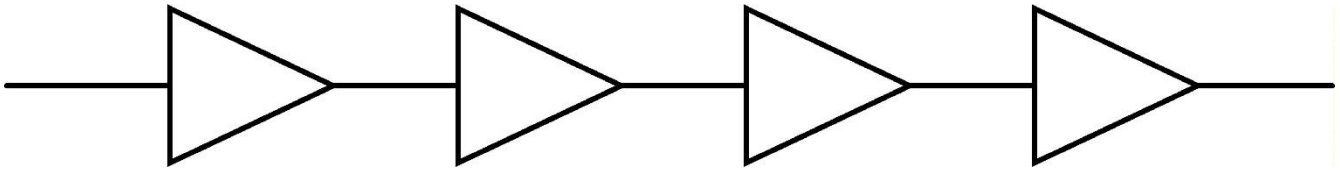
$$P_{RF,\max} = (V_{\max} - V_{\min}) I_{\max} / 8$$

$$\text{maximum drain/collector efficiency} = \eta_{\text{drain/collector}} = P_{RF,\max} / P_{DC} = 1/2$$

Power-added efficiency

$$\text{P.A.E.} \equiv (P_{out} - P_{in}) / P_{DC}$$

$$= \frac{P_{out}}{P_{DC}}\left[1 - \frac{P_{in}}{P_{out}}\right] = \eta_{\text{drain/collector}} \cdot \left[1 - \frac{1}{\text{gain}}\right]$$



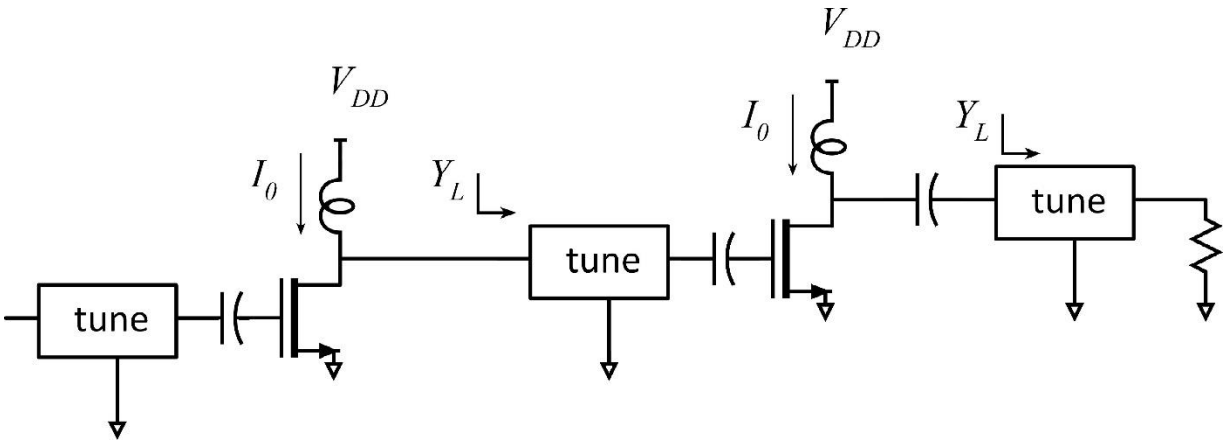
Noting that Pout for one stage is Pin for the next,

if we have a chain of PAs with identical PAE,

at that specific operating RF power, then

the PAE of the cascade will be that of the individual PAs.

Power Amplifier Design



For highest efficiency, each stage should be loaded with

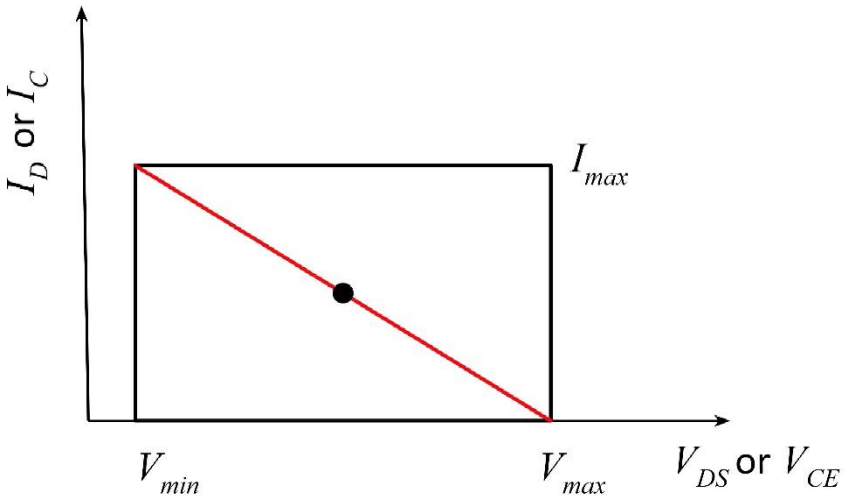
$$Z_{L,opt} = (V_{\max} - V_{\min}) / I_{\max}$$

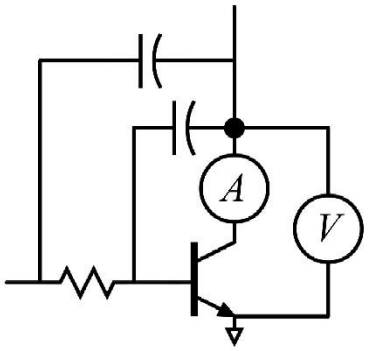
The interstage networks are tuning networks,

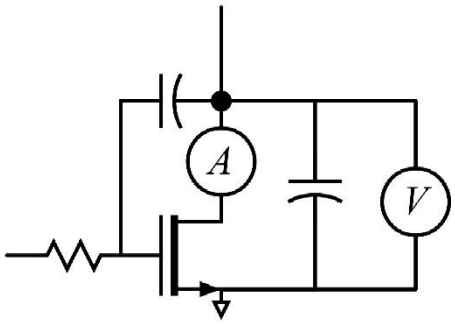
not matching networks.

Thus far, we have neglected transistor parasitics.

Loadline: inclusive of transistor parasitics







Transistors have resistive, capactive parasitics.

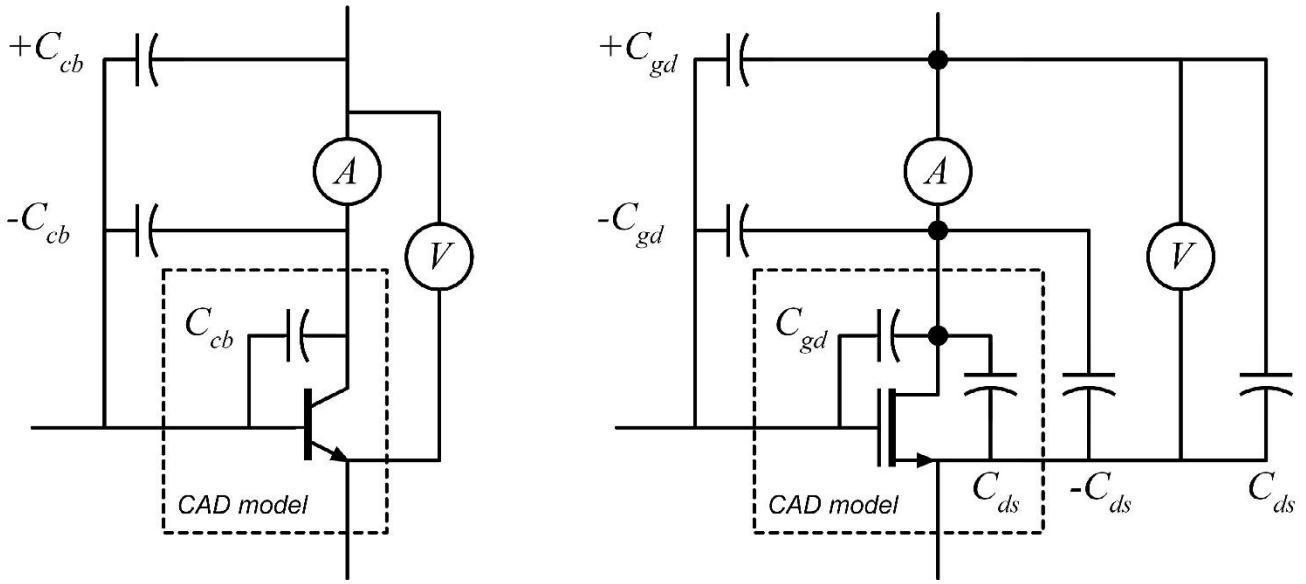
It is the *internal* (I_C, V_{CE}) or (I_D, V_{DS}) which must follow the above loadline.

Loadline current must be electron current, not $C \cdot dV / dt$ displacement current.

Current meters must be placed inside the capactive parastics.

How do we do this ?

Loadline: inclusive of transistor parasitics



Read the CAD device model → determine transistor capacitances.

Add external negative capacitances to cancel these.

Add voltmeter and current meter.

These correctly measure the loadline

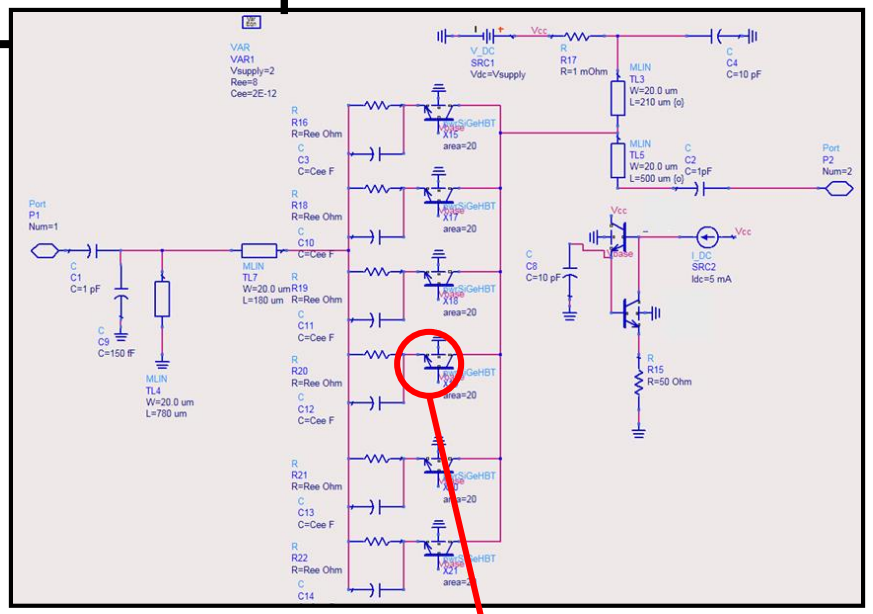
Then add external positive capacitances.

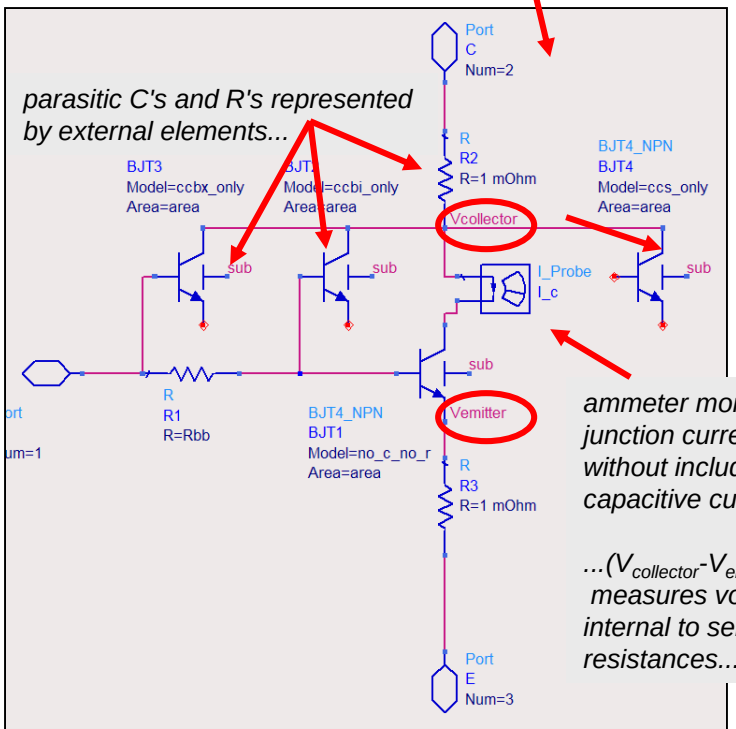
Example of ammeter, voltmeter placement

Here I took the CAD model and

1) created a variant with zero C_{cb}, zero $C_{c,sub}$
2) used this for the active transistor model.
3) created a second variant with C_{cbi} only
4) created a third variant with C_{cbx}only.

In this manner, voltage variation of the capacitances is correctly accounted for.





Power Amplifier Methodology

The above technique, direct loadline method

known as the Cripps technique

requires that you know, add, subtract capacitances.

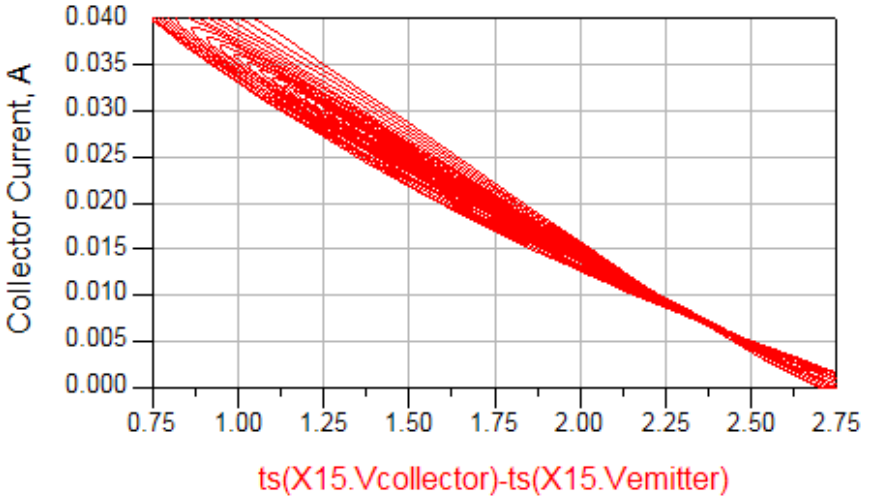
Alternate techniuque : load pull contours

Empirical, not analytical

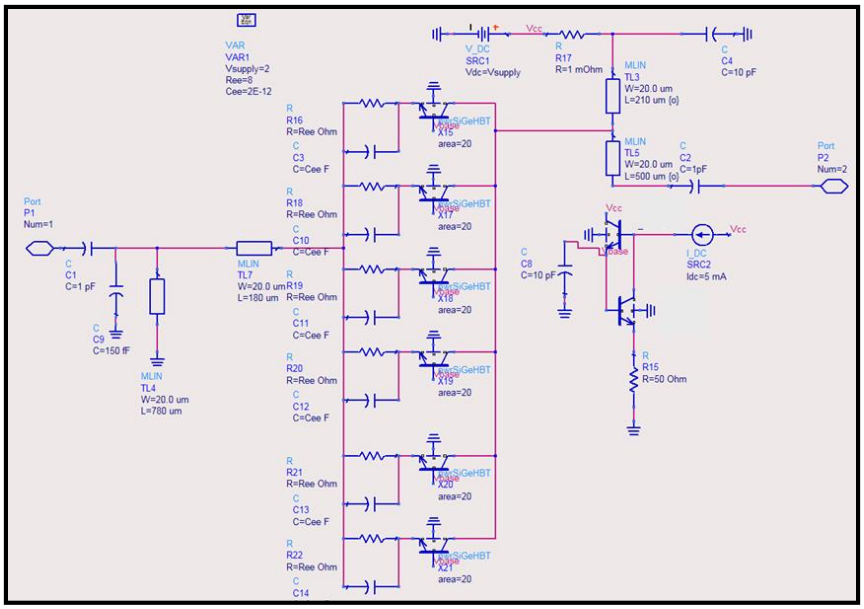
will cover in a few slides

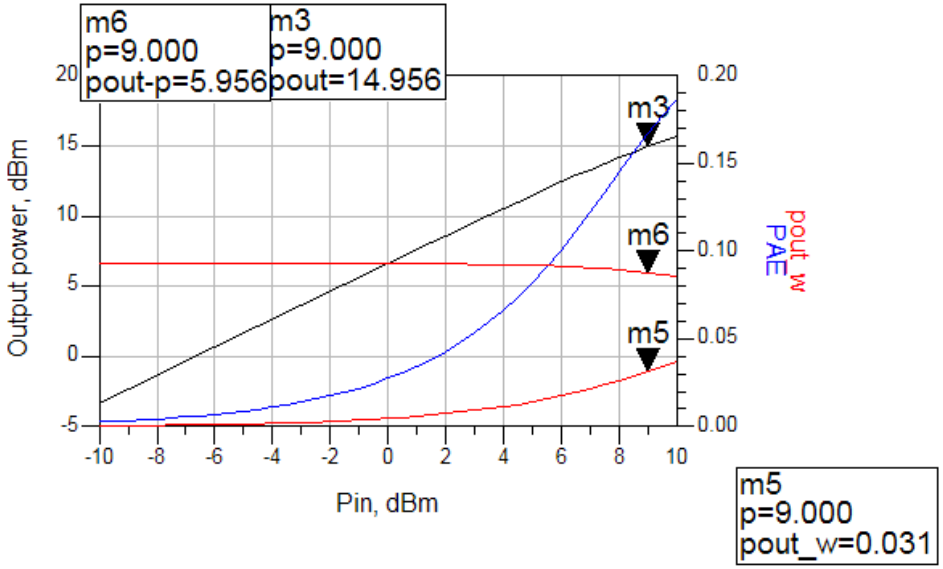
Power Amplifier Design (Cripps Method)

Design steps are
1) input stabilization (in-band)
2) output tuning for correct load-line
3) input tuning (match)
4) out-of-band stabilization



Example: 60 GHz, 30 mW PA, 130 nm BiCMOS

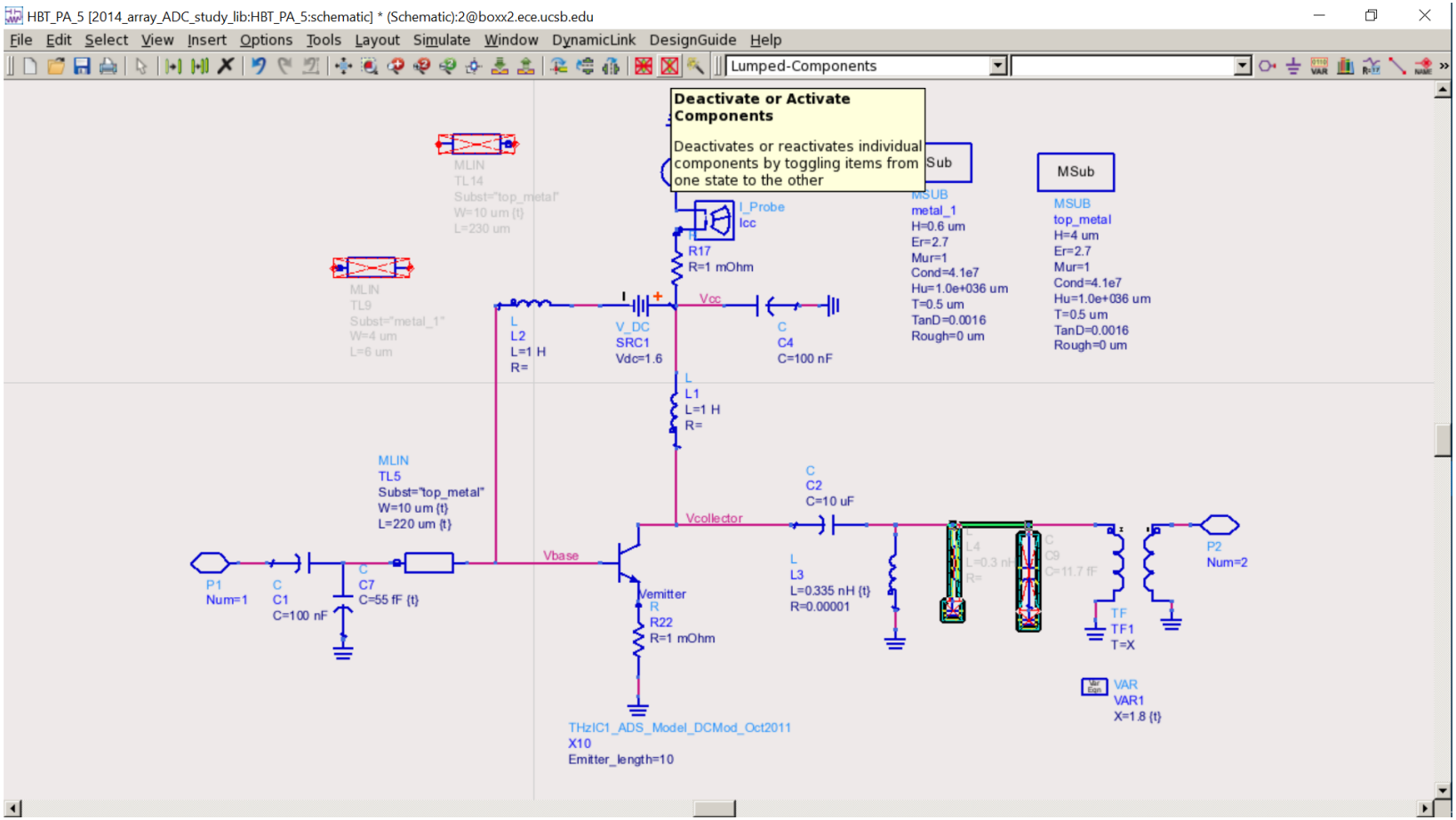




Power Amplifier Design Example

Power amplifier *cell*. 20 micron emitter finger.

bias : Ic = 10mA, Vcb = 1.86 Volts $\rightarrow V_{CE} = 2.5V$.



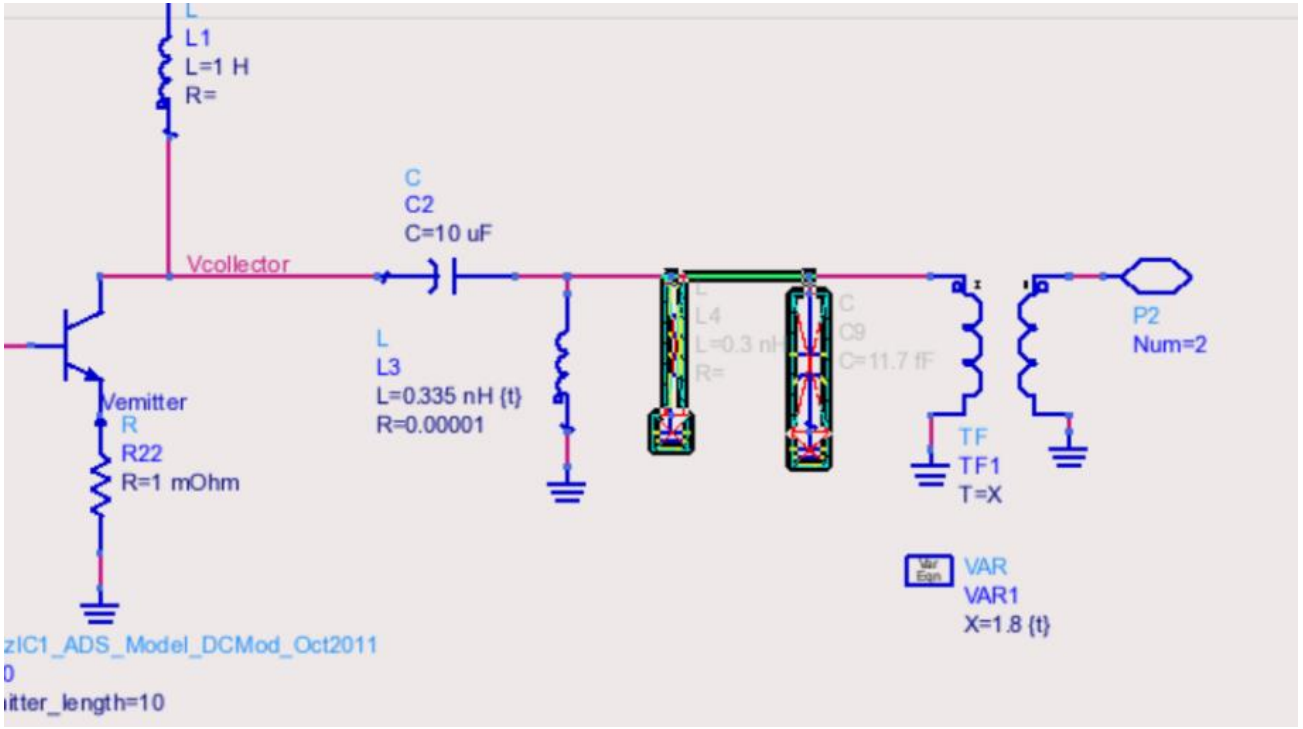
The biasing technique used is just for CAD experimentation; not practical

The inactivated output LC network is a bandpass filter

Power Amplifier Design Example

First, simulate the transistor vs frequency at the bias point,
determine fmax, MAG/MSG at the design frequency.
determine the stability factor at the design frequency
if unstable, stablize (input network) at the design frequency

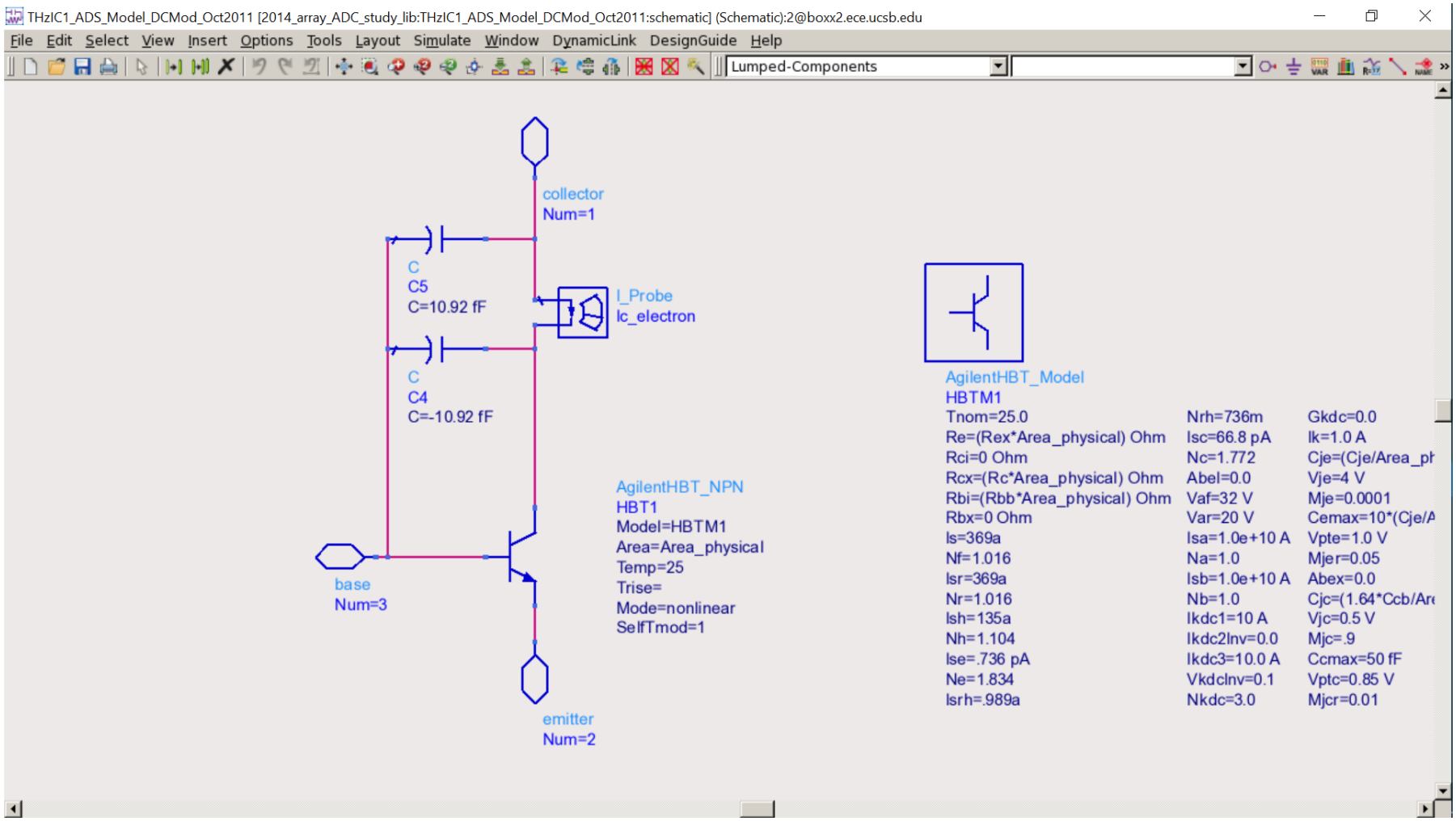
PA example: output network



Note the output network : ideal transformer plus parallel inductance.

This is not the final ouput network : it is used to quickly find $Y_{L,opt}$.

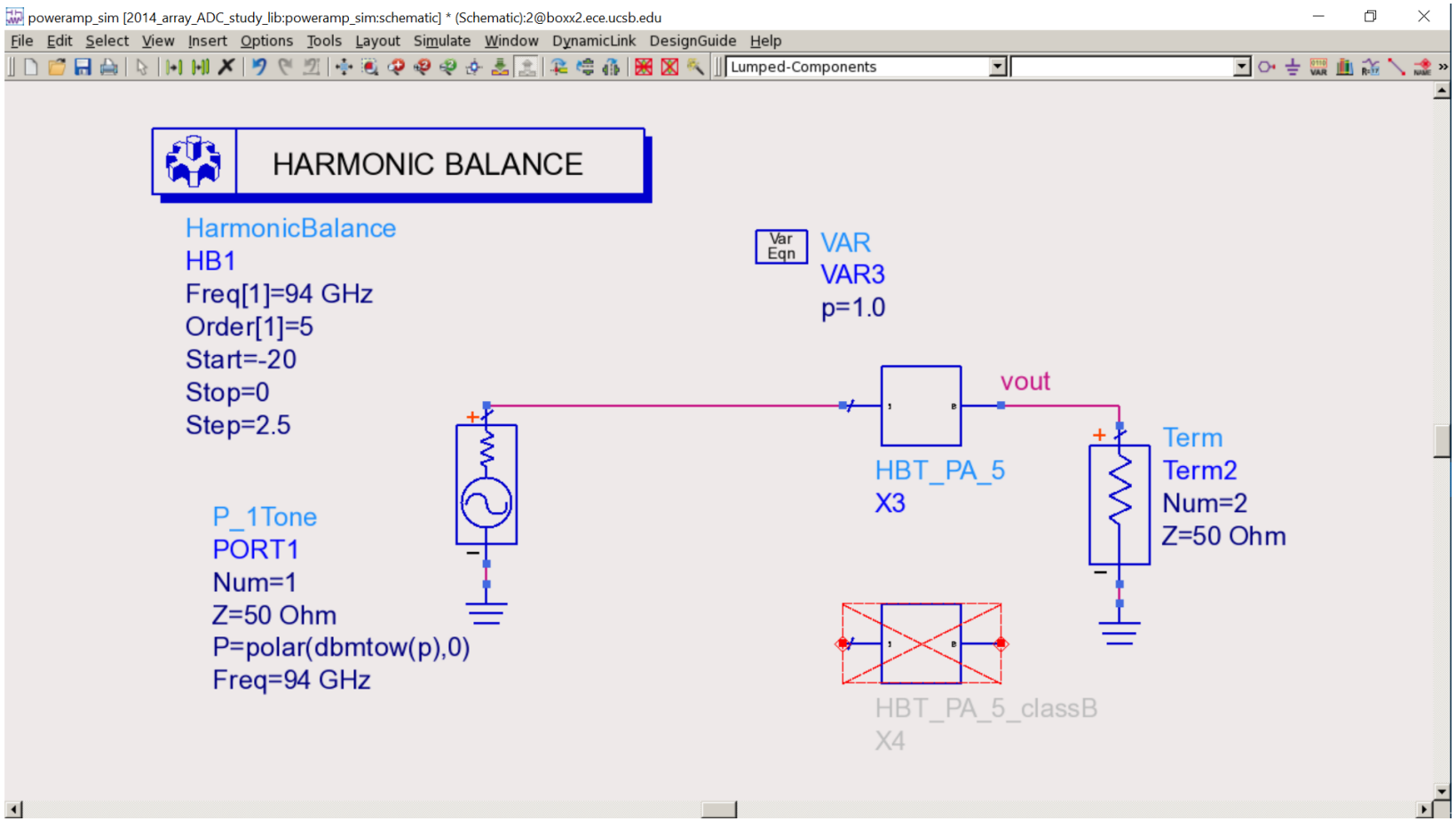
PA example: measuring the loadline



Dropping down in the heirarchy into the device model,

we see the monitoring ammeter plus negative and positive Ccb.

PA example: finding the optimum load



The input is not yet matched, and the load is not yet tuned.

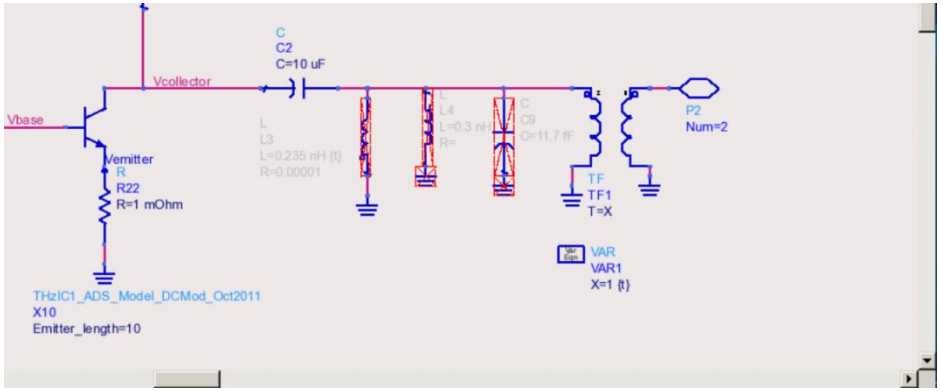
We drive the transistor with a large drive signal

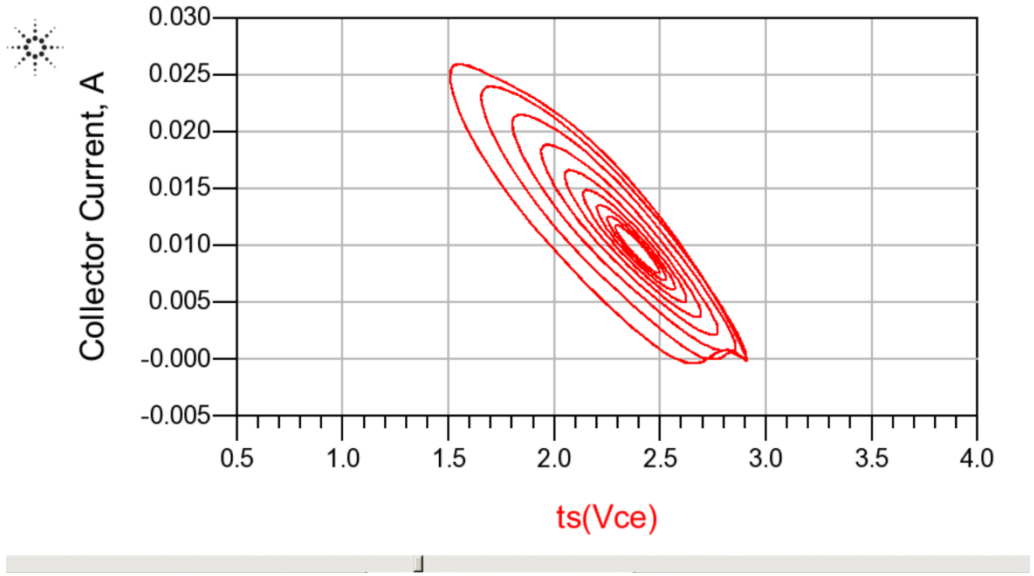
and observe the loadline

Power Amplifier Design Example

With no inductive tuning, and with a 1:1 transformer ratio,

The loadline initially looks like this :

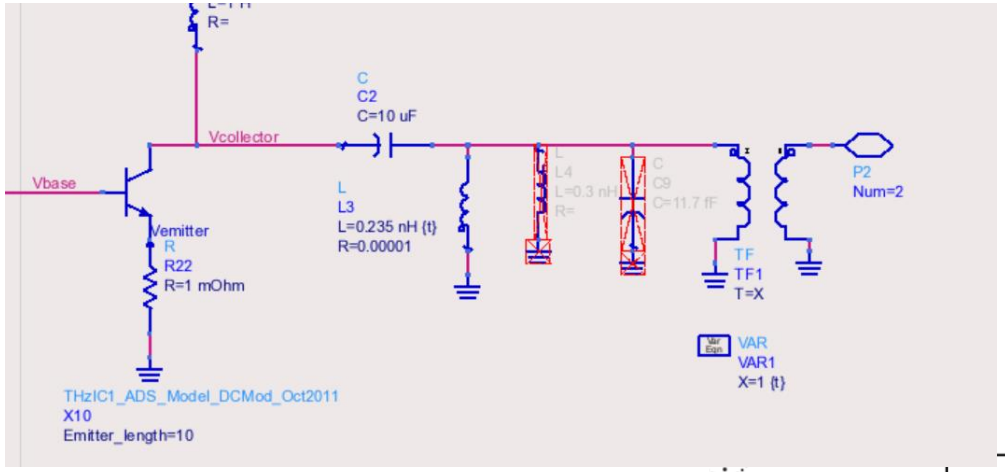


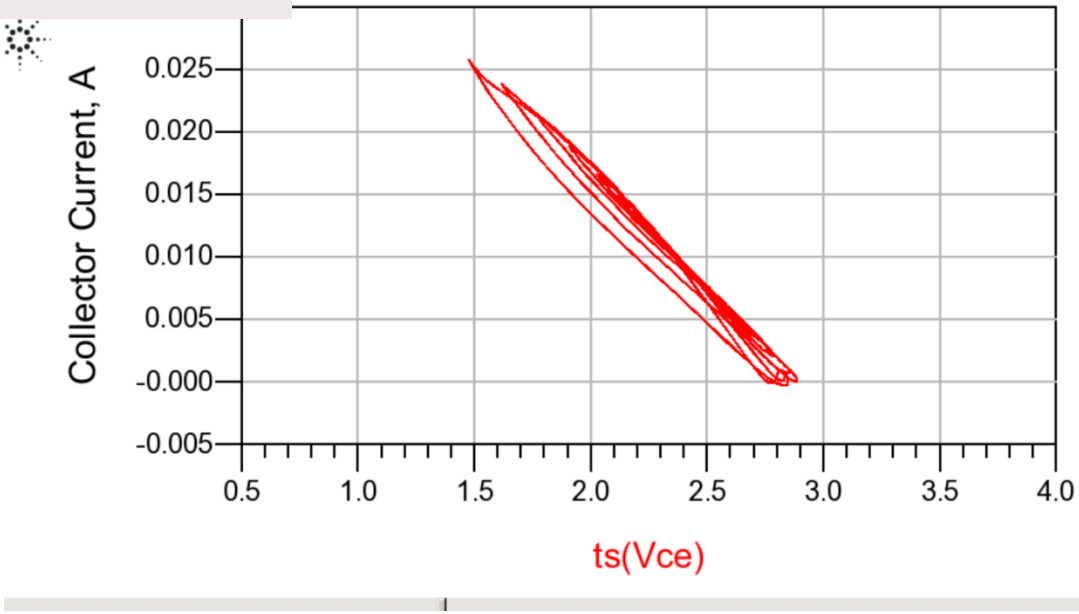


Power Amplifier Design Example

First add the inductive tuning, adjusting the shunt L

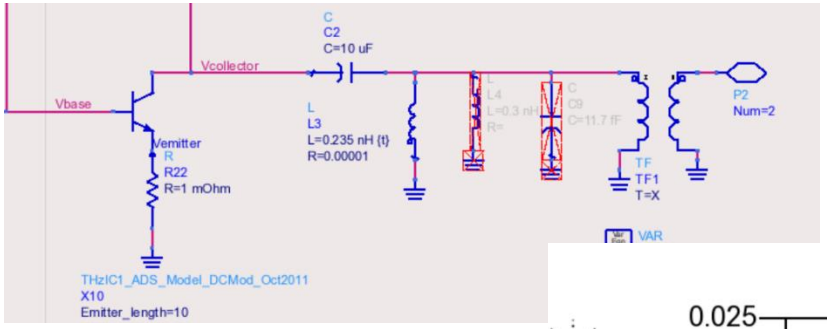
to eliminate loadline looping

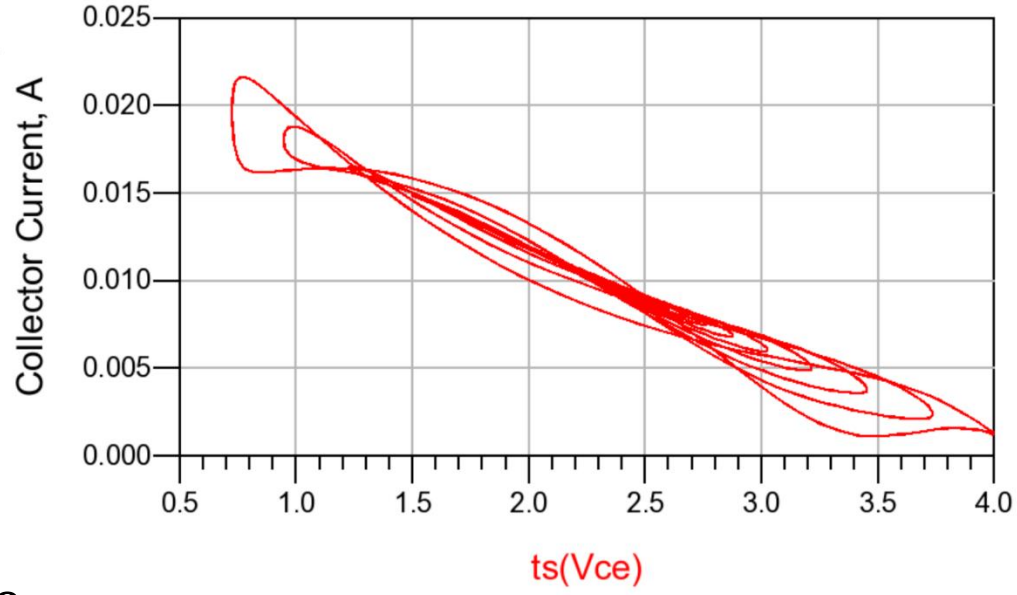




Power Amplifier Design Example

Then adjust the tnansformer ratio to obtain a loadline passing through the target endpoints $(V_{\min}, I_{\max})$ and $(V_{\max}, I_{\min} = 0A)$





We had expected a straight line.

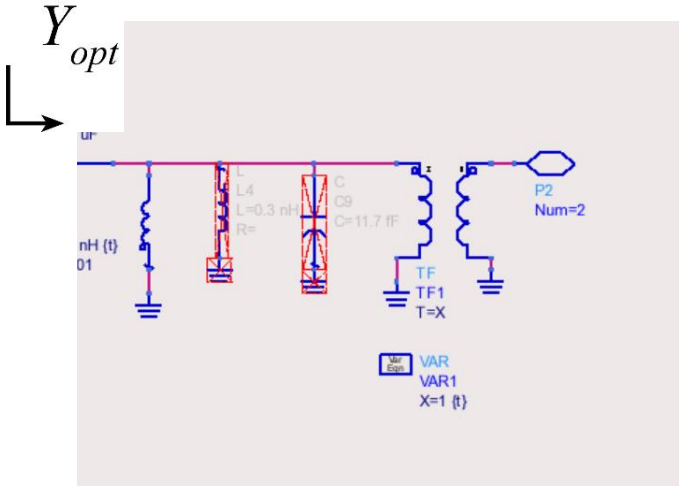
The looping (3 per cycle) is 3rd harmonic generation

Power Amplifier Design Example

We have now determined Y_{opt}.

We then (not shown), in a separate circuit simulation file, design a practical output network which provides Y_{opt}.

We then add this to the PA.



Power Amplifier Design Example

Remaining steps :

Input matching network

Out - of - band stabilization

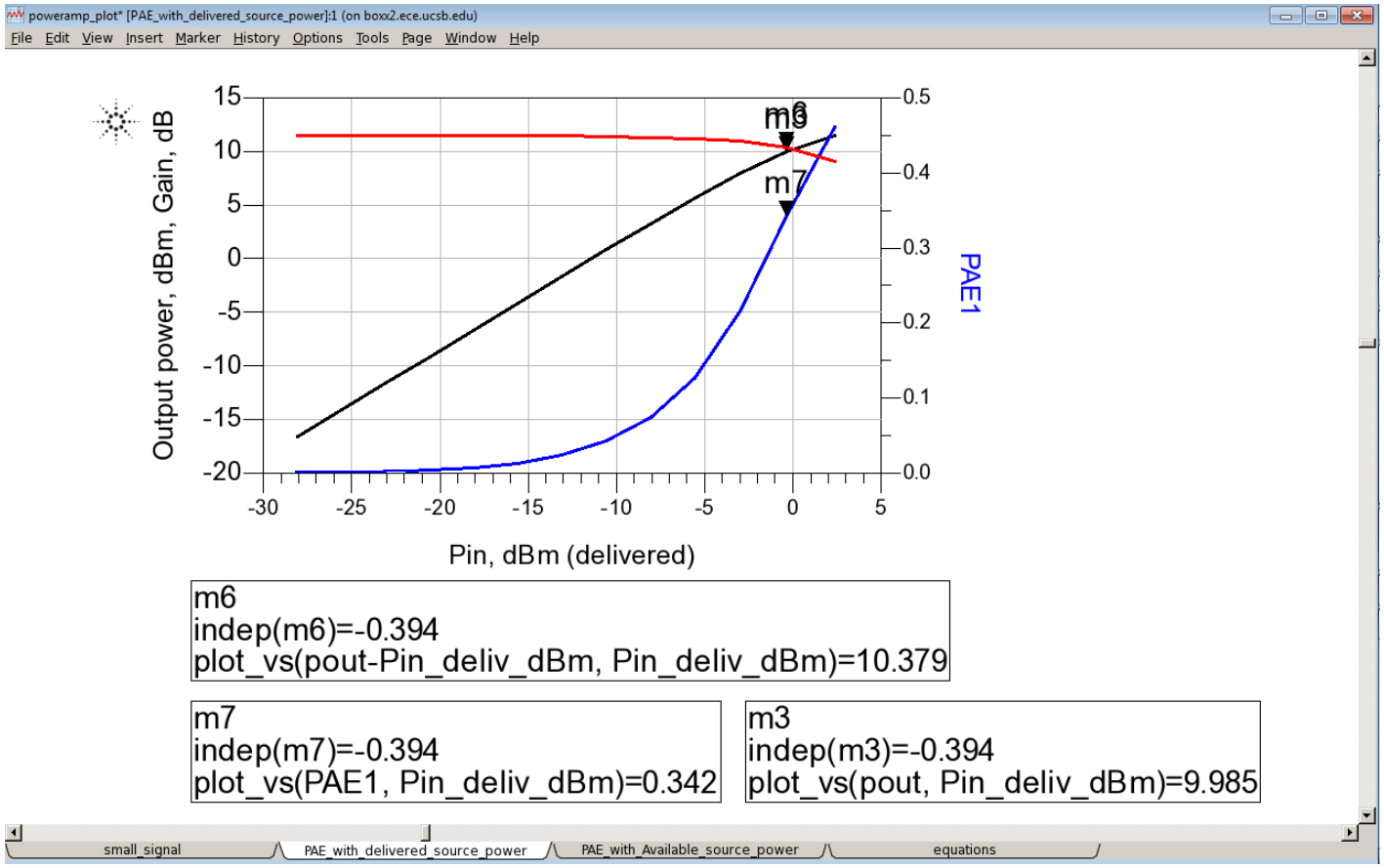
(ece145a)

Often : filters

to suppress 2nd, 3rd harmonics.

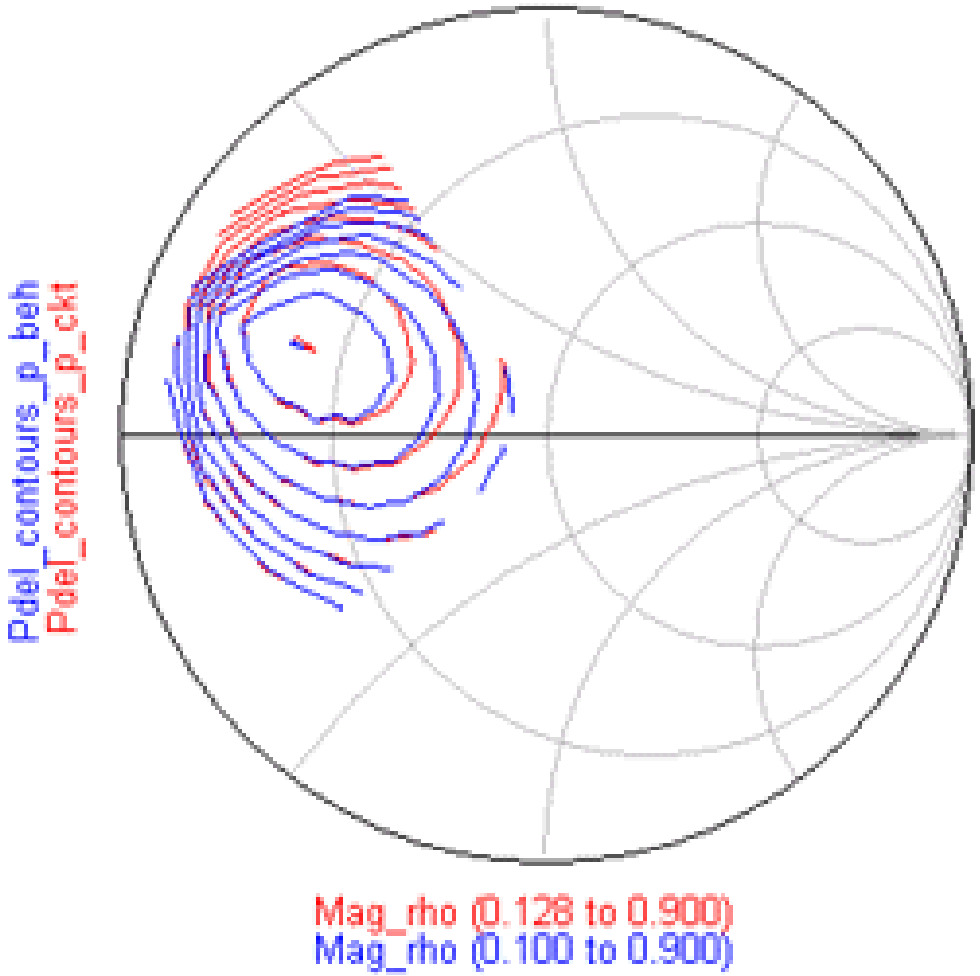
Power Amplifier Design Example

Here is our final simulated performance



Load pull method

We can also empirically determine (in CAD, or with instruments) the load impedance giving the largest saturated Pout. We then use this impedance for our PA design



Load pull method

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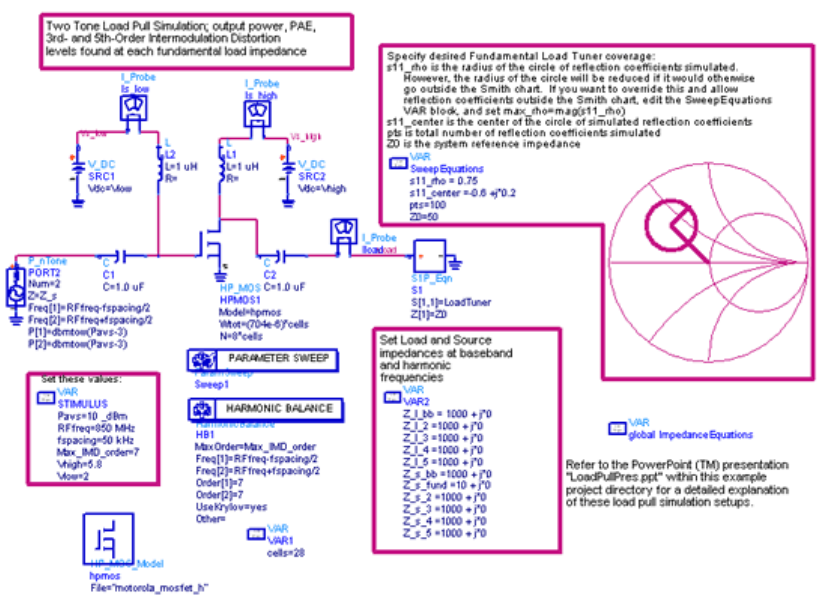
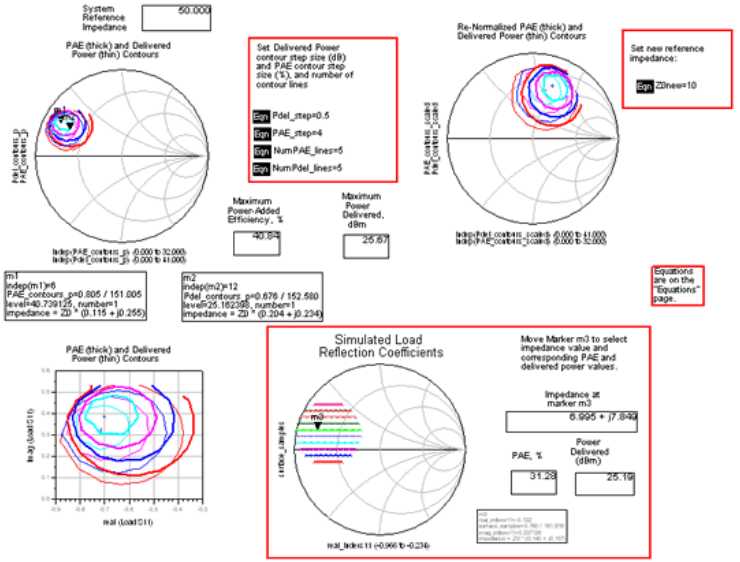




Keysight ADS has pre-configured test benches to do this.

I suspect that other CAD packages do, too.

I prefer the Cripps method.

The power-combiner problem

Output power : $P_{out} = (V_{\max} - V_{\min}) I_{\max} / 8$

Necessary load impedance : $R_L = (V_{\max} - V_{\min}) / I_{\max}$

So, output power $P_{out} = (V_{\max} - V_{\min})^2 / 8R_L$

High-frequency transistors have low $V_{\max}$.

High P_{out} requires very low R_L,

or

High P_{out} requires *power-combining*

Minimum load impedance

Transmission lines have some minimum $Z_{line,\min}$.

See ECE145A notes :

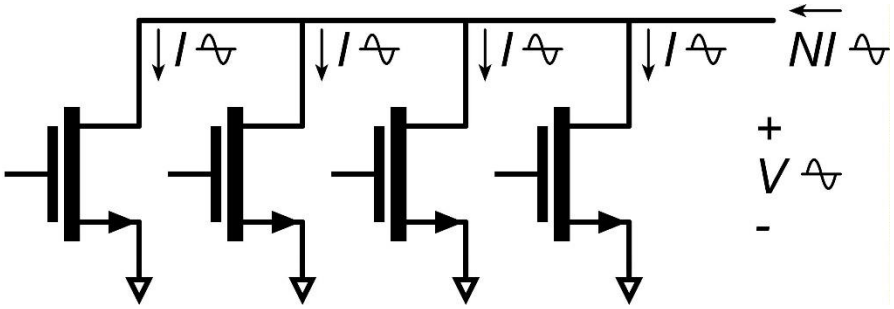
width, lateral modes, junction parasitics, high skin loss.

Impedance transformation permits $Z_{load} < Z_{line,\min}$

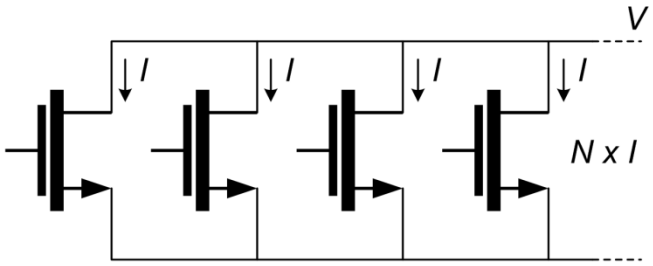
But high $Z_{load} : Z_{line,\min}$ ratios increase the line's VSWR

$\rightarrow$ increased line losses.

Z_{load} much below 10Ω will incur high losses



Parallel Power-Combining

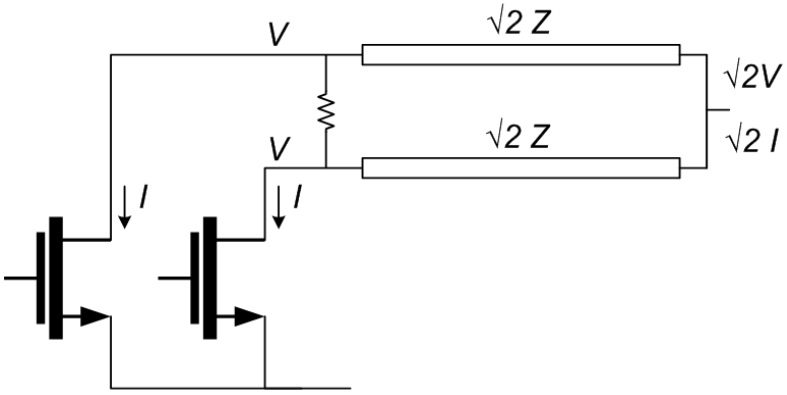


Output power: P_{OUT} = N x V x I

Parallel connection increases P_{OUT} ✓

Load Impedance: Z_{OPT} = V / (N x I)

Parallel connection decreases Z_{opt} ✗



High P_{OUT} → Low Z_{opt}

Needs impedance transformation:

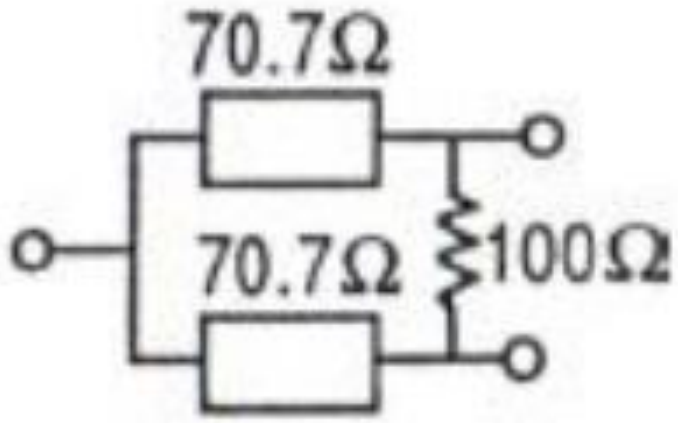
lumped lines, Wilkinson, …

High insertion loss ✗

Small bandwidth ✗

Large die area ✗

Wilkinson Power-Combiner



Lines are one quarter - wavelength

Does provide 2 : 1 combining, 50 Ohm ports.

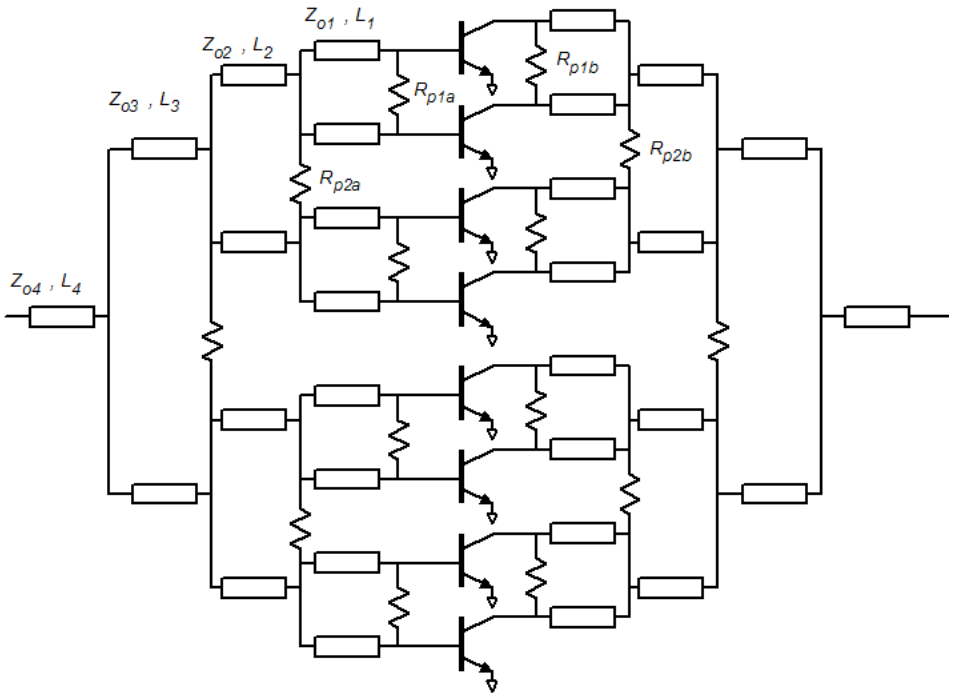
But :

Lines are long : large die area

Lines are long, hence lossy : loss in power, efficiency

from J Buckwalter's 145c notes

Corporate Wilkinson Power-combiner



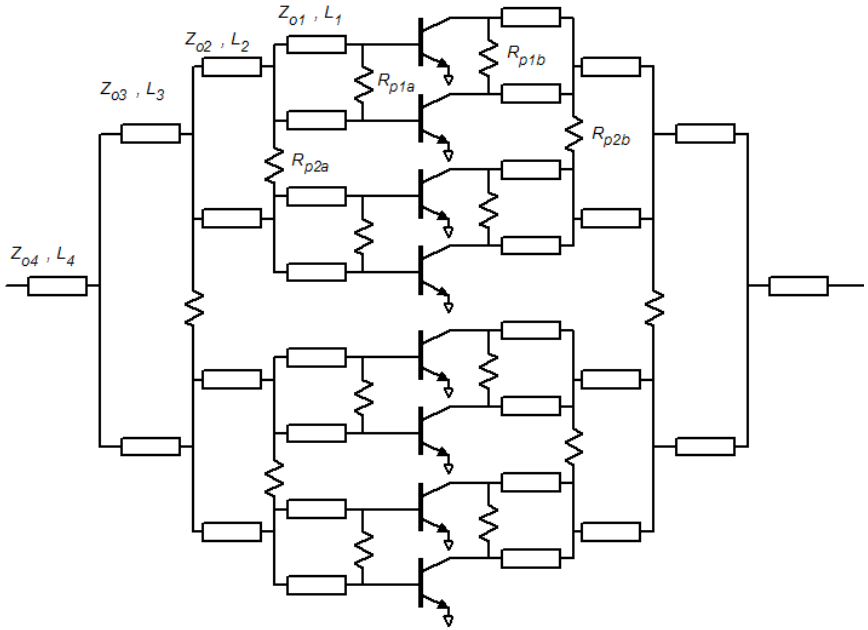
Assume : all these lines are $\sqrt{2} \times 50\Omega$ impedance

Assume : all these lines are quarter - wavelenght.

Then : this is a 3 - stage Wilkinson power - combiner

Then : we have 8 : 1 power - combining

Corporate Wilkinson Power-combiner



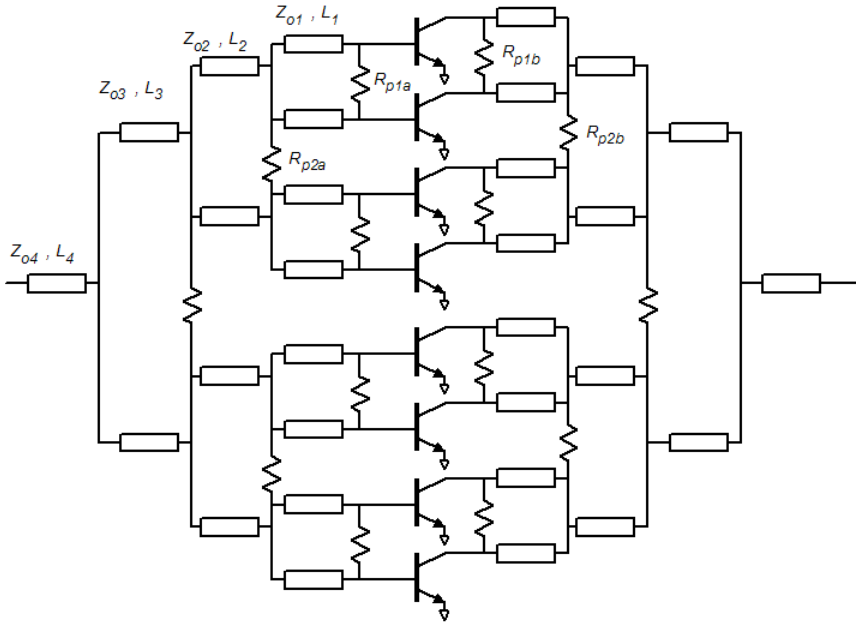
Corporate Wilkinson combiners are common in textbooks.

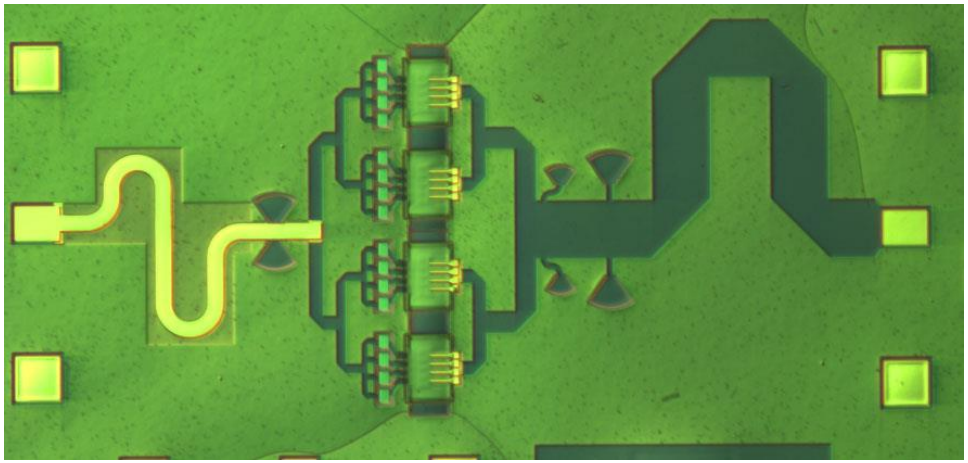
Corporate Wilkinson combiners are * rare * in ICs.

Why ?

Very long lines. Large die area. High losses

Corporate Power-combiners: Non-Wilkinson





Real IC power - combiners look like this.

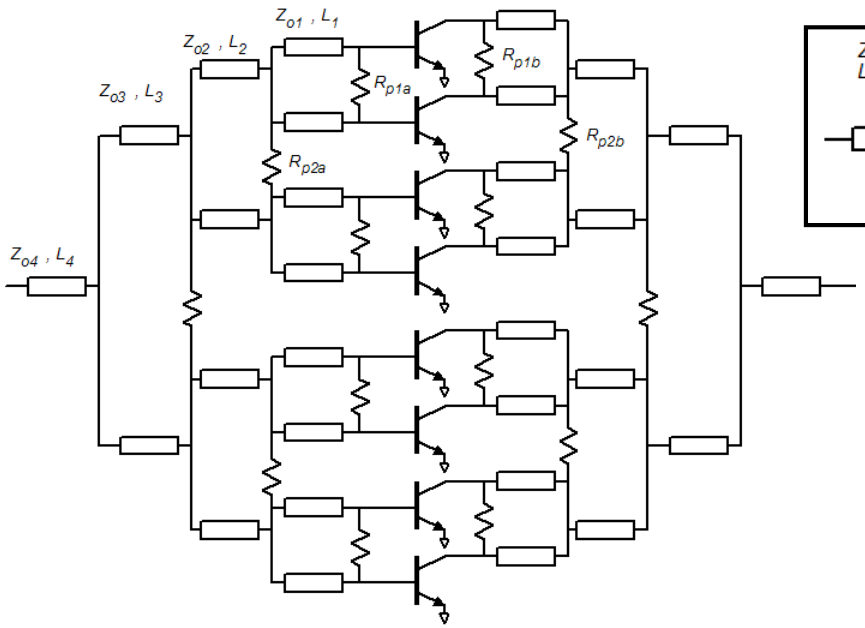
The structure is corporate.

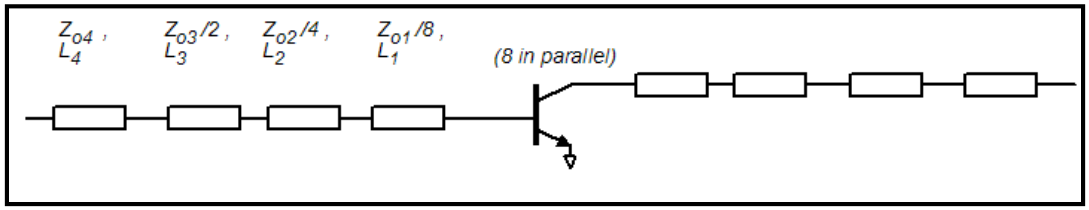
But, the lines are not 71 Ohms

And, the lines are much shorter than $\lambda_{\text{guide}} / 4$.

Shorter lines : less loss, smaller IC.

Design of Non-Wilkinson Combiners





Even-mode equivalent circuit

The equivalent circuit : a multi - section transmission - line transformer.

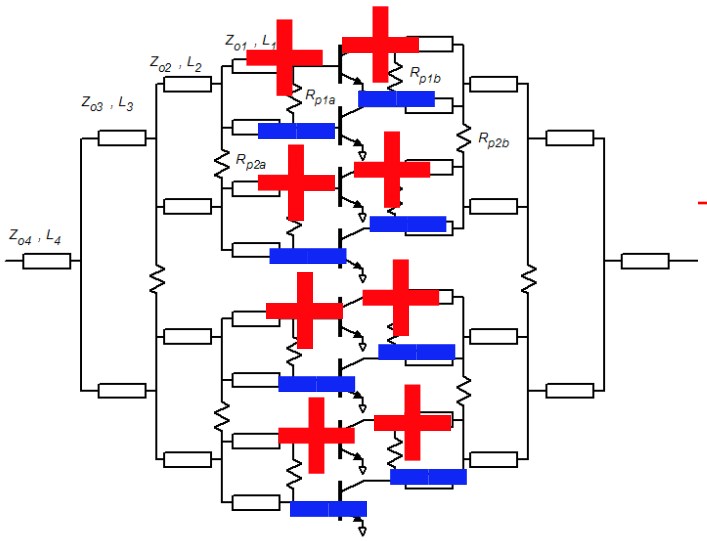
Shunt elements (inductors, capacitors) can also be added.

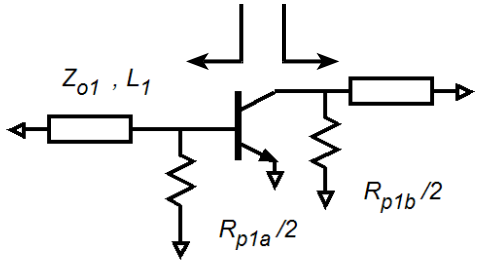
Line parameters are adjusted to reach $Z_{l,opt}$ and to match input.

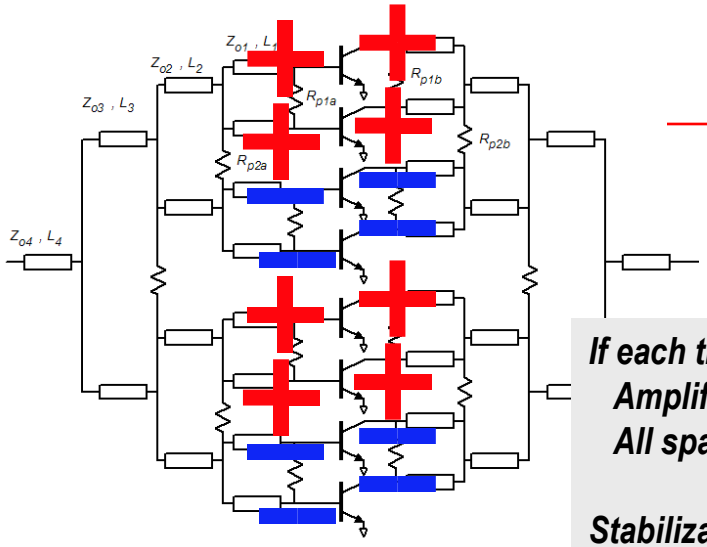
CAD approach :

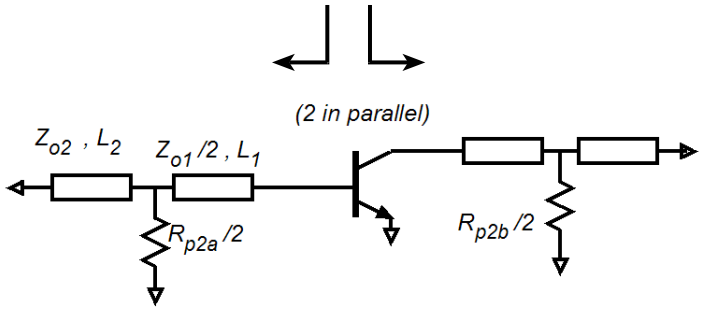
all similar lines defined by shared variables, simultaneously adjusted

Design: Multi-Finger Amplifiers: spatial mode instabilities







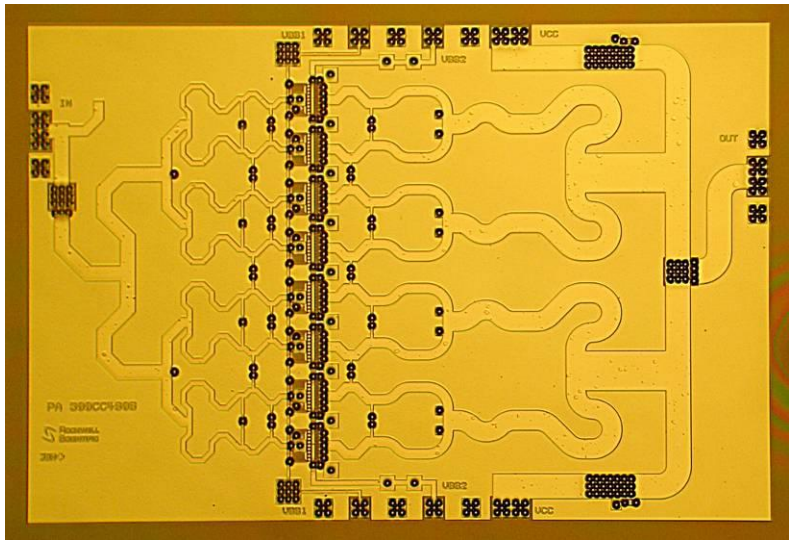


etc...

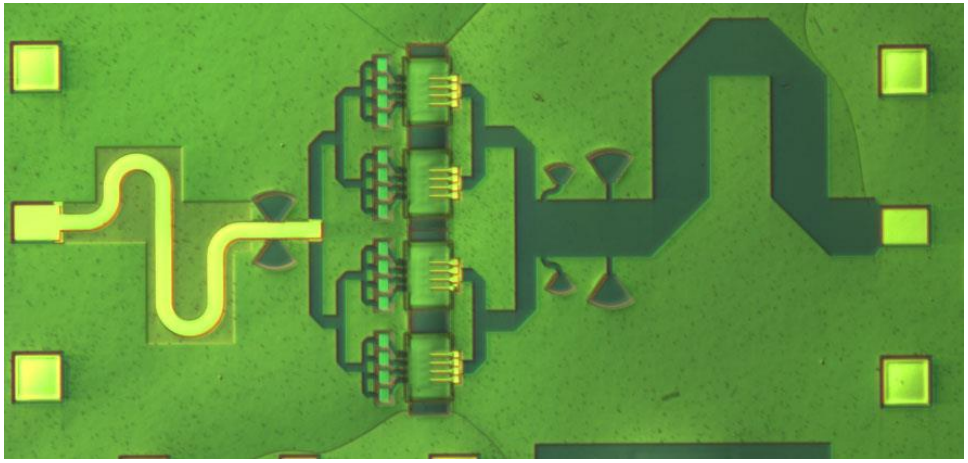
If each transistor finger is individually stabilized, high-order modes are stable.
Amplifier layout usually does not allow sufficient space for this.
All spatial modes must then be stabilized.

Stabilization method: bridging resistors → parallel loading to higher-order modes
Select so that (Z_S , Z_L) presented to device lie in the stable regions

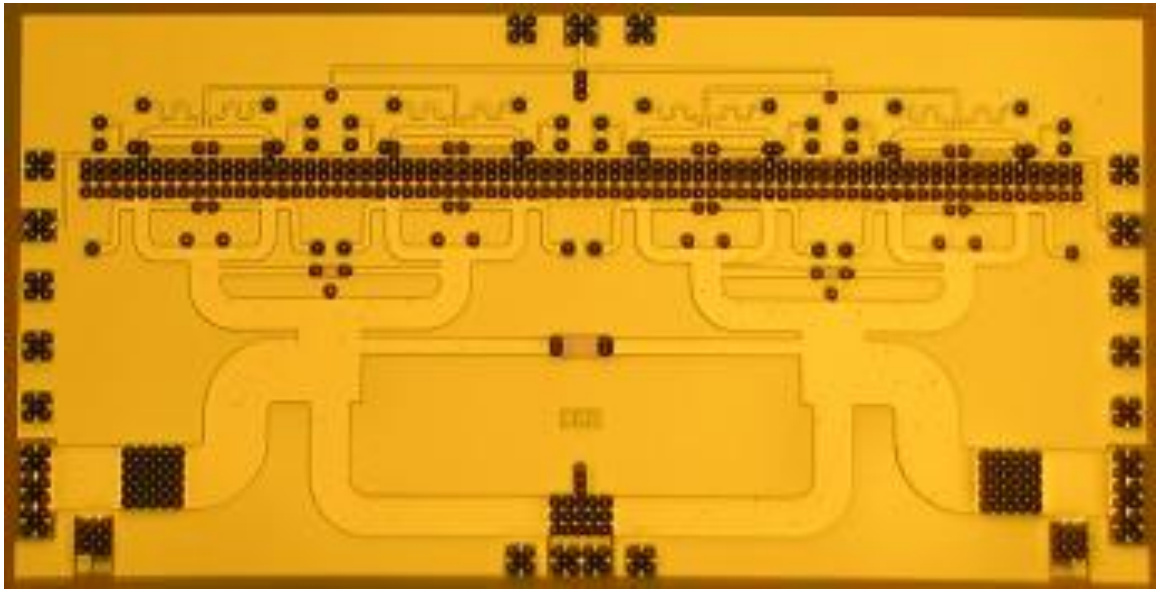
Examples: PAs with corporate combining



34 GH InP HBT power amplifier - Rockwell

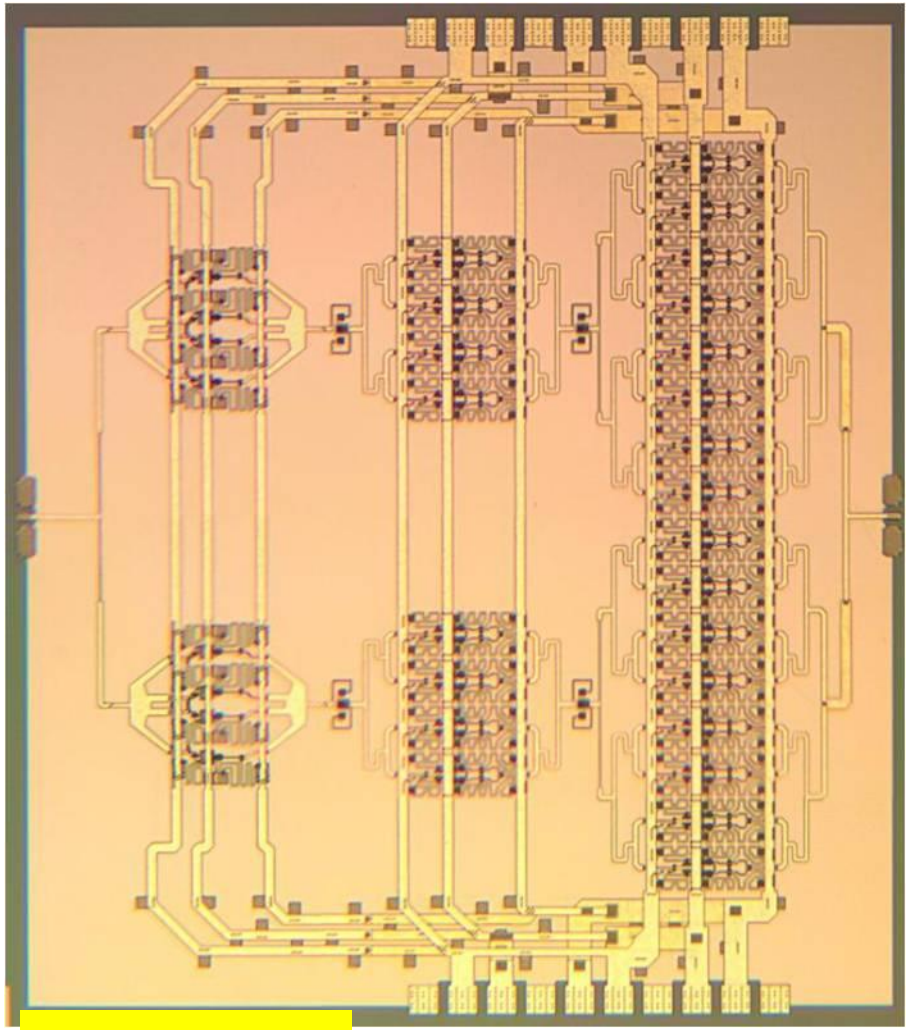


W-band InP HBT power amplifier - UCSB



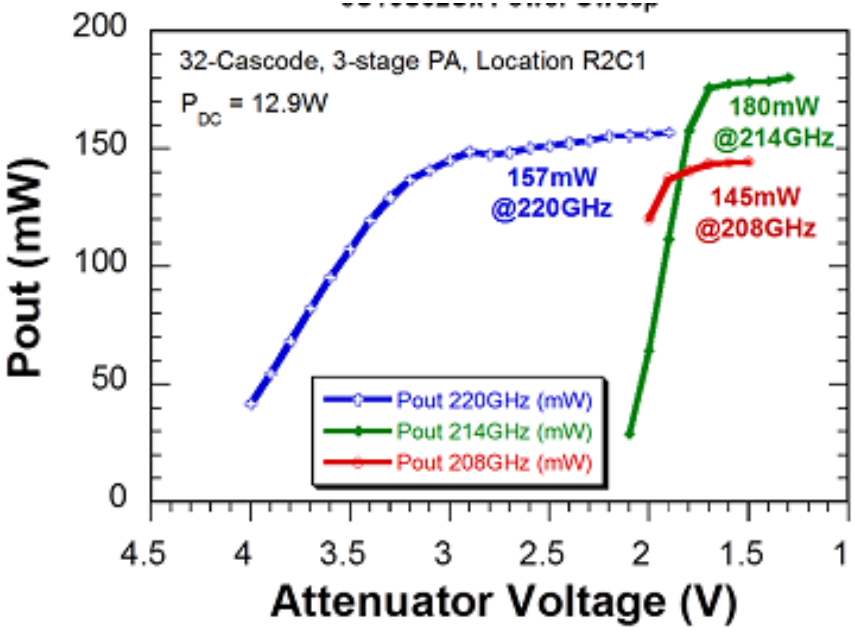
mm-wave InP HBT power amplifier - Rockwell

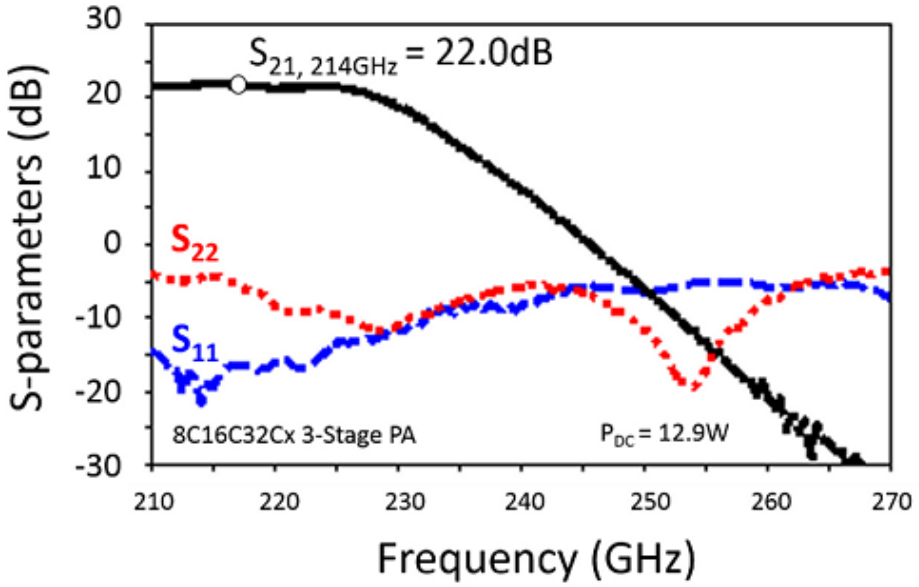
220 GHz 180mW Power Amplifier (330 mW design)



2.3 mm x 2.5 mm

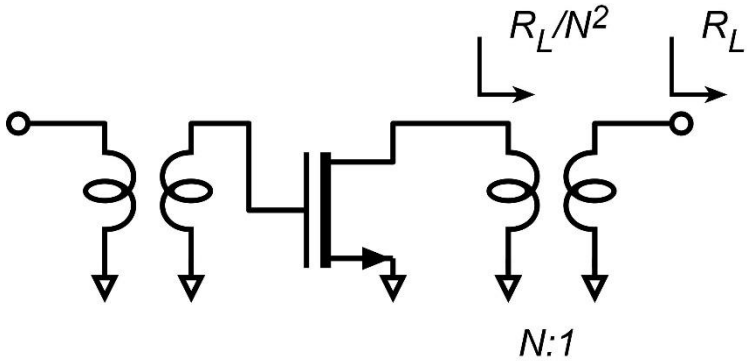
T. Reed, Z. Griffith et al
2013 CSIC symposium





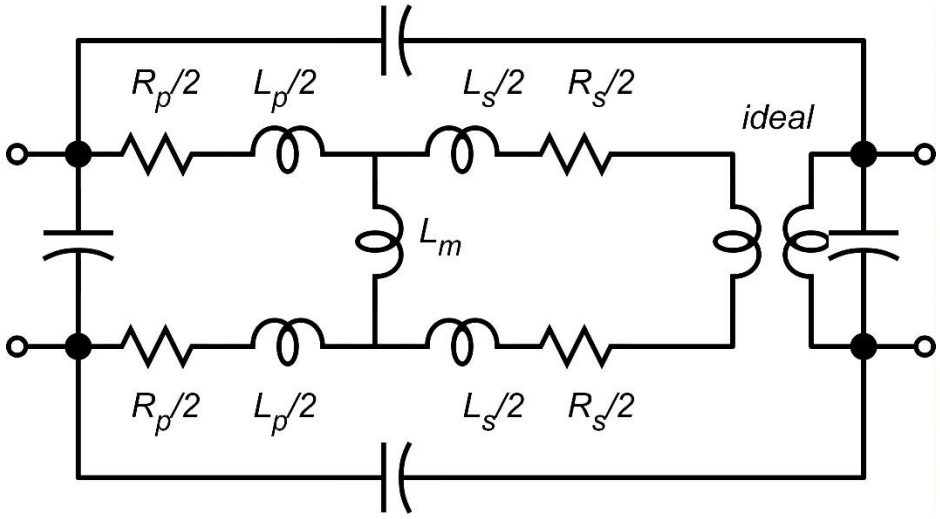
Transformers for impedance transformation

Here the transformer changes (decreases) the real part of the load admittance.



Additional tuning elements used to adjust $Im(Y_L)$

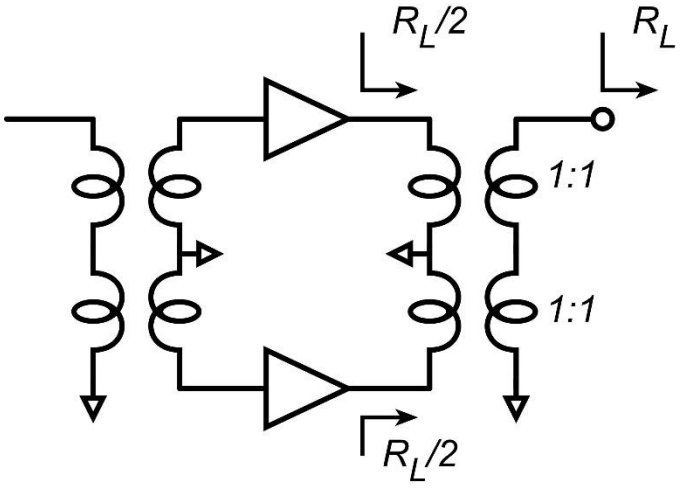
Transformers have extensive parastics and require careful electromagnetic modeling



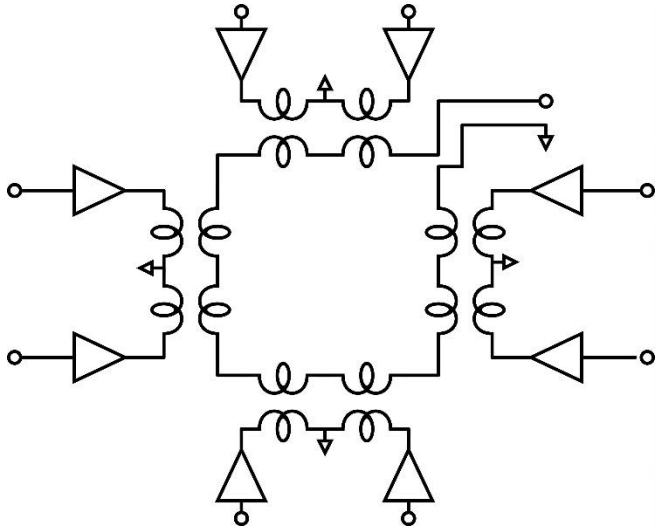
Transformers for power combining

Here the transformers combine power from 2 cells.

Each cell sees 1/2 the load impedance

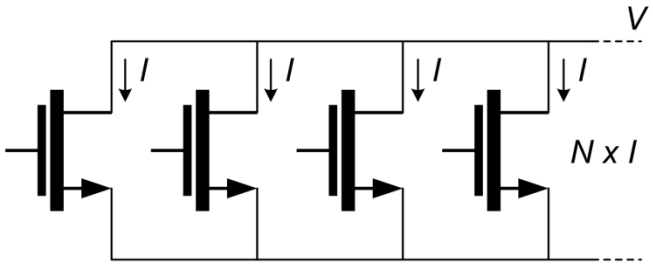


The transformer primary can be segmented to extend to N - way combining



I. Aoki *et al.* IEEE JSSC,March 2002

Parallel Power-Combining

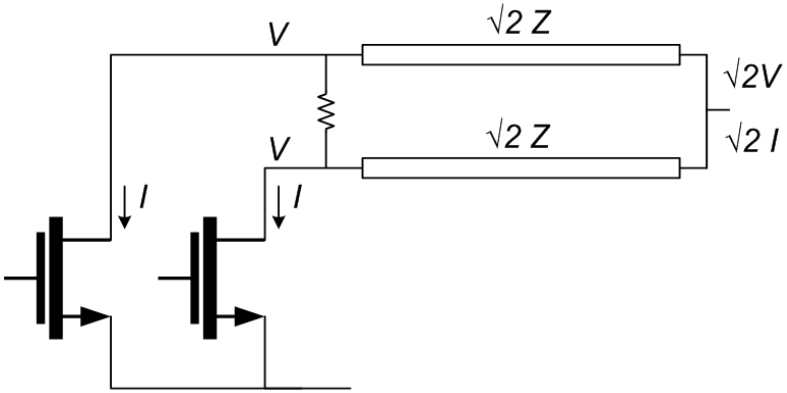


Output power: P_{OUT} = N x V x I

Parallel connection increases P_{OUT} ✓

Load Impedance: Z_{OPT} = V / (N x I)

Parallel connection decreases Z_{opt} ✗



High P_{OUT} → Low Z_{opt}

Needs impedance transformation:

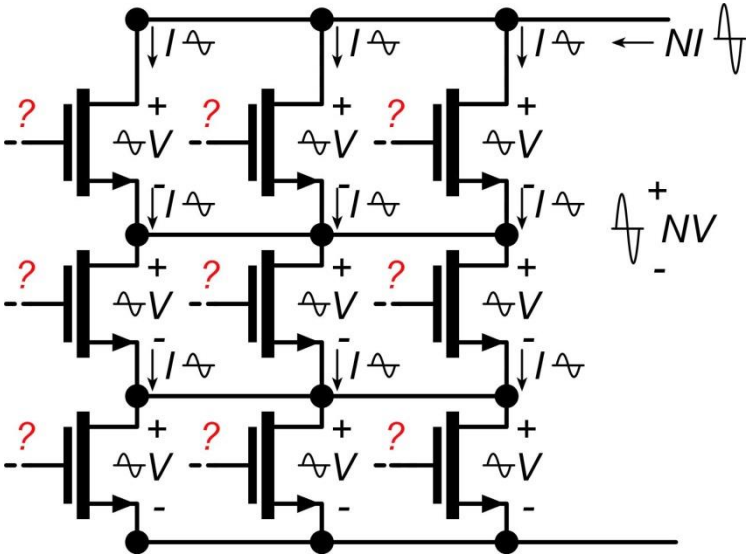
lumped lines, Wilkinson, …

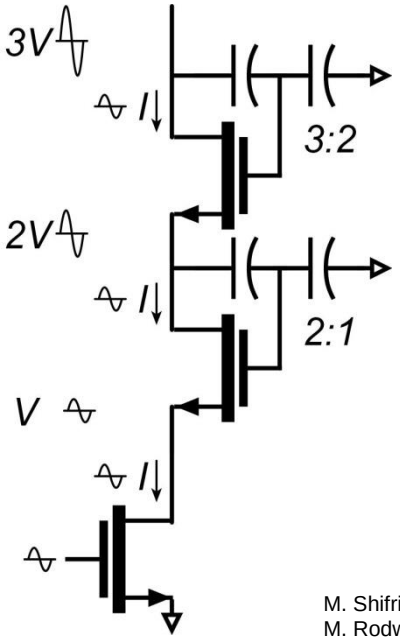
High insertion loss ✗

Small bandwidth ✗

Large die area ✗

Series Power-Combining & Stacks





Parallel connections: $I_{out}=N \times I$

Series connections: $V_{out}=N \times V$

Output power: $P_{out}=N^2 \times V \times I$

Load impedance: $Z_{opt}=V/I$ ✓

Small or zero power-combining losses ✓

Small die area ✓

How do we drive the gates ?

Local voltage feedback:

drives gates, sets voltage distribution

Design challenge:

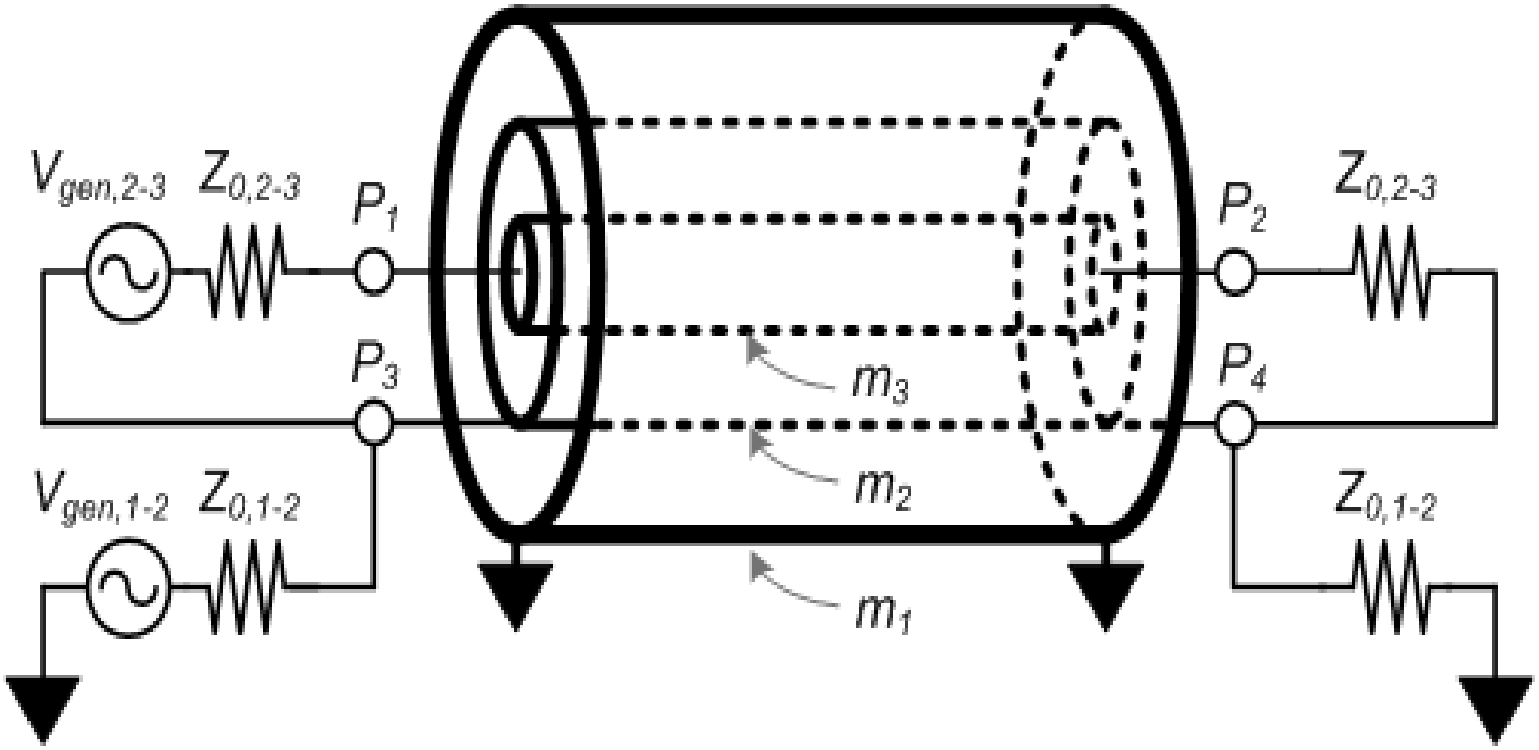
need uniform RF voltage distribution

need ~unity RF current gain per element

...needed for simultaneous compression of all FETs.

M. Shifrin, Y. Ayasli, and P. Katzin, 1992 IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp.
M. Rodwell and S. Jaganathan, U.S. Patent 5,945,879, Aug. 31, 1999.
S. Pornpromlikit, H.-T. Dabag, B. Hanafi, J. Kim, L. Larson, J. Buckwalter, and P. Asbeck, 2011 IEEE CSIC Symp.

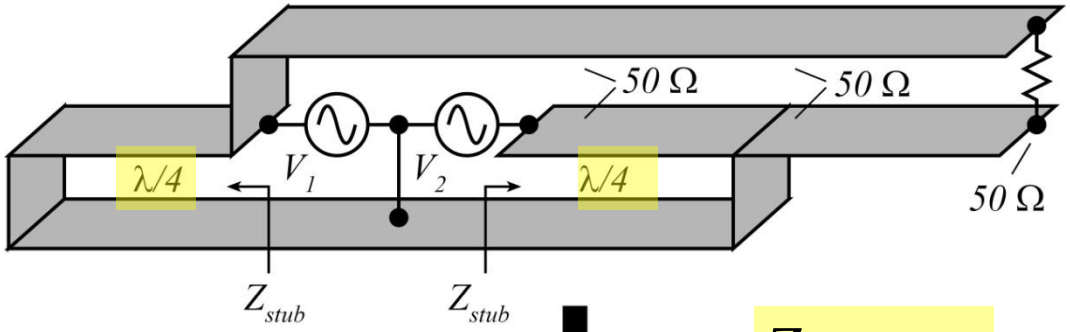
3-conductor transmission Lines



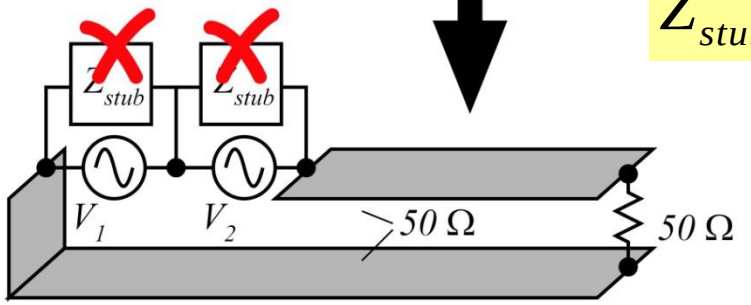
Two separate transmission lines (m_3-m_2, m_2-m_1)

→ E, H fields between m_3 and m_1 perfectly shielded

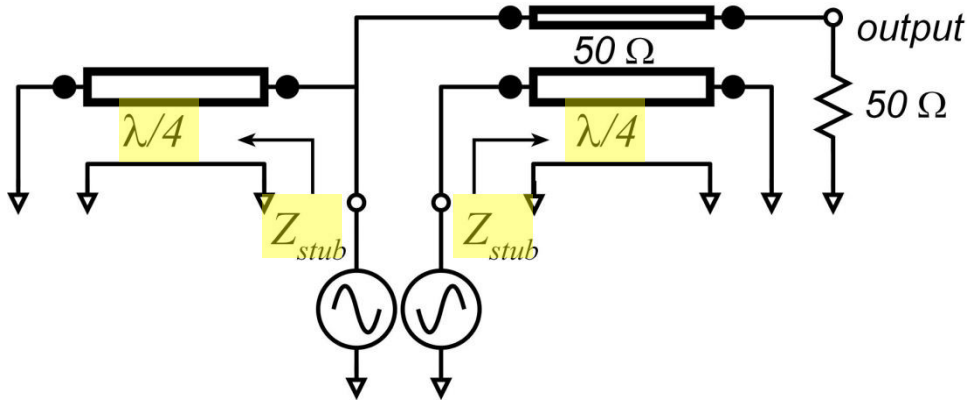
Standard λ/4 Baluns: **Series** Combining



$$Z_{stub} = \infty$$

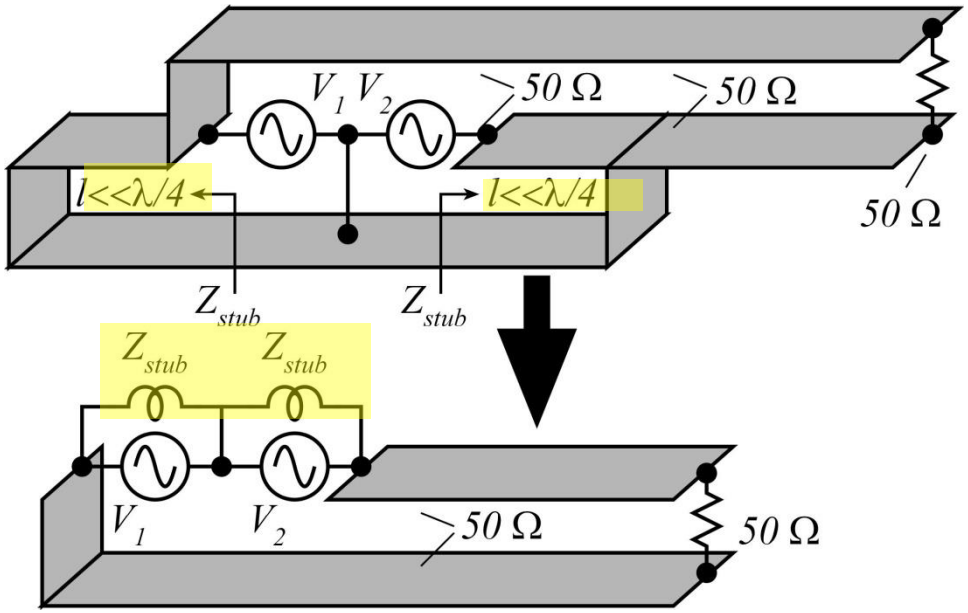


Balun combiner:
voltages add
2:1 series connection
each source sees 25 Ω
→ double I_{max} for each source
4:1 increased P_{out}



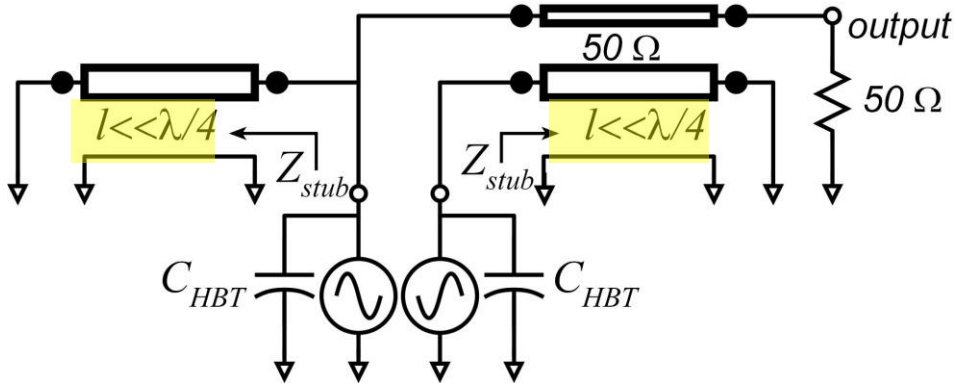
Standard λ/4 balun :
λ/4 stub→ open circuit
long lines→ high losses
long lines → large die

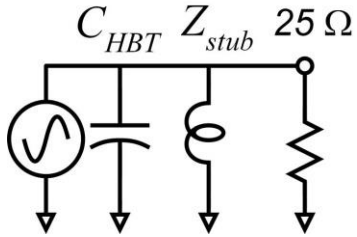
Sub-λ/4 Baluns for **Series** Combining



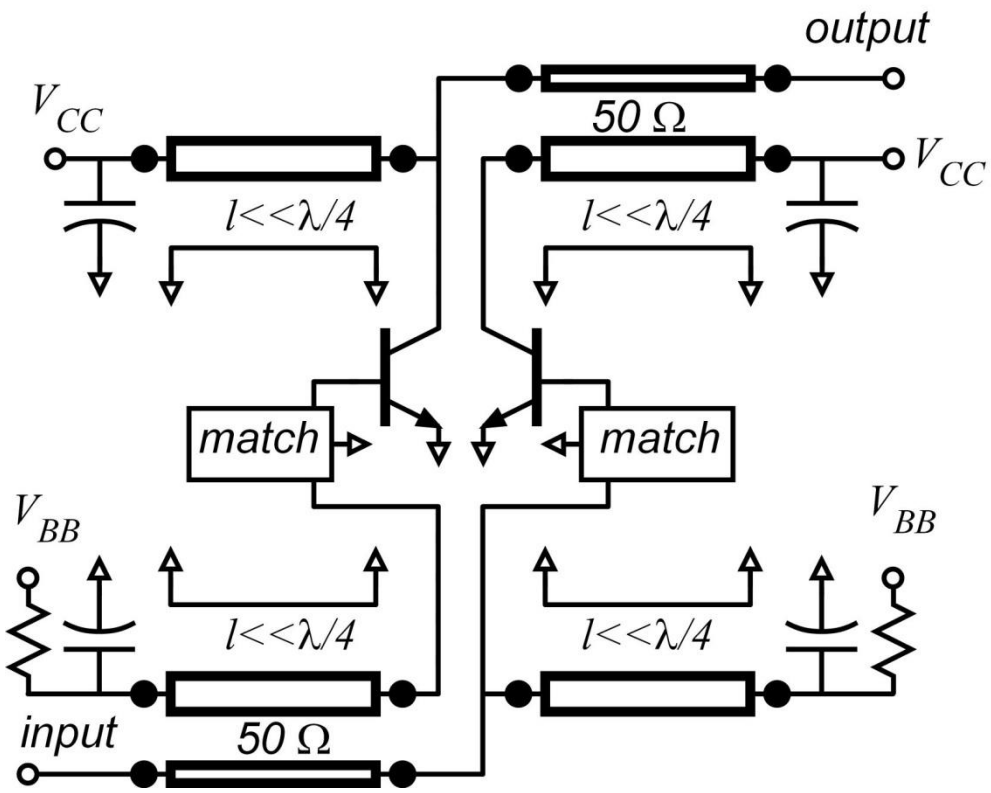
What if balun length is <<λ/4 ?
Stub becomes inductive

Sub-λ/4 balun :
stub→ inductive
tunes transistor C_{out}
short lines→ low losses
short lines → small die





Sub-λ/4 Baluns for **Series** Combining



2:1 baluns:

2:1 series connection

Each device loaded by 25Ω

→ HBTs are 2:1 larger than needed for 50Ω load.

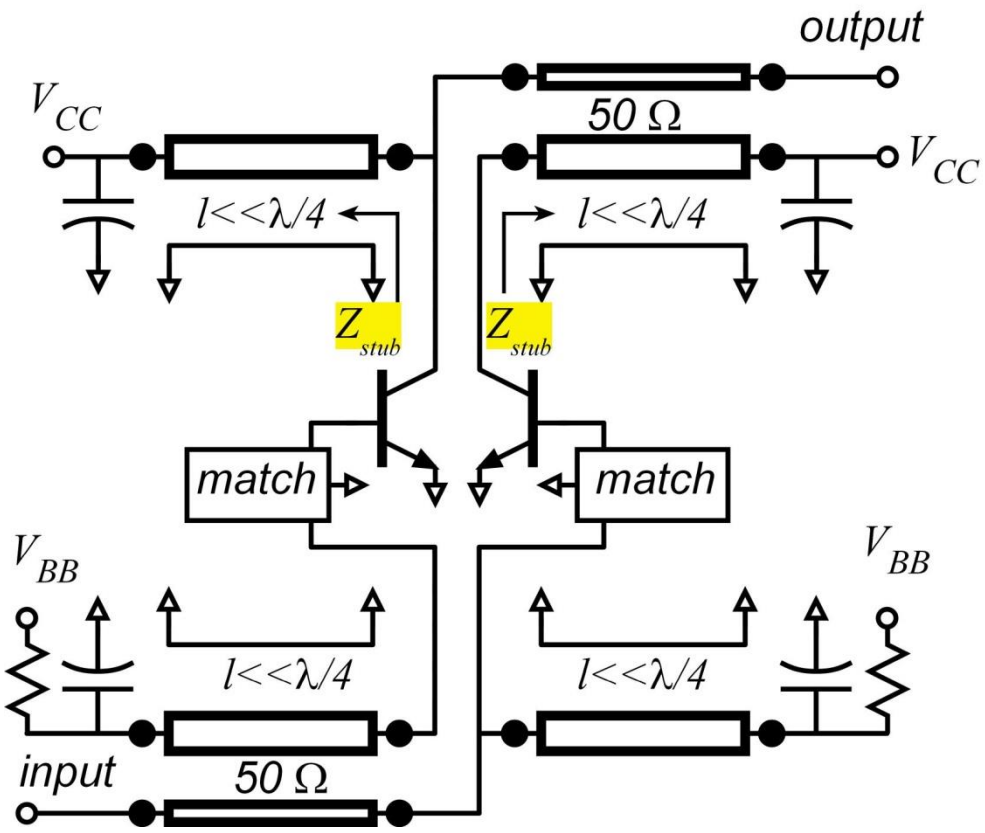
→ 4:1 increased P_{out}.

Sub λ/4 balun: inductive stub

balun inductive stub tunes HBT C_{out}.

Similar network on input.

Sub-λ/4 Balun Series-Combiner: Design



Each HBT loaded by 25Ω

HBT junction area selected so that $I_{max}=V_{max}/25\Omega$

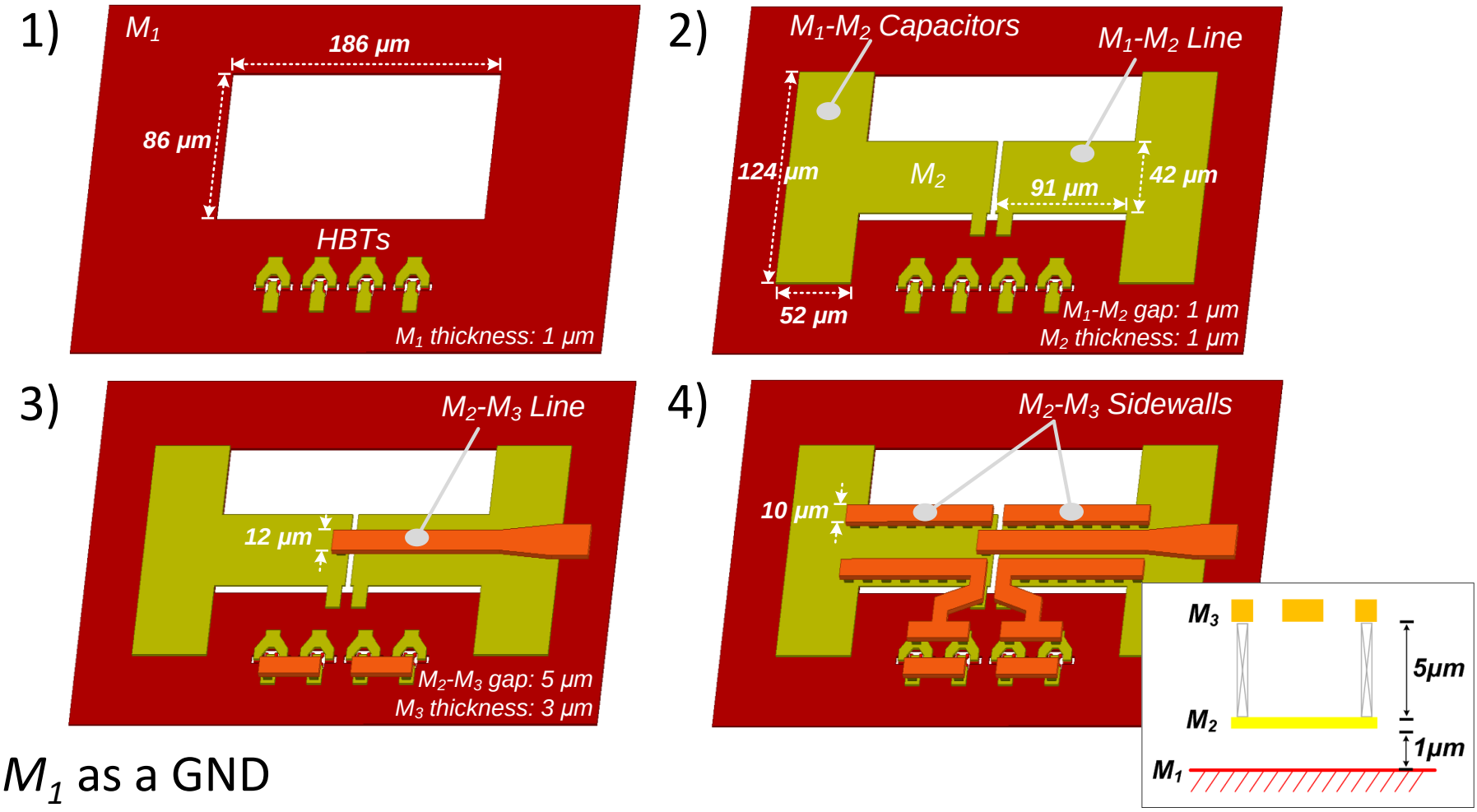
Each HBT has some C_{out} .

Stub length picked so that $Z_{stub}=-1/j\omega C_{out}$ → tunes HBT

$$P_{out} = 4 \times \left(\frac{V_{\max}^2}{8 \cdot 50\Omega} \right)$$

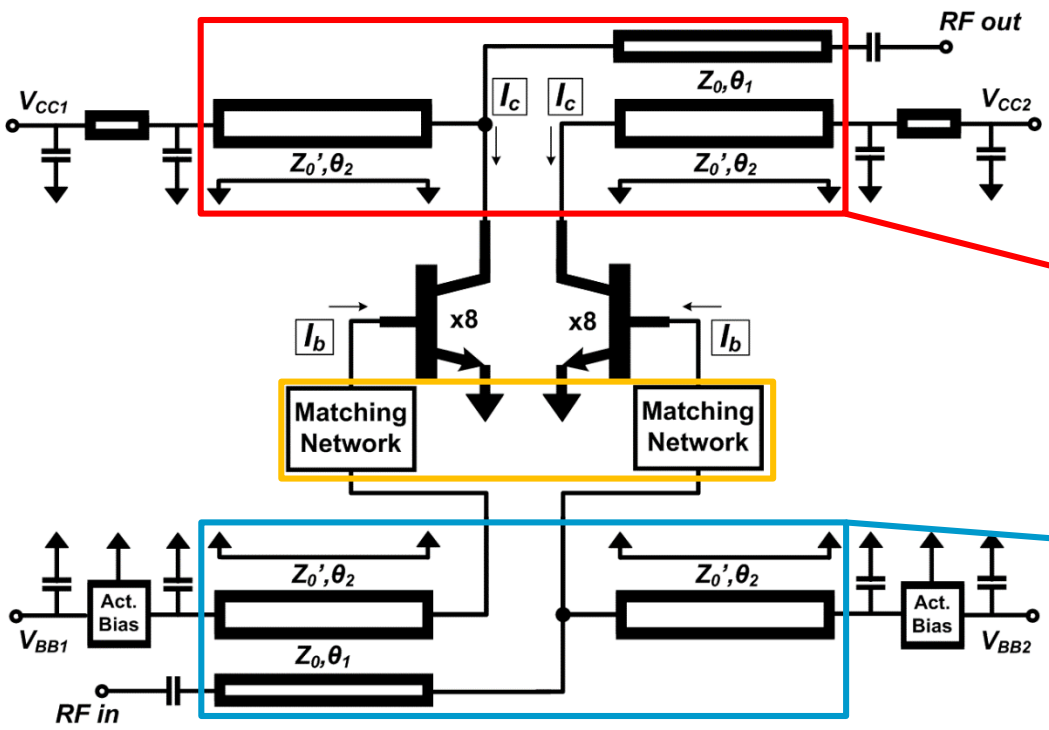
4:1 more power than without combiner.

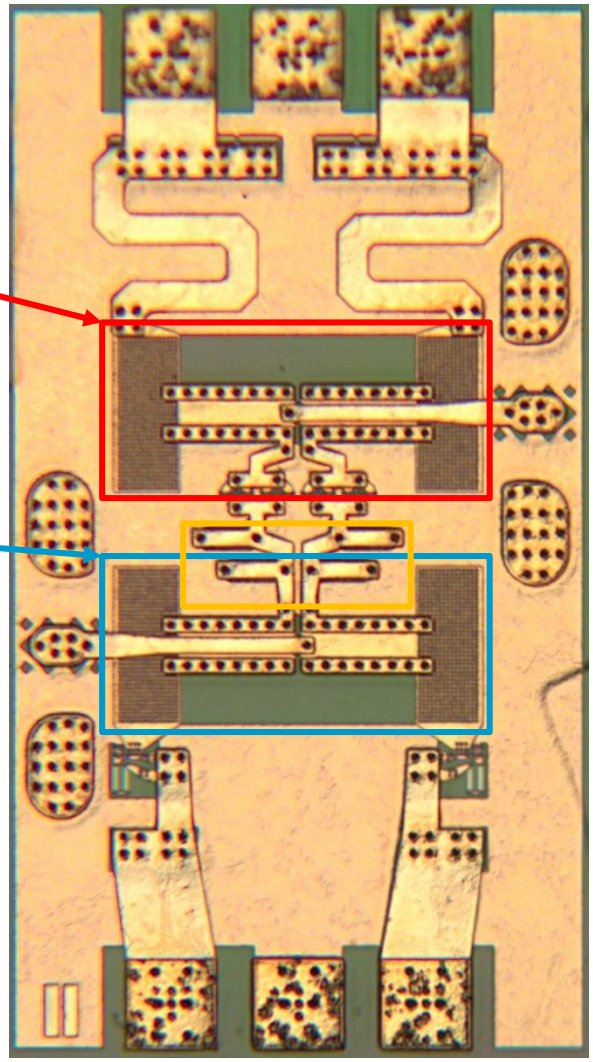
Baluns in **Real ICs**



1) M_1 as a GND
2) Slot-type transmission lines (M_1-M_2), AC short (2 pF MIM)
3) Microstrip line (M_2-M_3), E-field shielding NOT negligible
4) Sidewalls between M_3-M_1 (Faraday cages), λ/16 length

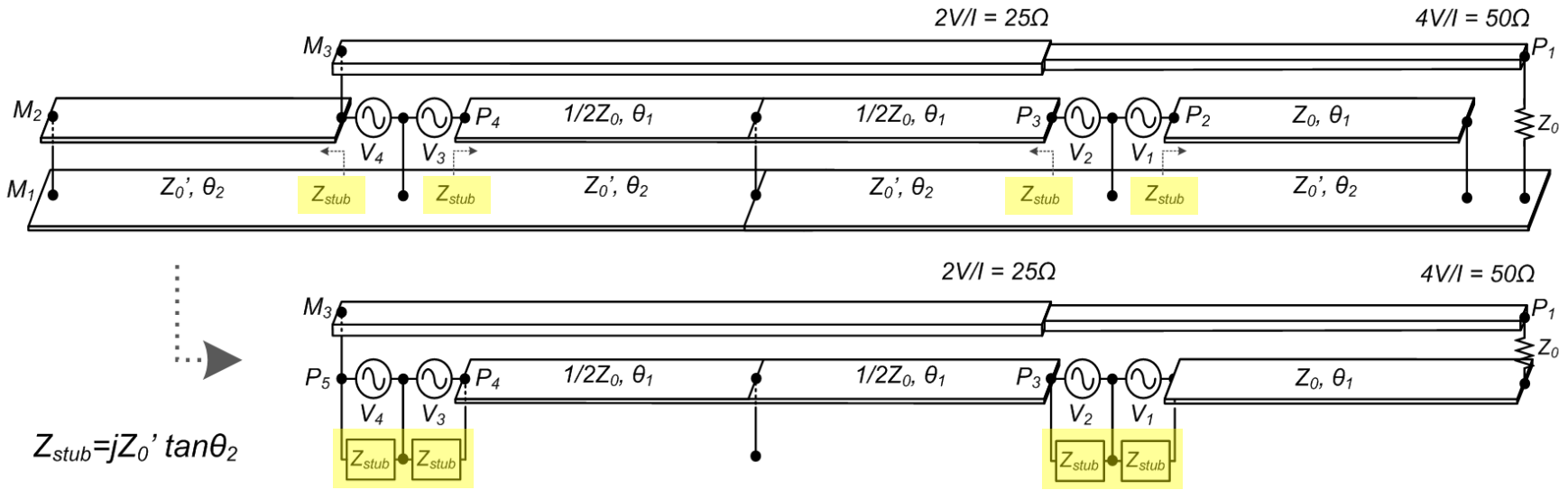
PA Designs Using 2:1 Balun





16:1 PA Using 4:1 Baluns

4:1 series-connected power-combining



Each HBT loaded by 12.5Ω

HBT junction area selected so that $I_{max}=V_{max}/12.5\Omega$

$$P_{out} = \underline{16} \times \left(\frac{V_{\max}^2}{8 \cdot 50\Omega} \right)$$

Each HBT has some C_{OUT}

Stub length picked so that $Z_{stub}=-1/j\omega C_{out}$ → tunes HBT

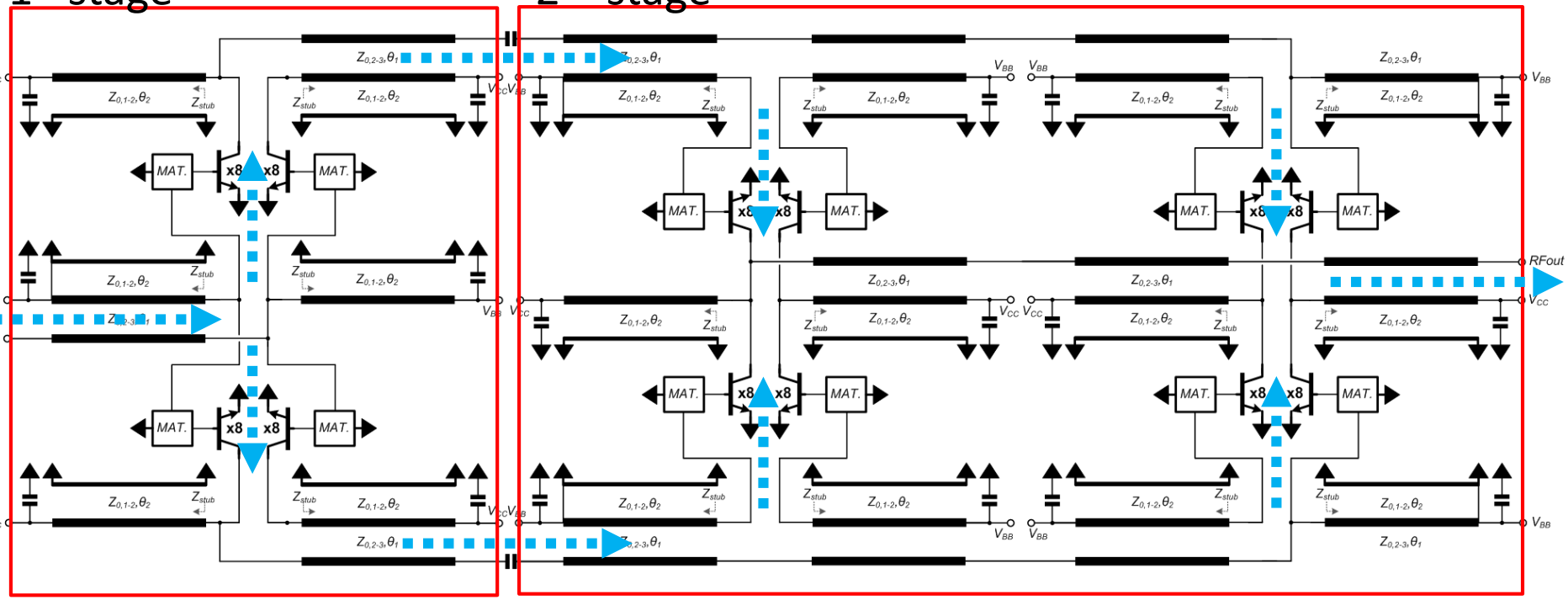
16:1 more power than without combiner.

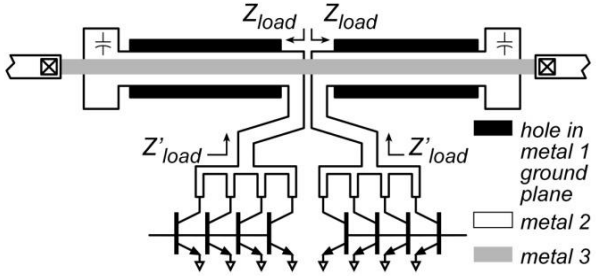
PA IC Schematic (2-stages)

2-stage PA using 2:1 and 4:1 baluns

1st stage

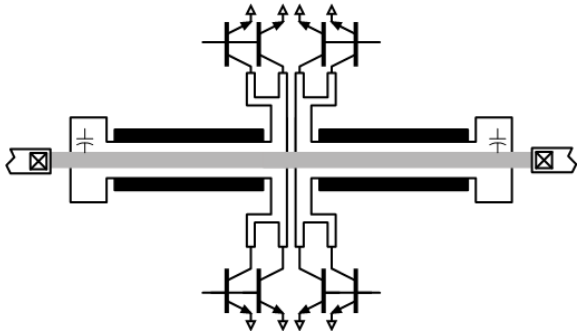
2nd stage





Long lead lines

$Z_{load} \neq Z'_{load}$



PA IC Die Image (2-stages)

IC Size: 1.08 x 0.98 mm^2