ECE145a / 218a: Notes Set 5 device models & device characteristics:

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Content:

Bipolar Transistor Models

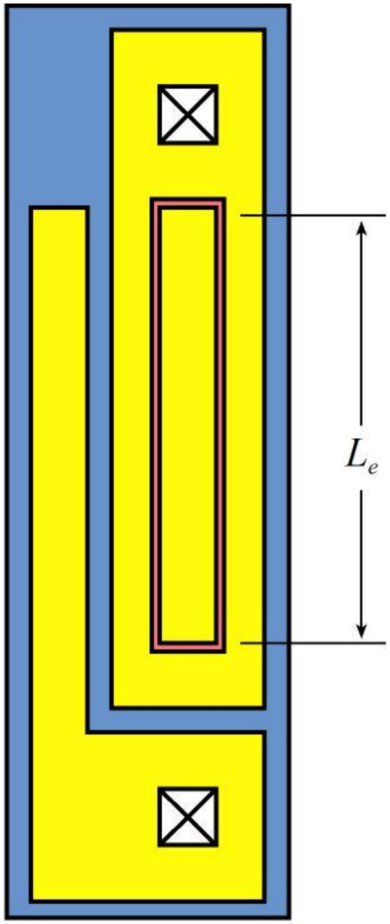
MOSFET Models

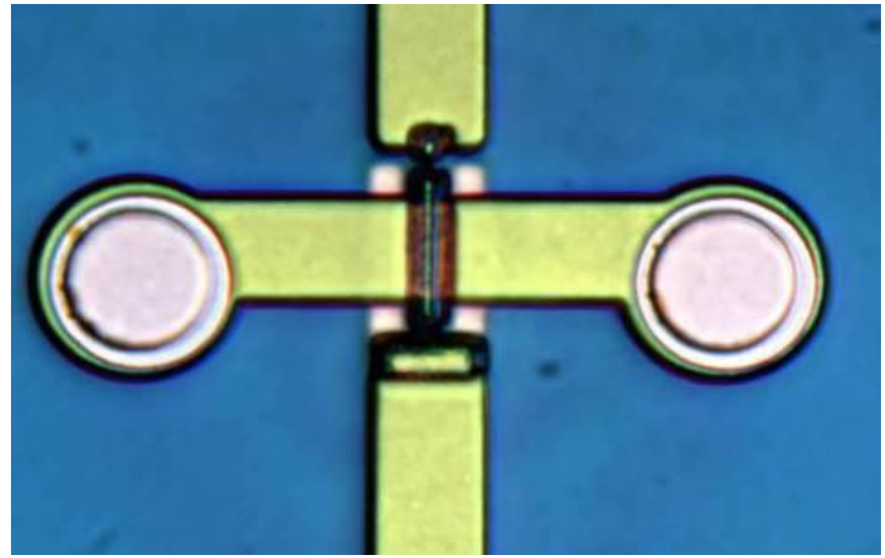
HEMT (JFET) models

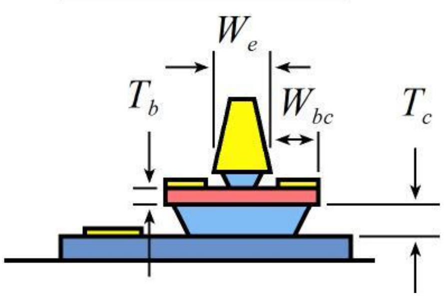
Cutoff frequencies.

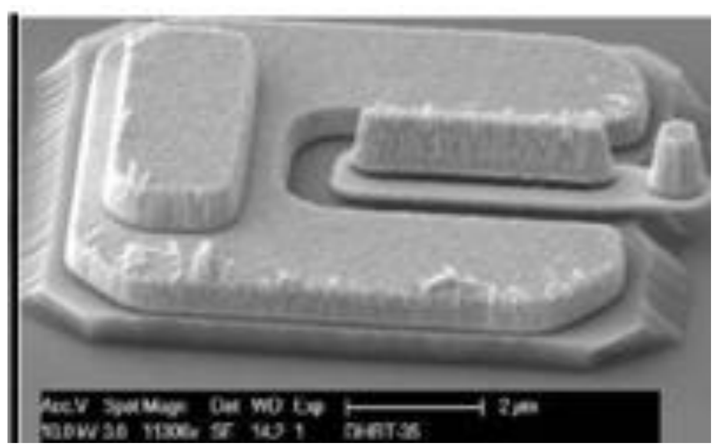
Active Devices:
Bipolar Transistors

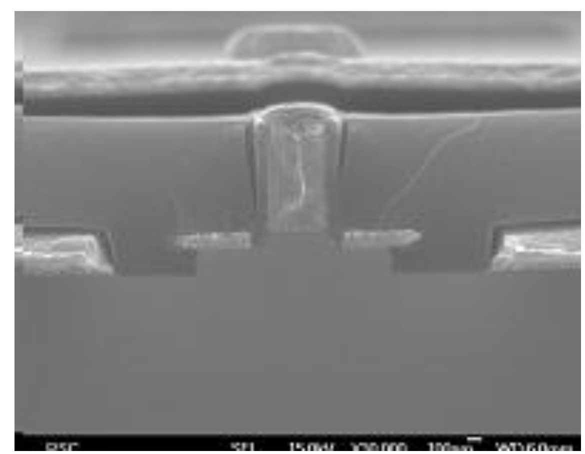
HBT Physical Structure



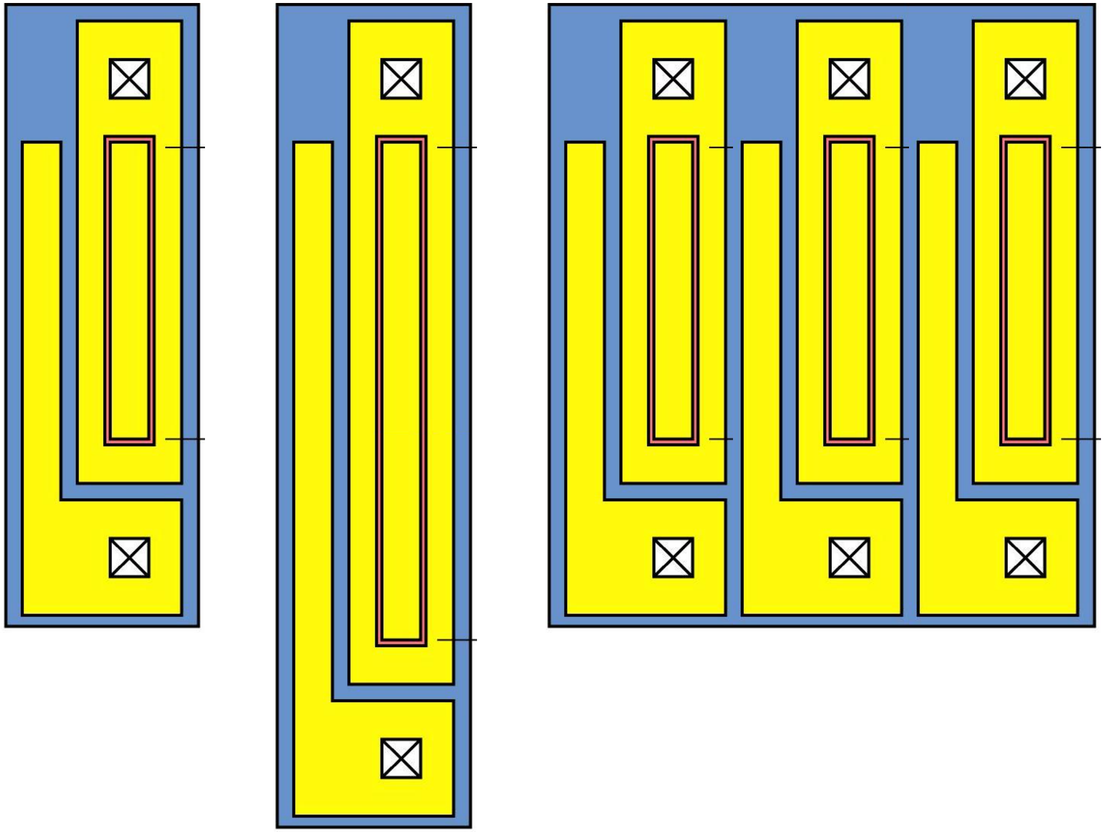


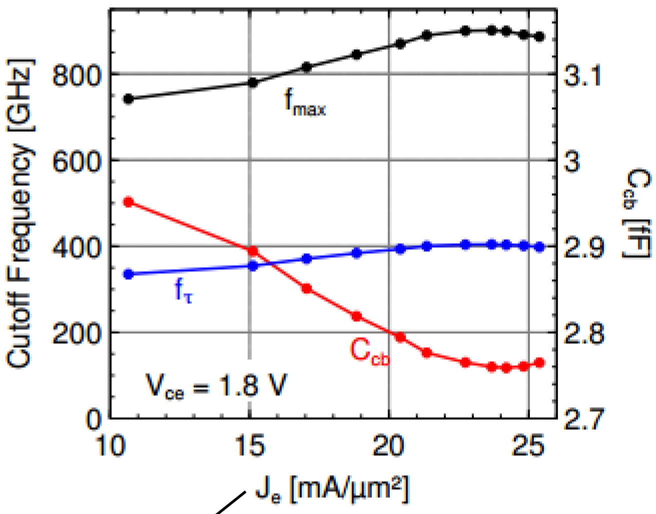






Increasing total emitter area



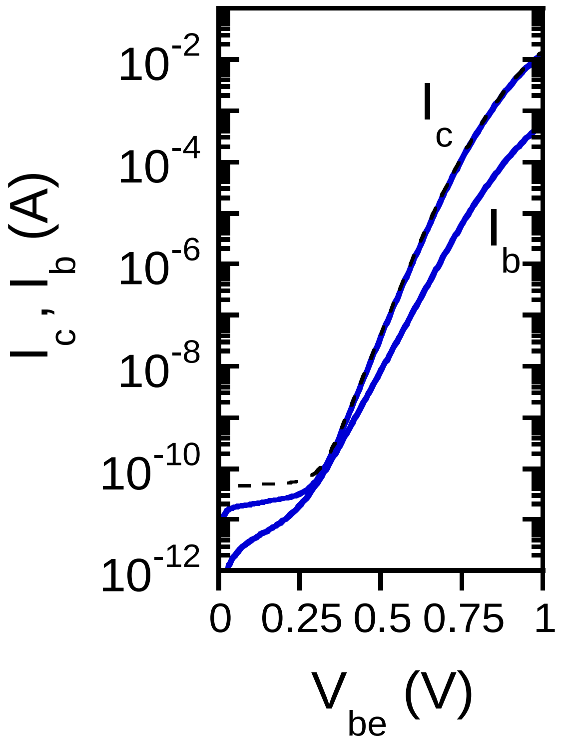


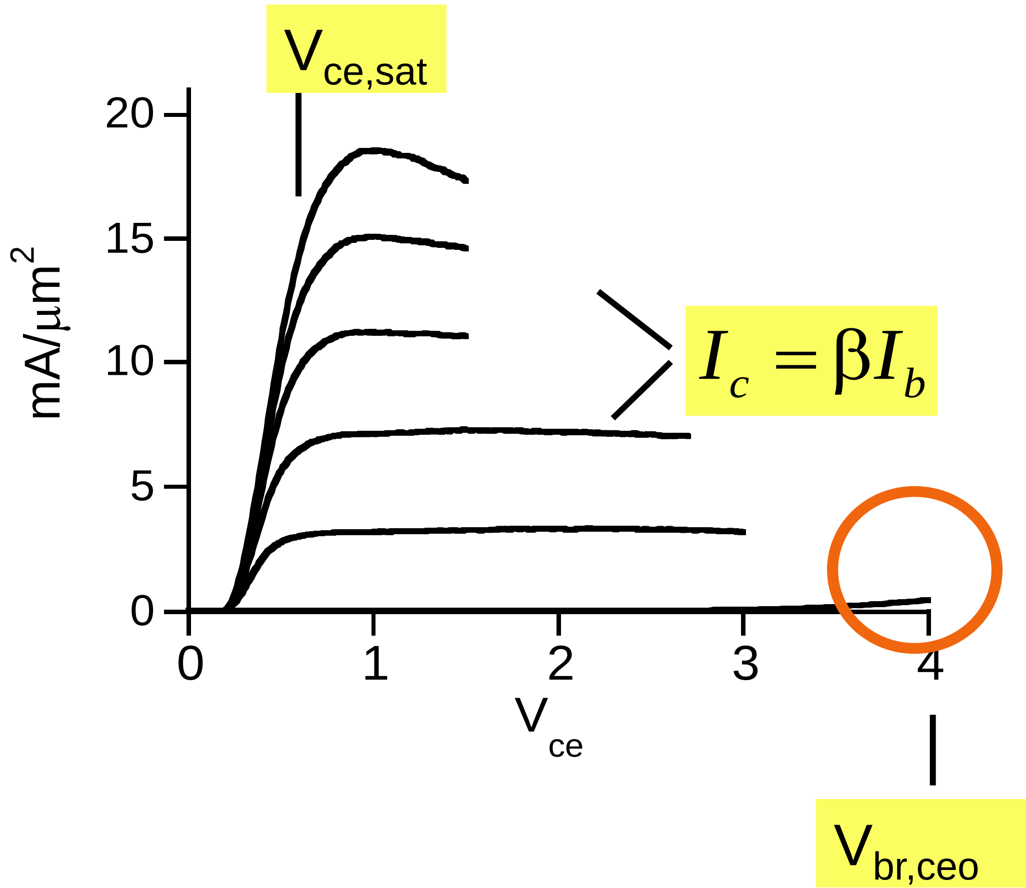
$$J_E = I_E /(\text{total emitter area})$$

Increasing the emitter area (increasing L_E, or multiple fingers) increases the maximum current.

Emitter area generally selected to reach peak bandwidth at some specified current.

Bipolar Transistor: DC characteristics: common-emitter





Approximately :

$$I_c = I_s e^{qV_{be}/nkT} \text{ and } I_b = I_c / \beta$$

These relationships are approximate,

and fail at higher current densities

HBT hybrid-Pi equivalent-circuit model

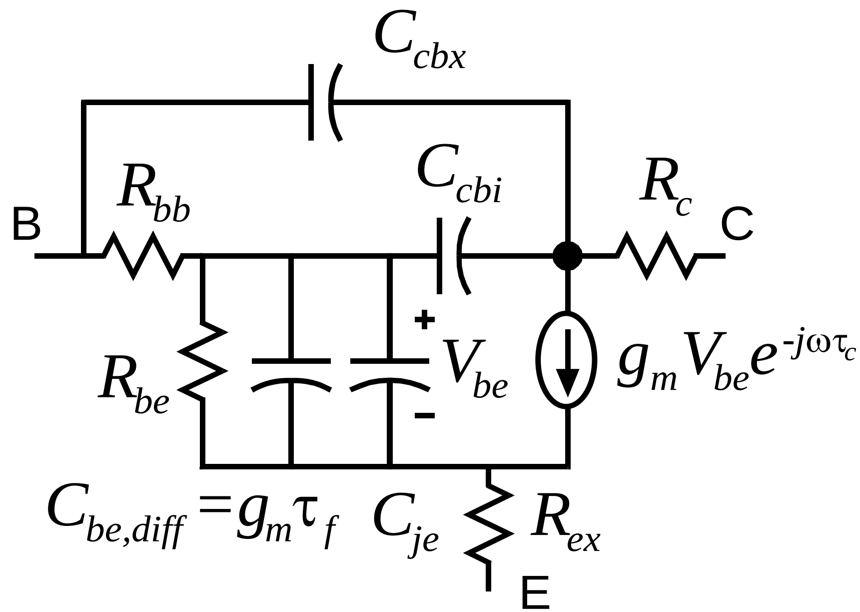
$$R_{be} = \beta / g_m$$

$$\tau_f = \tau_b + \tau_c$$

$$\tau_f = \tau_{base} + \tau_{collector}$$

$$g_{mo} \equiv \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{(nkT/q)}$$

$$g_m = g_{mo} e^{-j\omega\gamma\tau_c} \quad 0 < \gamma < 1 \text{ (typically} \sim 0.8)$$



C_{je}, C_{cbi}, C_{cbx} : depletion capacitances

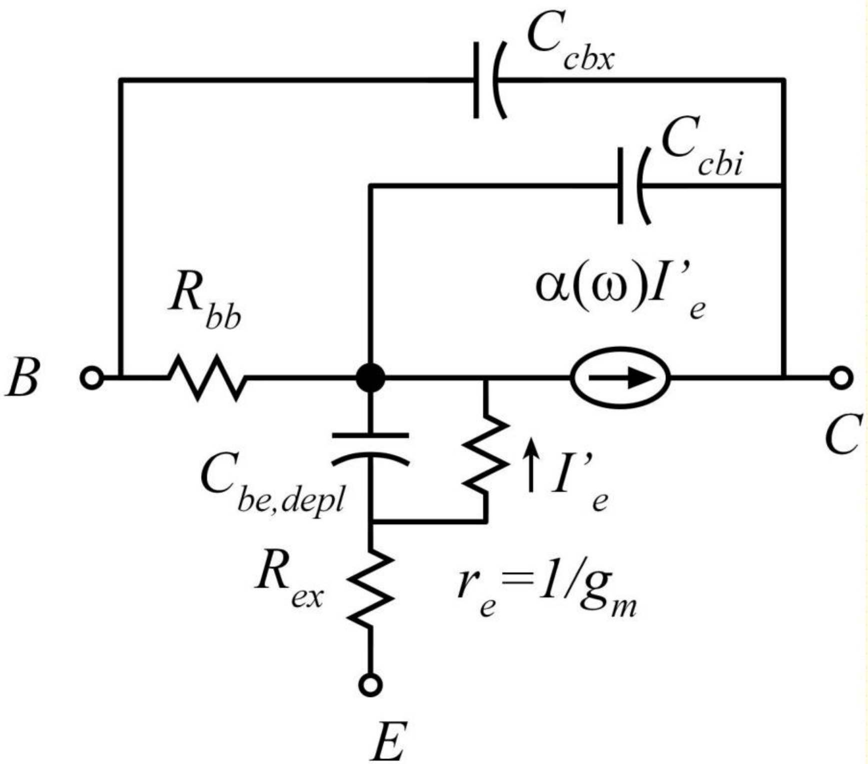
$C_{be,diff}$: diffusion capacitance

τ_b, τ_c : carrier transit times in base and collector

R_b, R_e, R_c : parasitic resitances

The term $e^{-j\omega\gamma\tau_c}$, though often neglected, can be significant in some circuits.

Bipolar Transistor T-model



$$\alpha(\omega) \cong \alpha_0 \left(\frac{1}{1 + j\omega\tau_b} \right) \exp(-j\omega\tau_c)$$

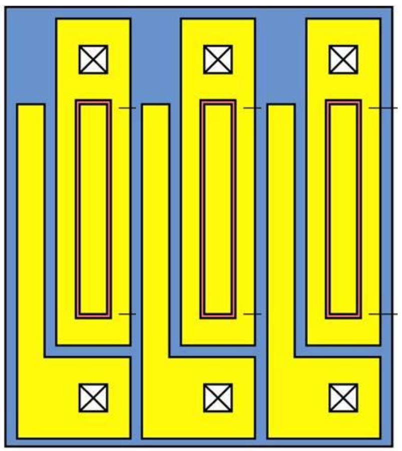
$$\cong \alpha_0 \left(\frac{1}{1 + j\omega\tau_b} \right) \left(\frac{1}{1 + j\omega\tau_c} \right)$$

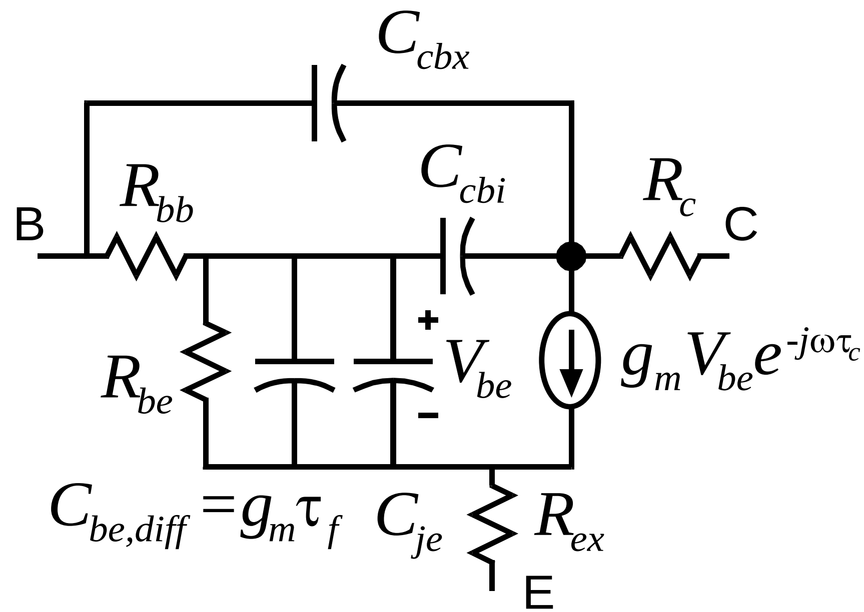
$$\cong \alpha_0 \left(\frac{1}{1 + j\omega(\tau_b + \tau_c)} \right)$$

The approximations above, if taken to first order in ω, produce the hybrid pi model.

The T model is more convenient for common-base amplifier analysis.

How model varies as emitter area is increased





Increasing the emitter area by $N:1 \rightarrow$ same as wiring N HBTs in parallel.

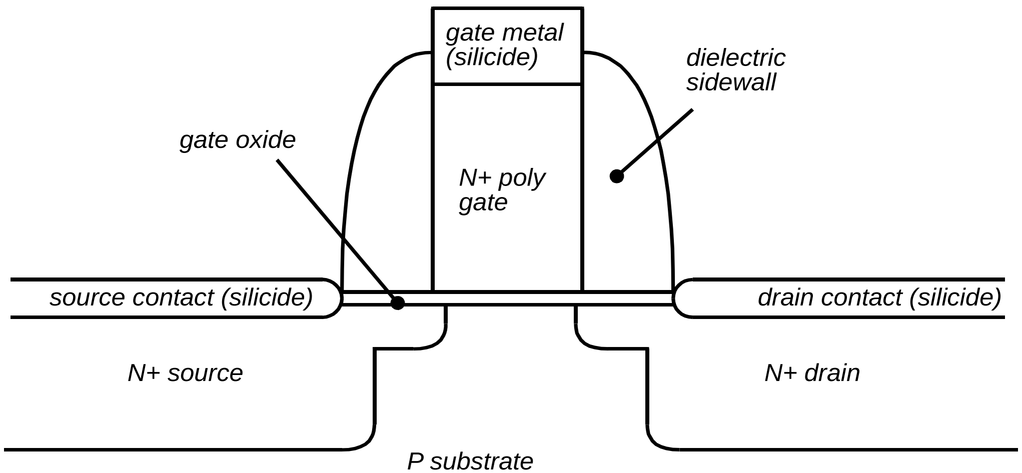
All capacitances increase $N:1$, all resistances decrease $1:N$.

C_{be}, R_{be} and g_m are given by the formulas on the previous pages.

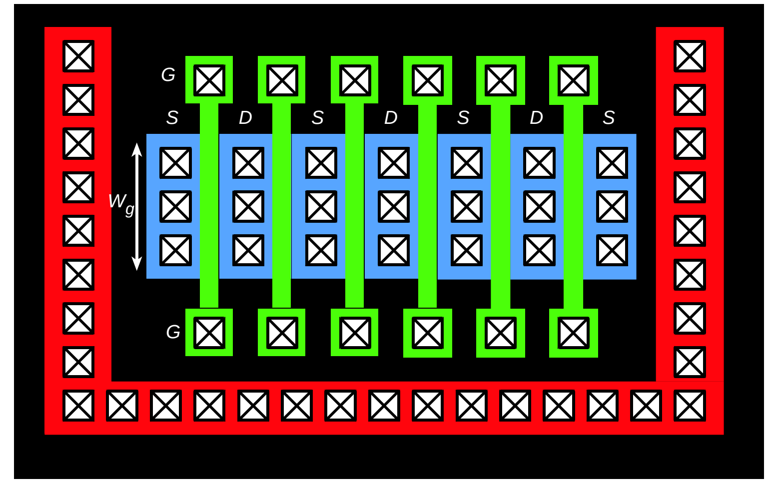
Active Devices: Silicon MOSFETs

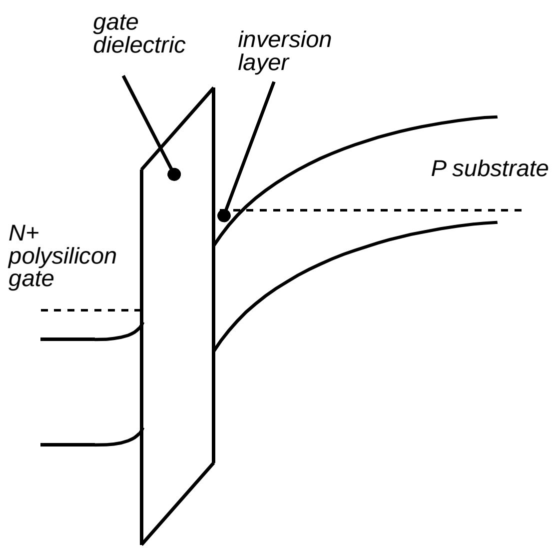
Planar Bulk MOSFET

Cross-Section

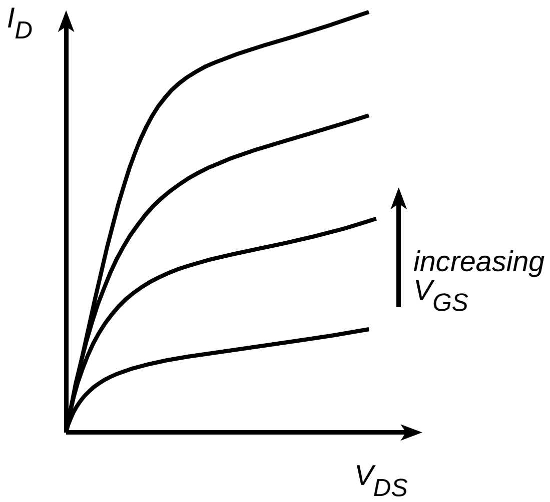


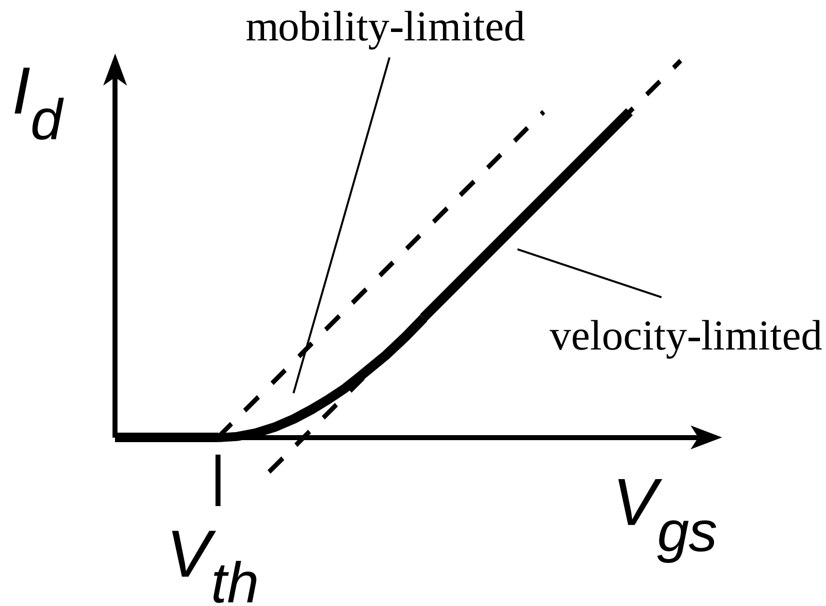
Layout (multi-finger)





MOSFET DC Characteristics





For drain voltages larger than the knee voltage :

mobility – limited current

$$I_{D,\mu} = \mu c_{ox} W_g (V_{gs} - V_{th})^2 / 2L_g$$

velocity – limited current

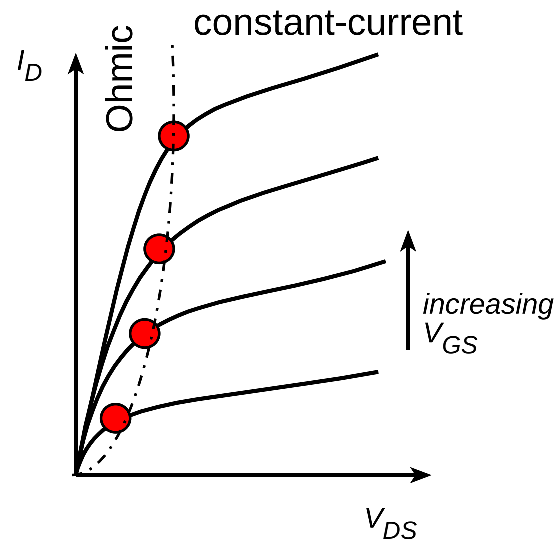
$$I_{D,v} = c_{ox} W_g v_{sat} (V_{gs} - V_{th})$$

Generalized Expression

$$\left(\frac{I_D}{I_{D,v}}\right)^2 + \left(\frac{I_D}{I_{D,\mu}}\right) = 1$$

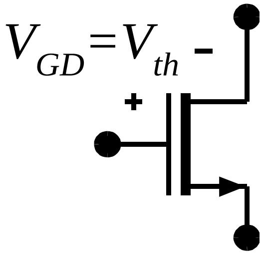
Knee Voltage: Mobility-Limited Case

The knee voltage defines the boundary between the Ohmic and constant-current regions

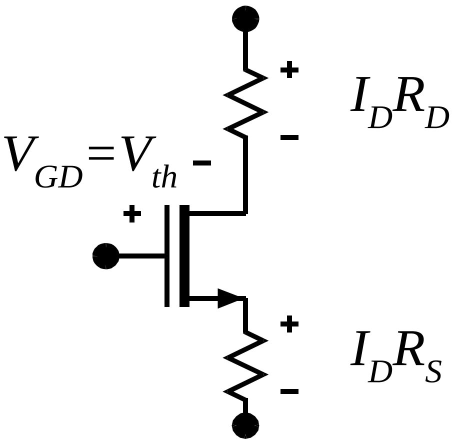


In the mobility-limited regime, the knee in curve occurs when

$$V_{dg} = V_{ds} - V_{gs} = -V_{th}$$

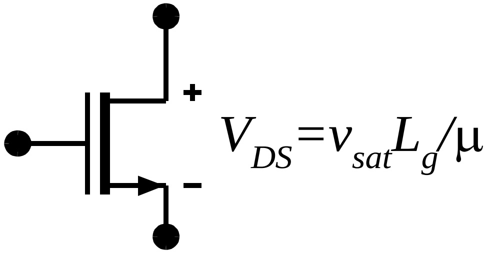


The Knee Voltage is further increased by voltage drops across the parasitic source & drain resistances.

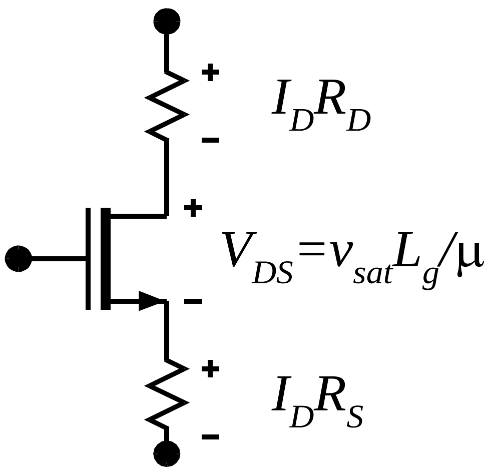


Knee Voltage: Velocity-Limited Case

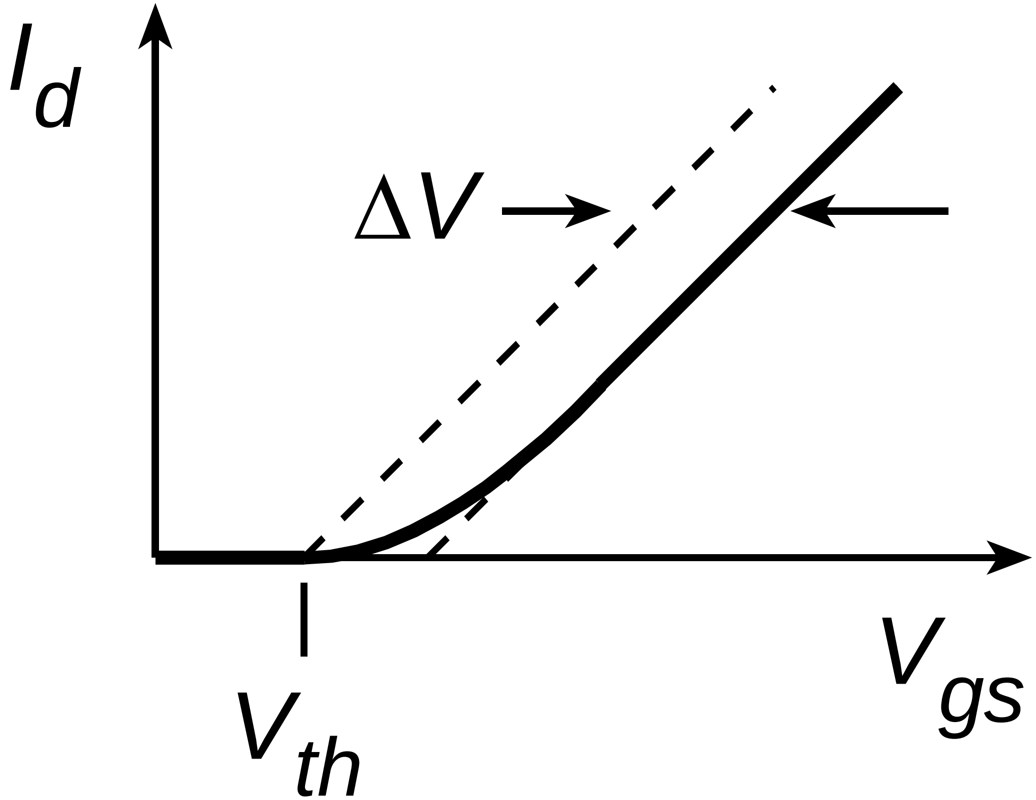
In the velocity - limited regime, the knee in curve occurs when $V_{ds} = v_{sat} L_g / \mu$



Again, the Knee Voltage is further increased by voltage drops across the parasitic source & drain resistances.



DC Characteristics---Far Above Threshold



$$I_D \approx c_{ox} W_g v_{sat} (V_{gs} - V_{th} - \Delta V) \text{ for } (V_{gs} - V_{th}) / \Delta V >> 1$$

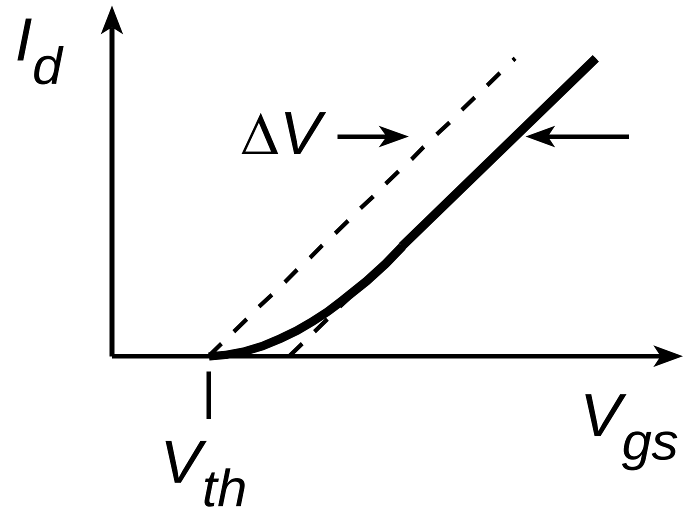
where $\Delta V = v_{sat} L_g / \mu$

MOSFET Transconductance

mobility – limited

$$I_{D,\mu} = \mu c_{ox} W_g (V_{gs} - V_{th})^2 / 2L_g$$

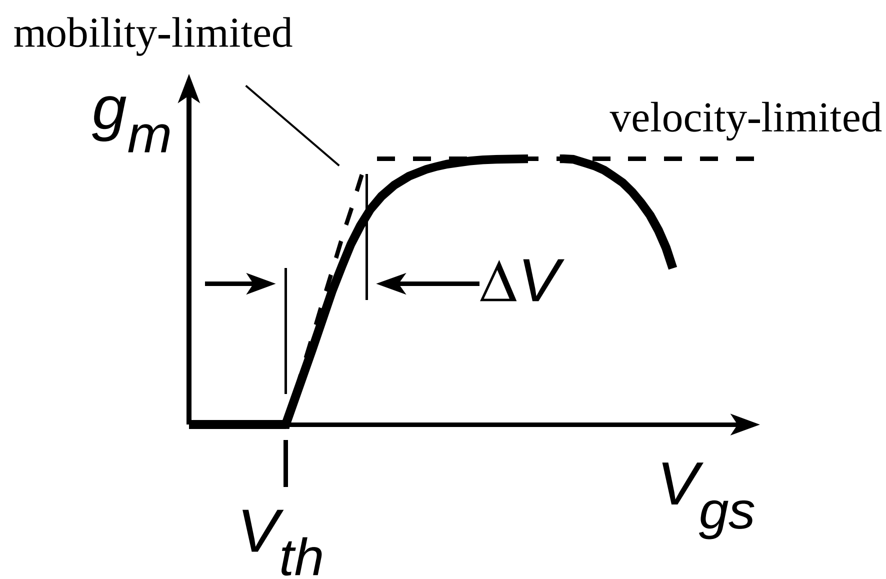
$$\rightarrow g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu c_{ox} W_g (V_{gs} - V_{th}) / L_g$$



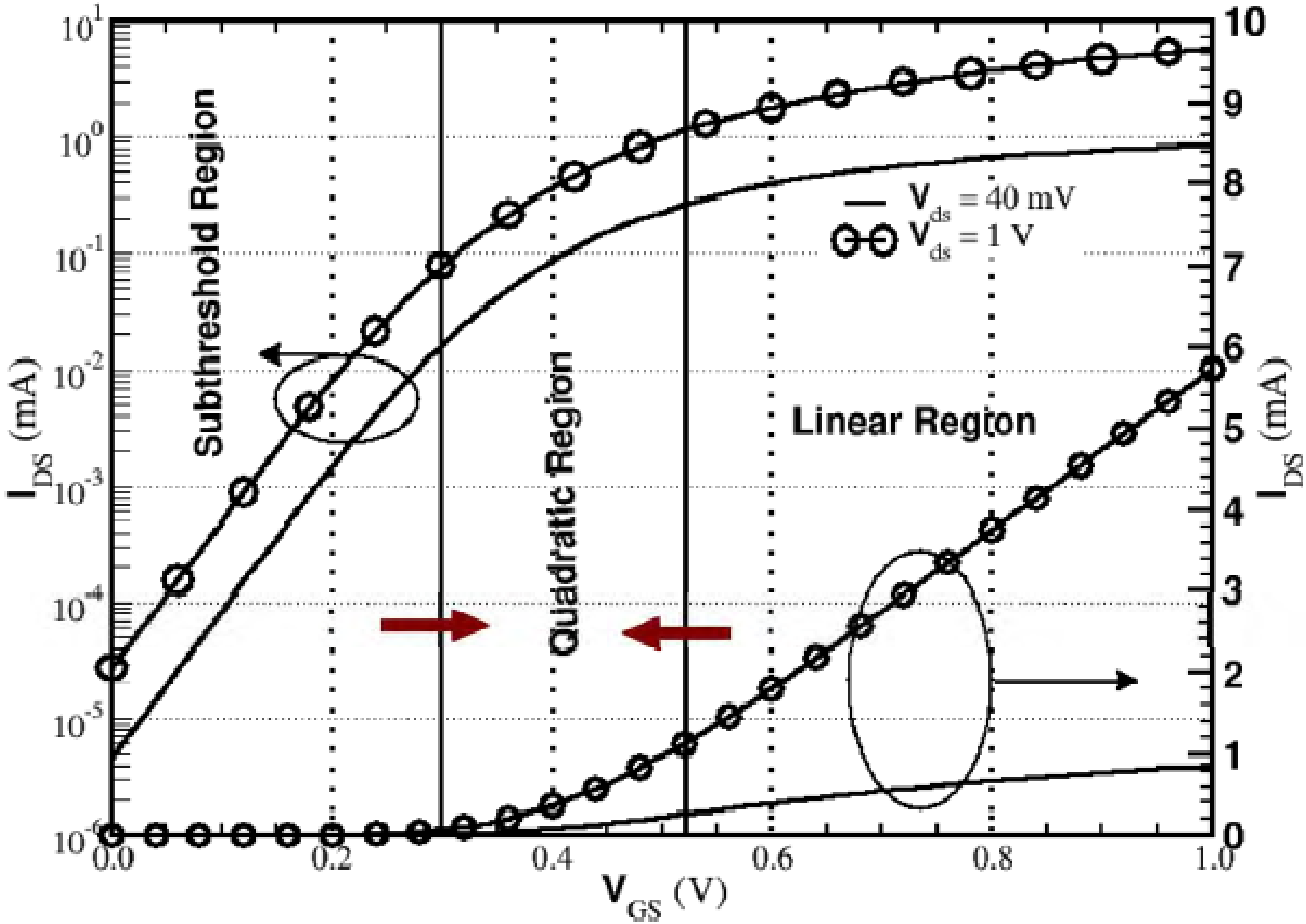
velocity – limited

$$I_{D,v} = c_{ox} W_g v_{sat} (V_{gs} - V_{th})$$

$$\rightarrow g_m = \frac{\partial I_D}{\partial V_{GS}} = c_{ox} W_g v_{sat}$$

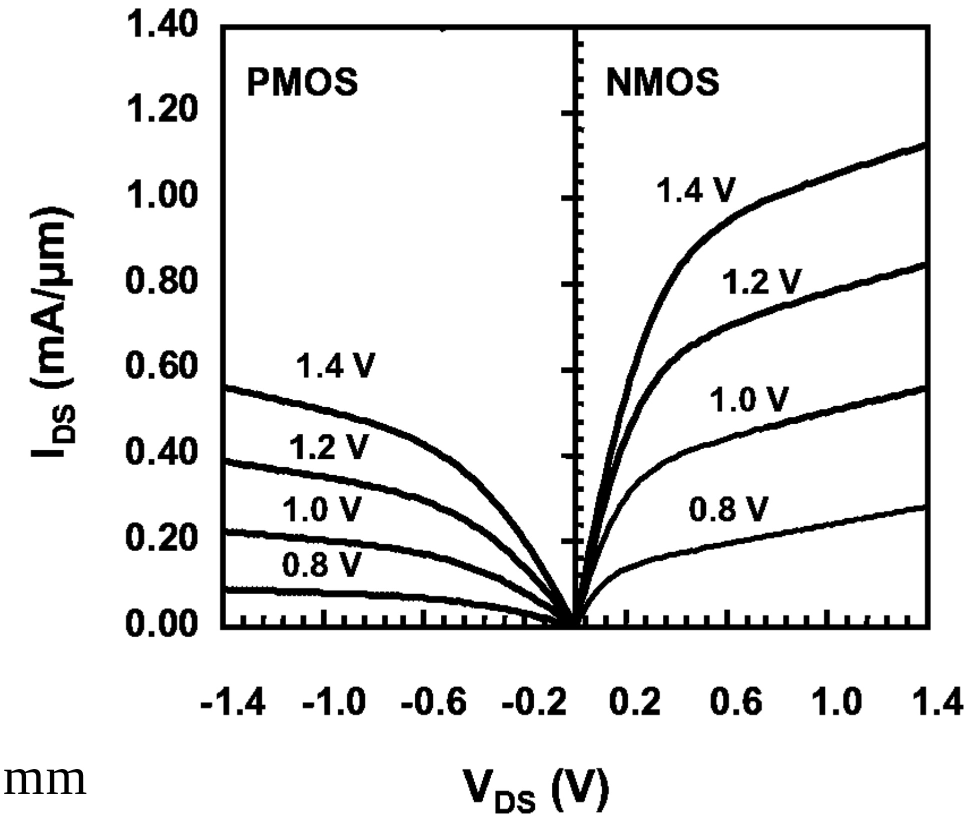


Linear vs. Square-Law Characteristics: 90 nm



Sorin Voinigescu, CSICS RF & High Speed CMOS, Nov. 12, 2006

90 nm MOSFET DC Characteristics



N - channel

$$g_m / W_g = c_{ox} v_{sat} = 1.4 \text{ mS/μm} = 1.4 \text{ S/mm}$$

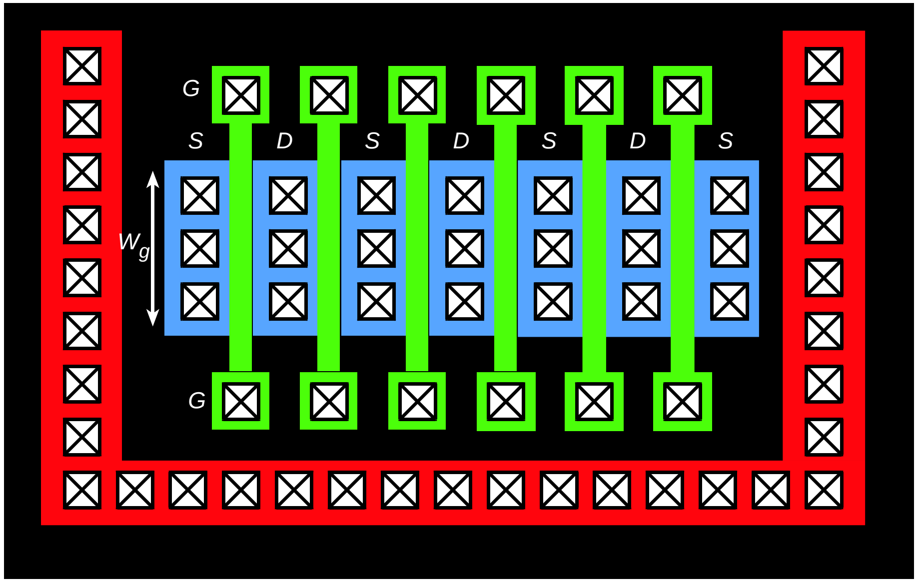
$$V_{th} = 0.6 \text{ V} \quad 1/\lambda \sim 3\text{V}$$

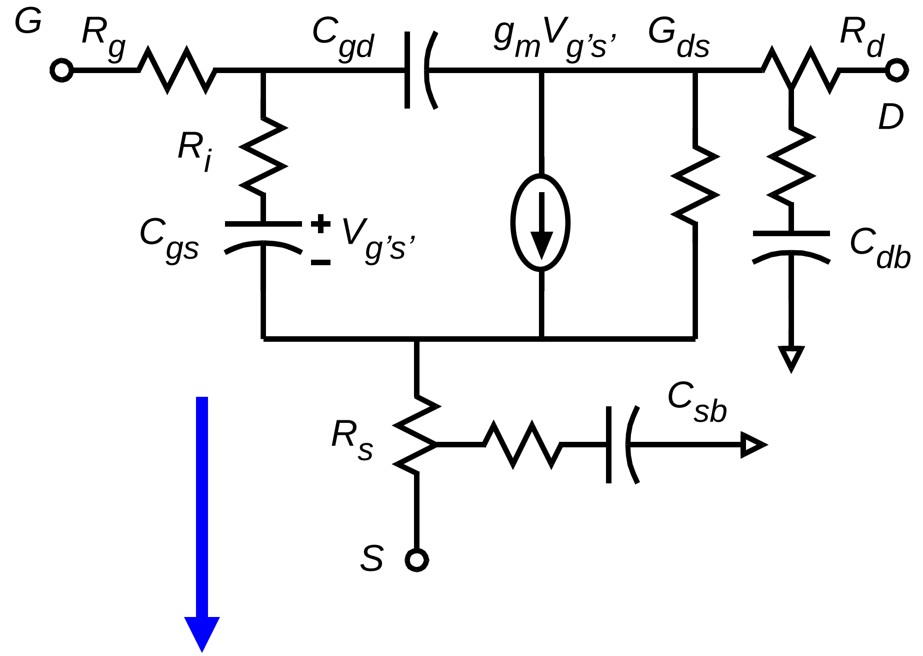
P - channel

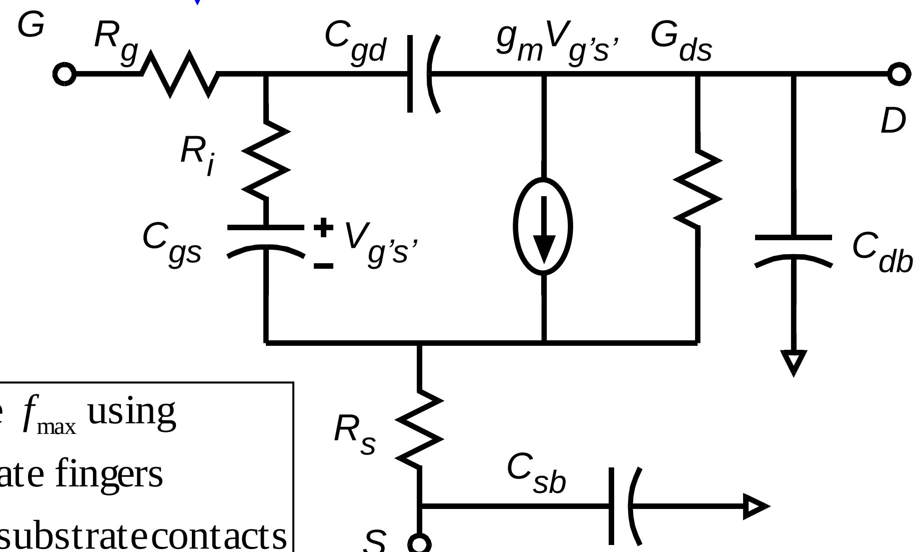
$$g_m / W_g = c_{ox} v_{sat} = 0.7 \text{ mS/μm} = 0.7 \text{ S/mm}$$

$$|V_{th}| = 0.6 \text{ V} \quad 1/\lambda \sim 3\text{V}$$

Device Structure and Model: multi-finger device







$$g_m \cong \frac{\varepsilon}{T_{eq}} v_{eff}\left(NW_g\right) \text{or} \frac{\varepsilon}{T_{eq}} \mu\left(NW_g\right)\left(V_{gs}-V_{th}\right)$$

$$C_{gd} \cong k_o W_g$$

$$k_o \approx (0.3-0.5)\text{fF}/\mu\text{m}$$

$$C_{gs} \cong \frac{\varepsilon}{T_{eq}} L_g\left(NW_g\right)+k_o W_g$$

$$G_{ds} \propto NW_g$$

$$R_i \sim 1/g_m$$

$$R_g \sim \frac{\rho_s}{12L_g}\left(\frac{W_g}{N}\right)+\frac{R_{end}}{2N}$$

$$R_d \propto 1/NW_g$$

$$R_s \propto 1/NW_g$$

$$C_{sb} \propto NW_g$$

$$C_{db} \propto NW_g$$

Increase $f_{\max}$ using
- short gate fingers
- ample substrate contacts

Oversimplified Model

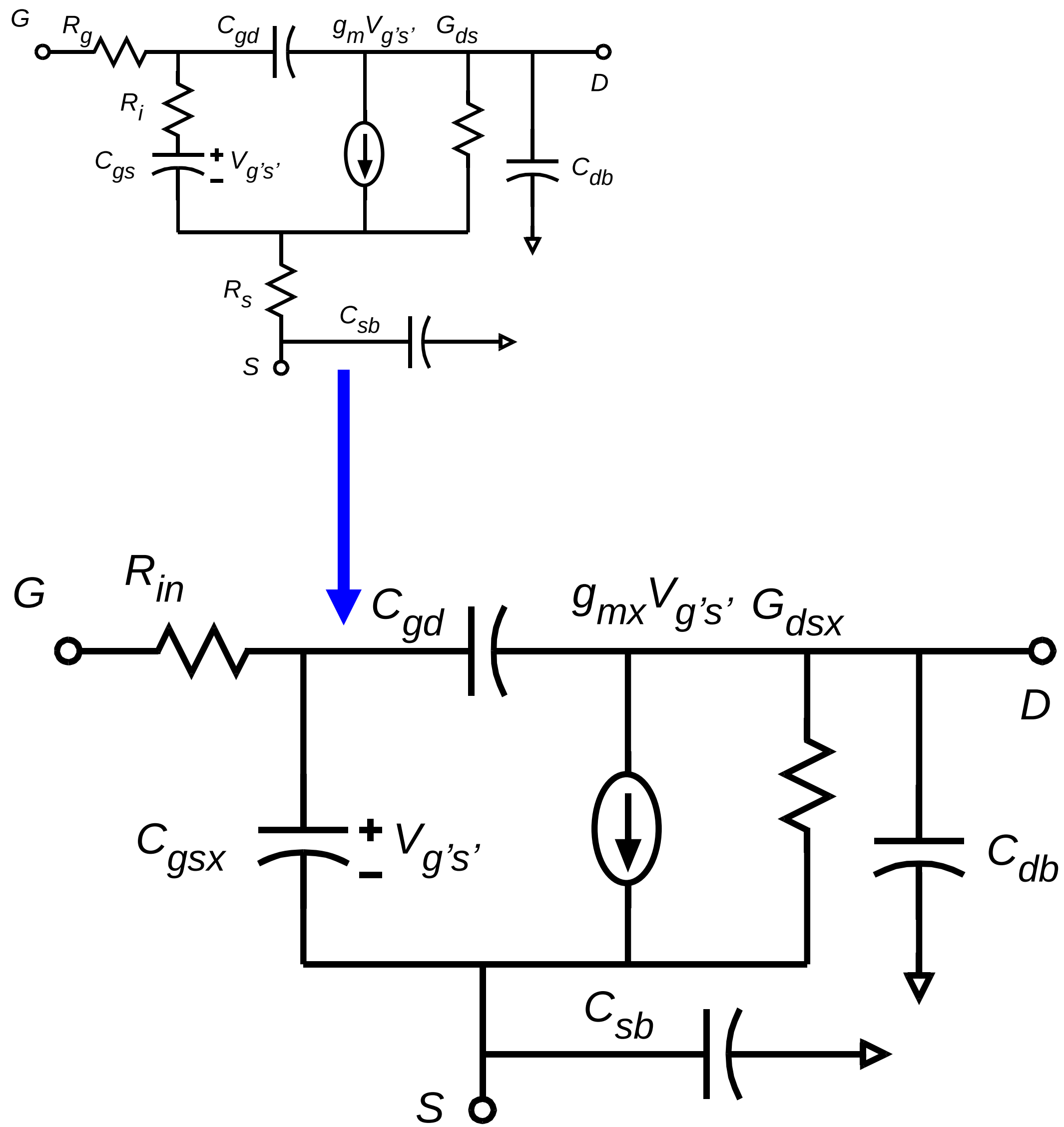
For rough hand analysis, etc

$$g_{mx} \sim \frac{g_m}{1+g_m R_s}$$

$$C_{gsx} \sim \frac{C_{gs}}{1+g_m R_s}$$

$$G_{dsx} \sim \frac{G_{ds}}{1+g_m R_s}$$

$$R_{in} \sim R_s + R_g + R_i$$



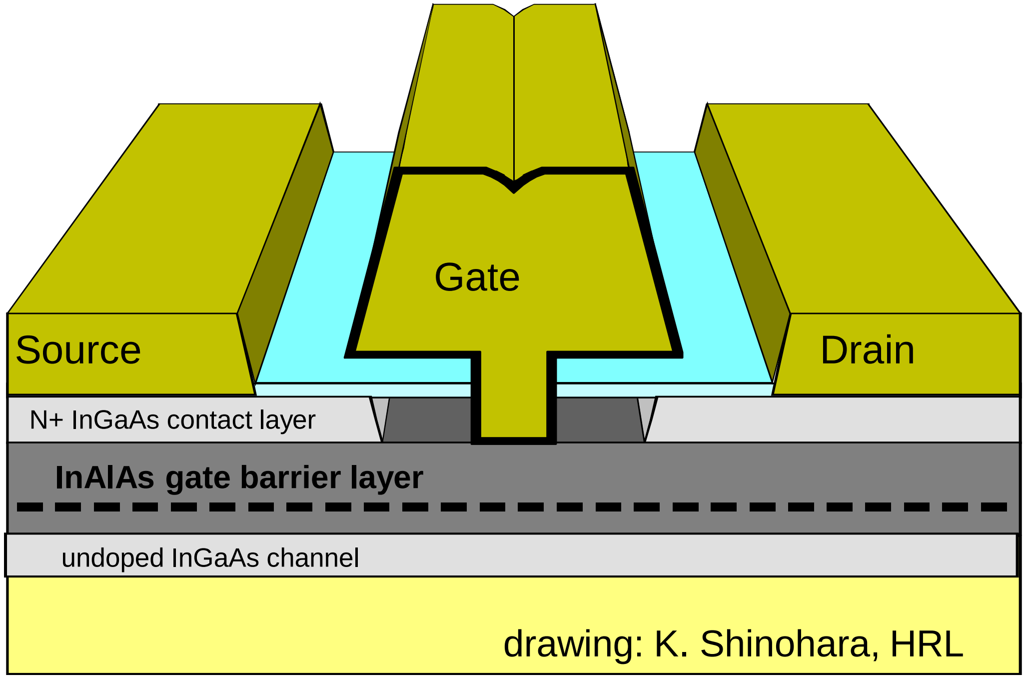
Approximate cutoff frequencies

$$1/2\pi f_\tau \sim C_{gs}/g_m + C_{gd}/g_m + (R_s + R_d)C_{gd}$$

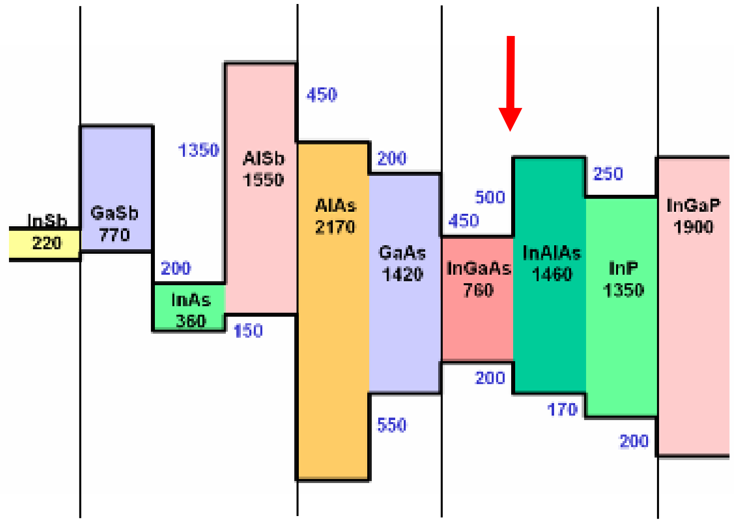
$$f_{\max} \sim \frac{f_\tau}{2\sqrt{(R_s + R_g + R_i)G_{ds} + 2\pi R_g C_{gd}}}$$

Active Devices:
III-V
Field-Effect Transistors

FET with Heterojunction for Gate Barrier → HEMT

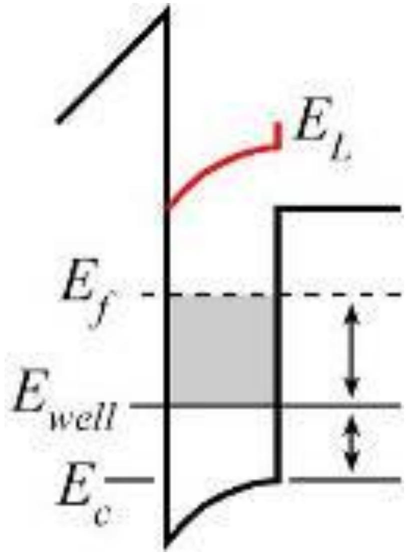


drawing : B. Brar.



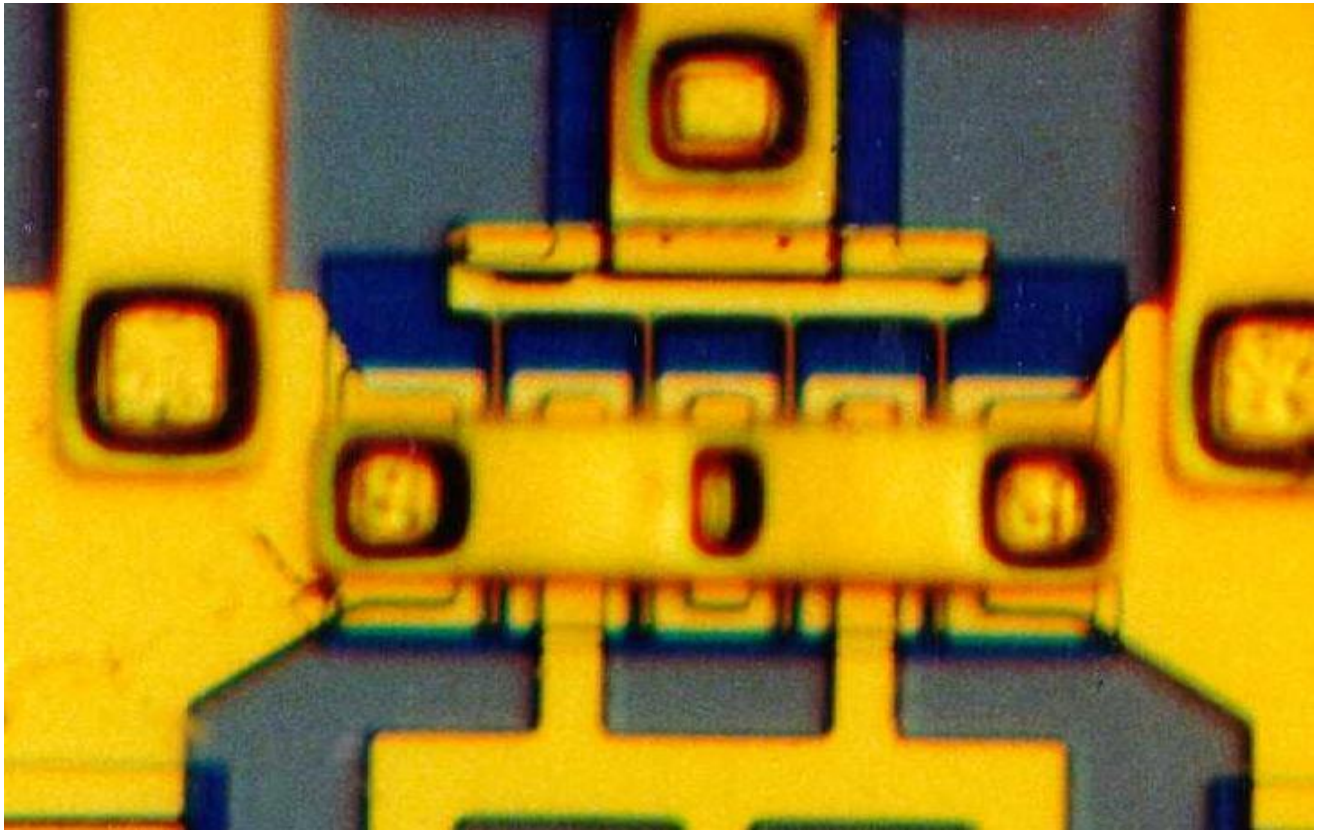
HEMT:

FET with semiconductor heterojunction for barrier between channel and gate.



HEMTs: Typical interdigitated structure

gate

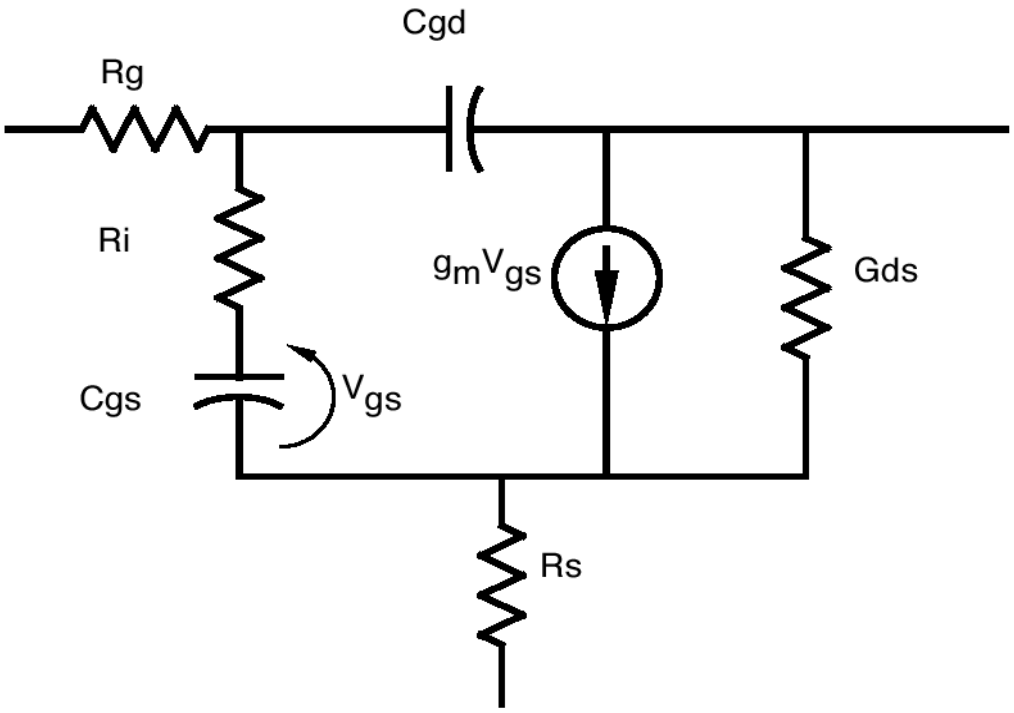


source

drain

Note multiple gate fingers.

HEMT: approximate equivalent circuit model

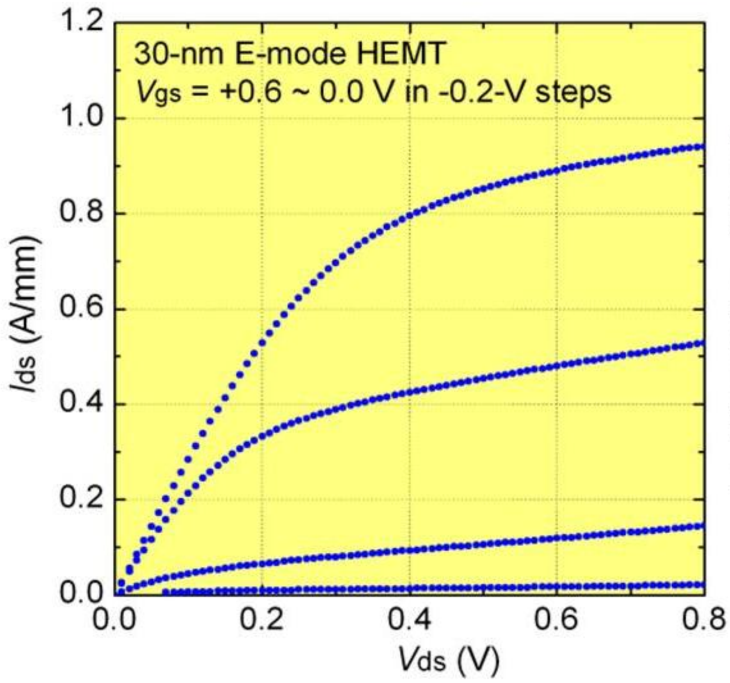


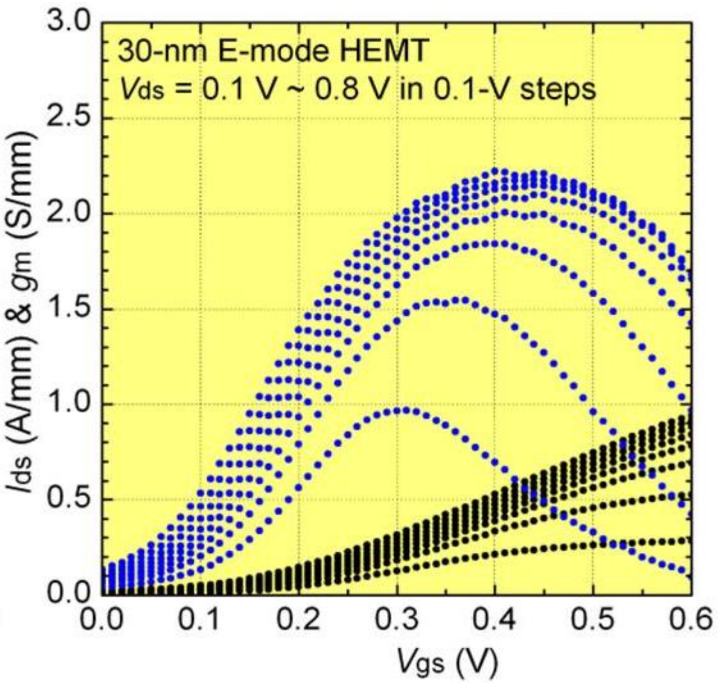
Idss. Cgs, Cgd, gm, Gds all scale proportionally with gate periphery

Ri, Rs scale proportionally with (1/ gate periphery)

Rg scales proportionally to (gate finger length)/(number fingers)

HEMT DC-IV characteristics





Data : K. Shinohara, Teledyne Scientific

Schottky diode between gate and channel;

gate will draw current for V_{gs} more positive than c.a. 0.6 V

Figures of Merit

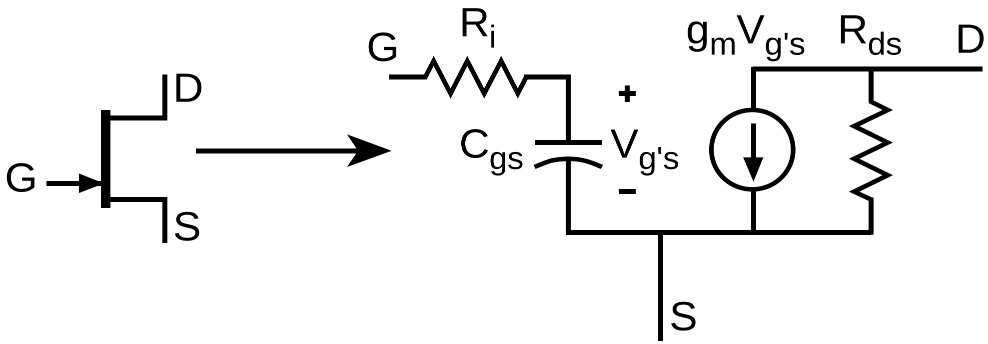
Transistor figures of Merit

Transistor small-signal bandwidth is typically stated in terms of the figures of merit f_τ and f_{max}

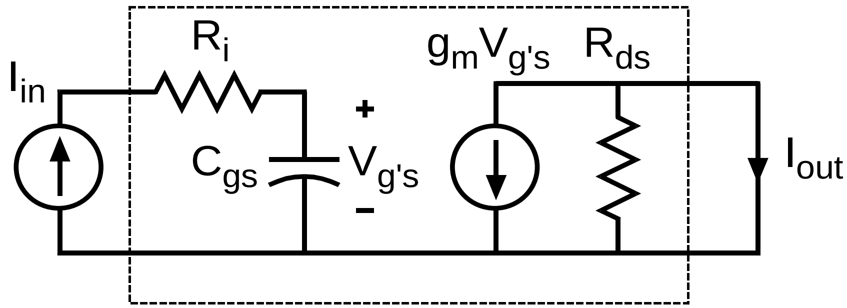
In order to understand these figures of merit, we must introduce device power gain.

These power gains will be studied in more detail
later in the course.

Definition of short-circuit current gain



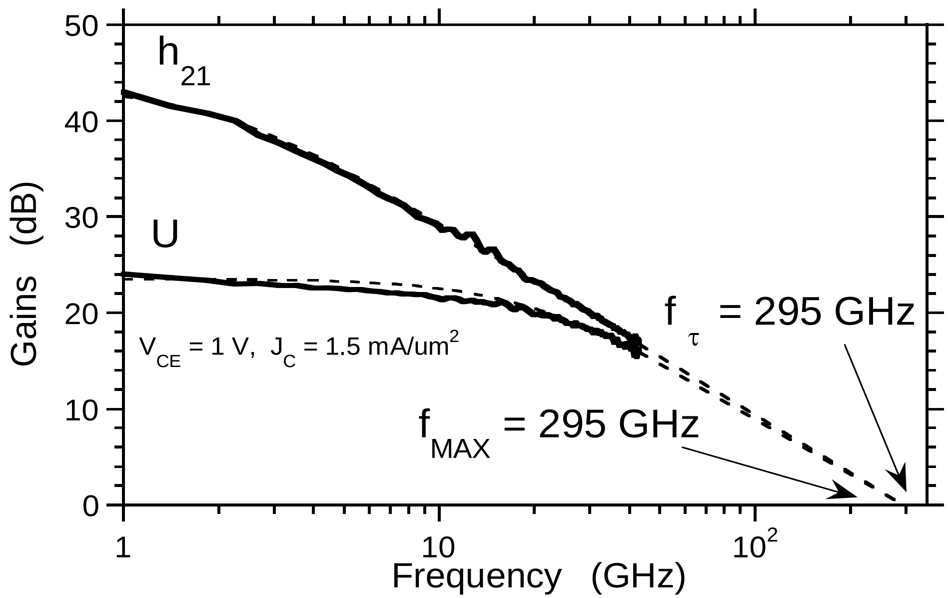
example: FET small-signal model



short-circuit current gain: drive input with AC current, short output, measure I_{out}/I_{in}

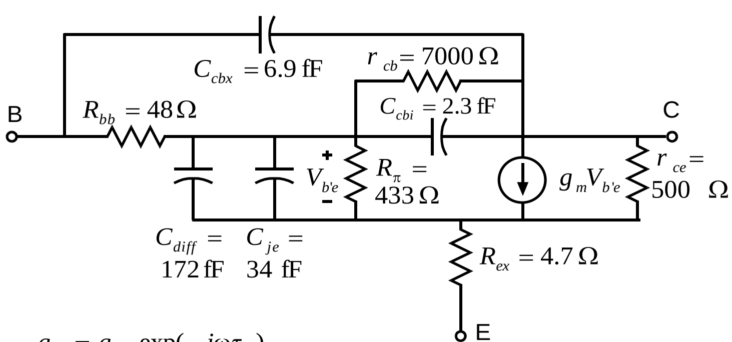
$$V_{gs} = I_{in} / j\omega C_{gs} \qquad \frac{I_{out}}{I_{in}} = \frac{g_m V_{gs}}{I_{in}} = \left(\frac{g_m}{j\omega C_{gs}}\right) = \left(\frac{f_\tau}{jf}\right)$$

Variation of H21 with frequency: Bipolar Transistors



H21 is plotted in dB. because H21 is a current gain:

$$dB(H_{21}) = 20 * \log_{10}(H_{21})$$

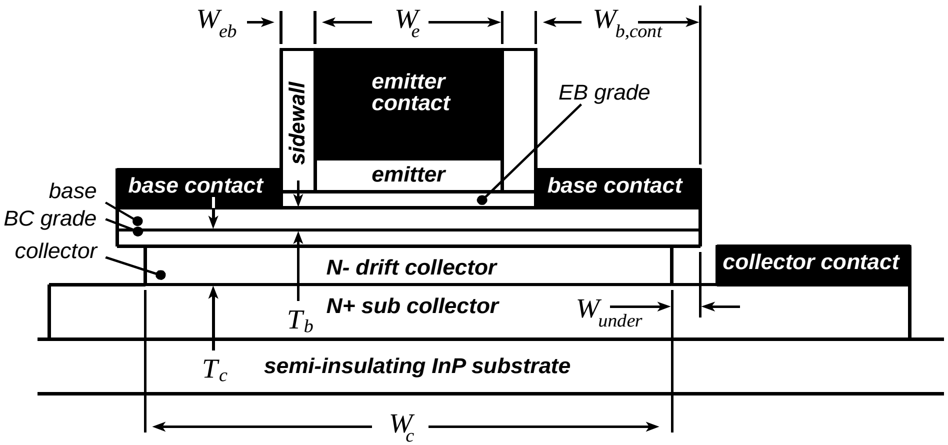


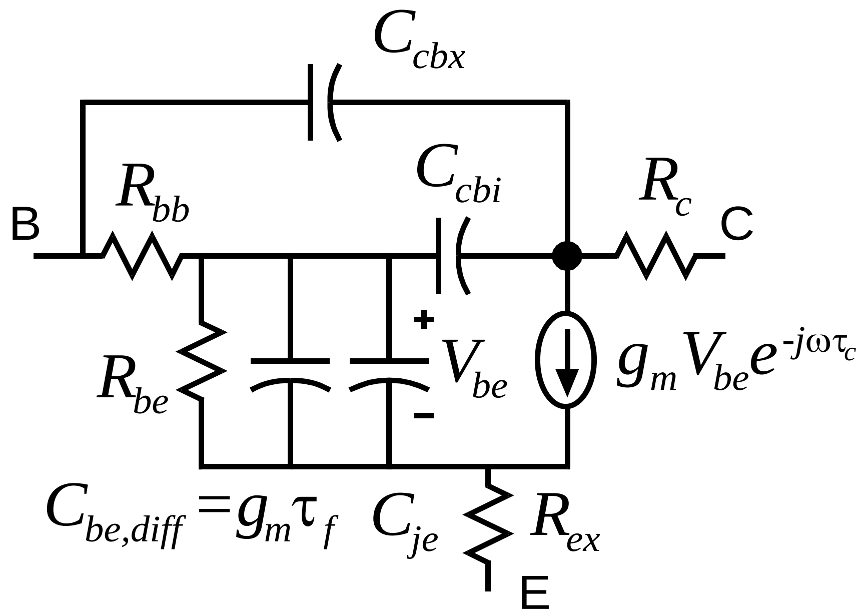
$$g_m = g_{mo} \exp(-j\omega\tau_c)$$
$$C_{diff} = g_{mo}\tau_f$$
$$R_\pi = \beta / g_m$$

Because of effect of $R_\pi = \beta / g_m$:

$$H_{21}(f) = \frac{1}{(1/\beta) + (f_\tau / jf)}$$

Current-gain cutoff frequency: Bipolar Transistors

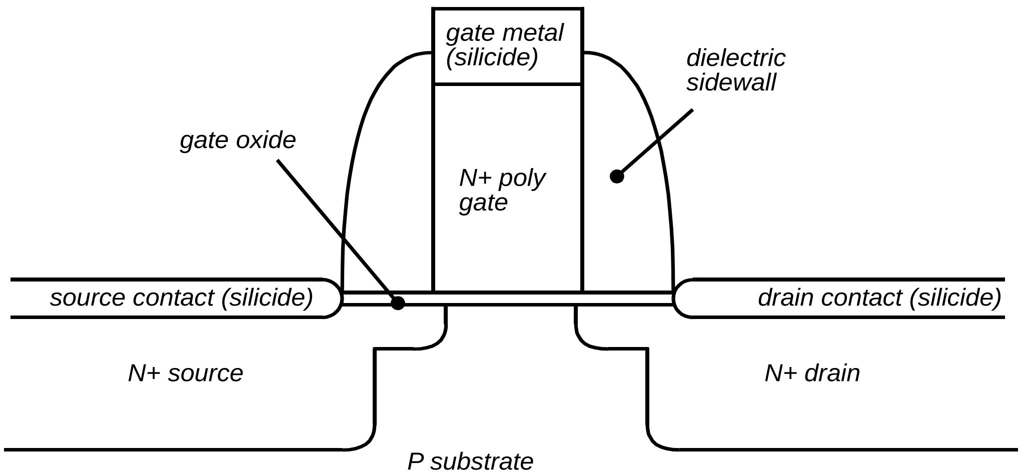


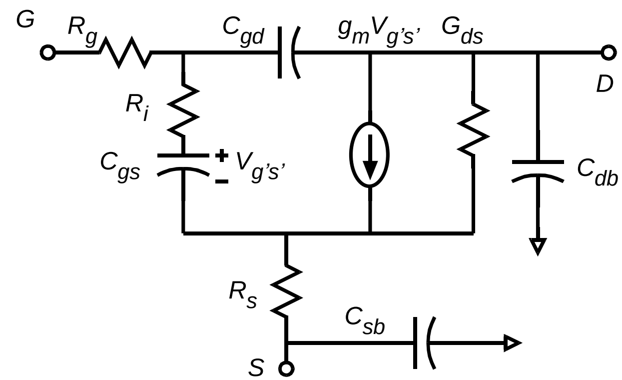


$$\frac{1}{2\pi f_\tau} = \tau_{base} + \tau_{collector} + C_{je}\frac{kT}{qI_E} + C_{bc}\left(\frac{kT}{qI_E} + R_{ex} + R_{coll}\right)$$

$$\tau_{base} \approx T_b^2 / 2D_n \qquad \tau_{collector} \approx T_c / 2v_{sat}$$

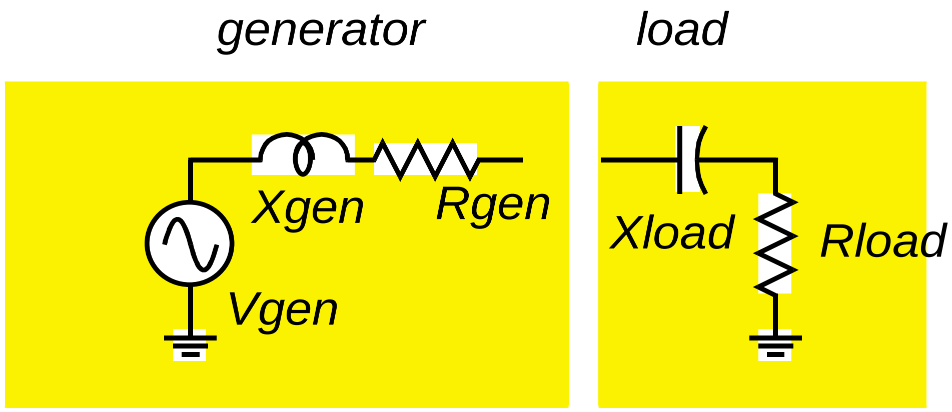
Current-gain cutoff frequency: Field-Effect Transistors





$$f_\tau \cong \frac{g_m}{2\pi(C_{gs}+C_{gd})}$$

Maximum Power Transfer Theorem



Maximum power is transferred from generator to load if

$X_{load} = -X_{gen}$ and $R_{load} = R_{gen}$

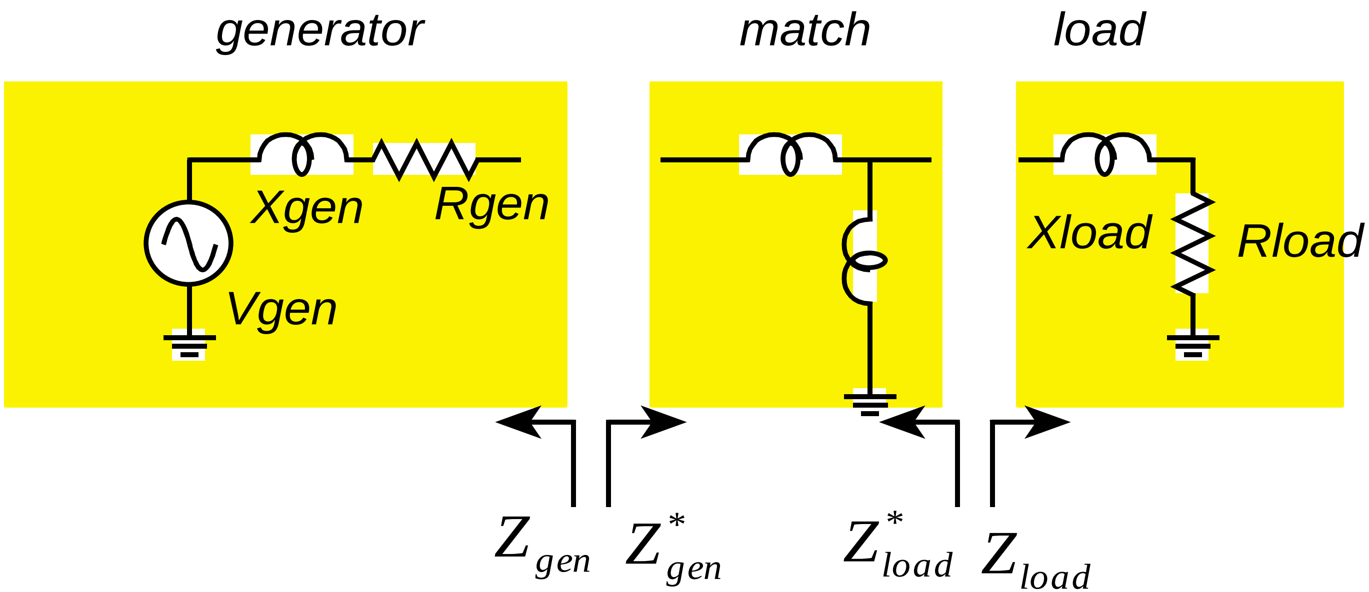
this is called *** conjugate impedance matching ***

The power delivered, called the available generator power is

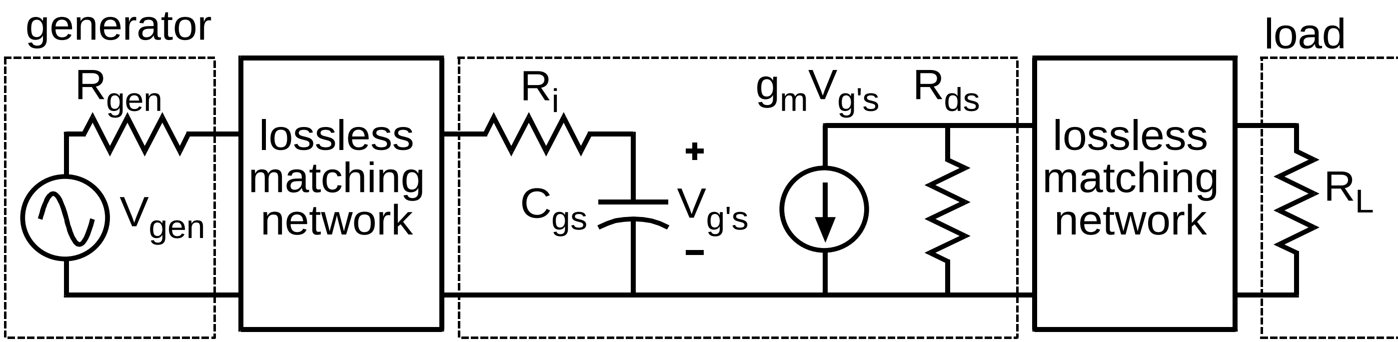
$$P_{avg} = \frac{V^2_{gen,(RMS)}}{4R_{gen}}$$

Impedance Matching

Maximum power transfer can be obtained by adding a ***lossless*** (no resistances) impedance matching network between the generator and the load:



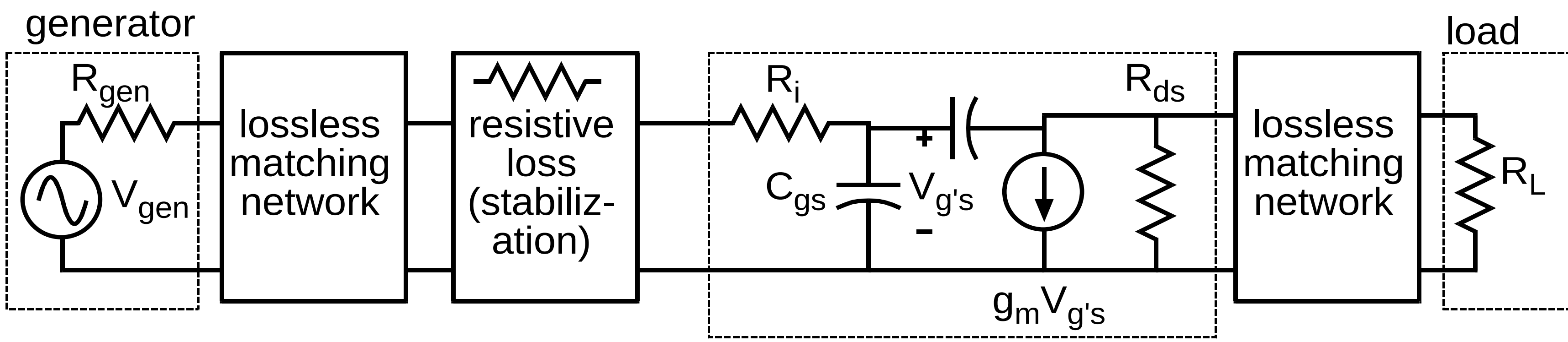
Maximum Available Power Gain (if it exists)



The transistor or amplifier is connected to generator and load via lossless matching networks. If it is possible to match at both input and output, then the power gain is called the *maximum available gain* (MAG)

Detailed microwave circuit theory (see later notes) indicates that this procedure often produces an oscillator (if the device is “potentially unstable”) . In that case we must define ***Maximum stable gain***

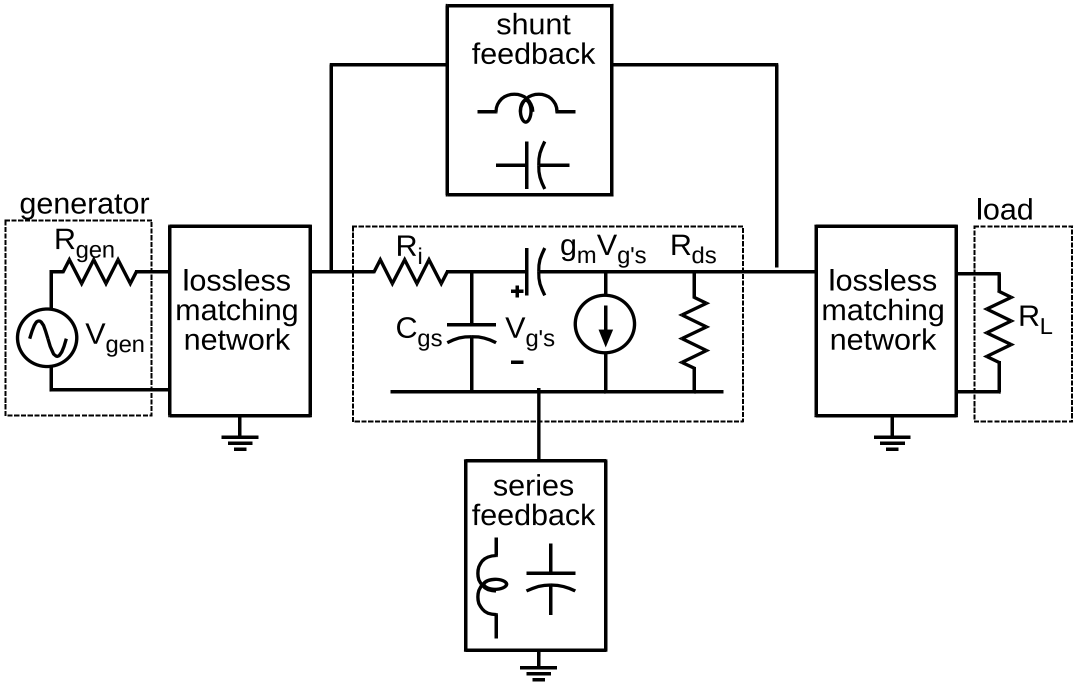
Maximum Stable Power Gain (if MAG does not exist)



If the device is potentially unstable (usually due to strong feedback through Cgd as indicated), addition of a minimum amount of series/shunt resistance to the device input/output will prevent oscillation, and the device can then be matched. The resulting power gain is called the

Maximum stable power gain.

Unilateral power gain

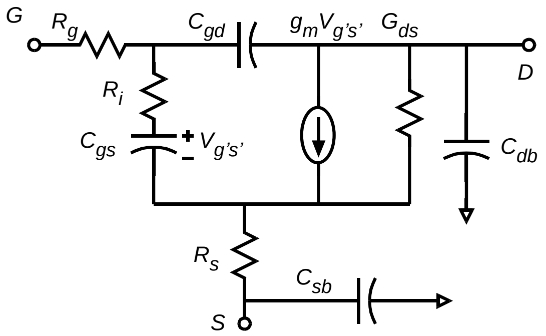


If the device is potentially unstable (due to strong feedback), addition of lossless reactive feedback as indicated can cancel the feedback and prevent oscillation. The device can then be matched. The resulting power gain is called ***Mason's invariant power gain **or** the Unilateral power gain , U.***

Power-Gain Cutoff Frequency (Fmax)

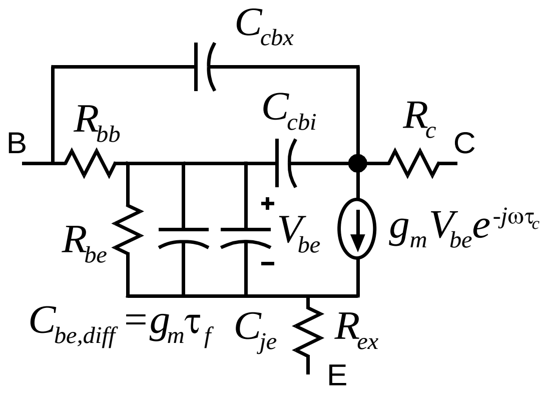
This is the frequency at which the device Unilateral power gain reaches unity.

The maximum available gain (either in the forward or reverse direction) also reaches unity at the same frequency



For Field-Effect Transistors:

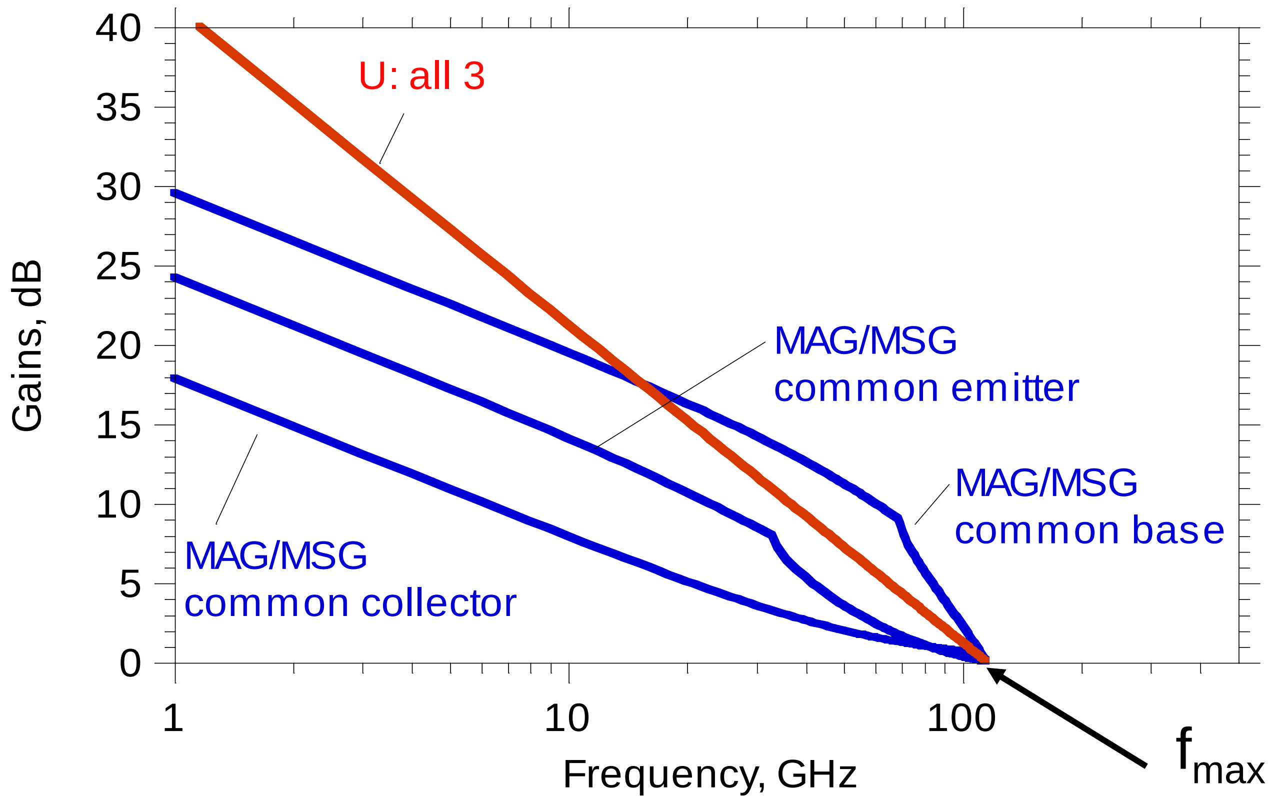
$$f_{\max} \cong \frac{f_\tau}{2\sqrt{(R_i + R_s + R_g)G_{ds} + 2\pi f_\tau R_g C_{dg}}}$$



For Bipolar Transistors (R_{ce} being large):

$$f_{\max} \cong \frac{f_\tau}{2\sqrt{R_{bb}/R_{ce} + 2\pi f_\tau R_{bb} C_{cbi}}} \rightarrow \sqrt{\frac{f_\tau}{8\pi R_{bb} C_{cbi}}}$$

Power gains of a typical transistor



The inflection in the curves is the break between unstable (MSG) at lower frequencies and stable (MAG) at higher frequencies.

MAG/MSG is directly relevant for RF/microwave/mm-wave IC design.

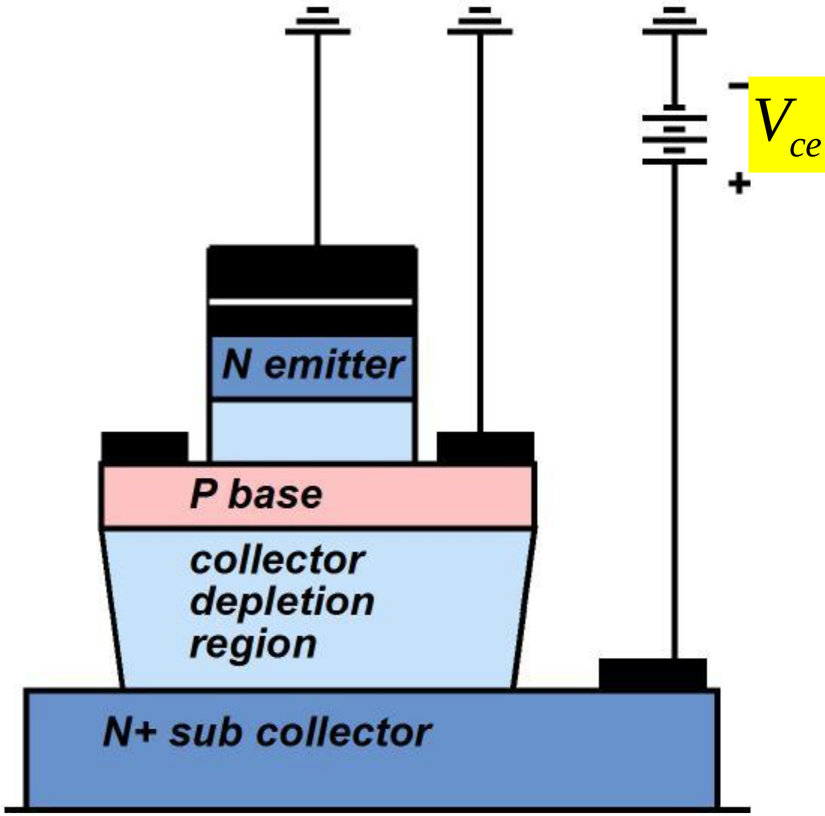
Because U has -20 dB/decade slope, it is used to extrapolate measurements to determine f_{max}

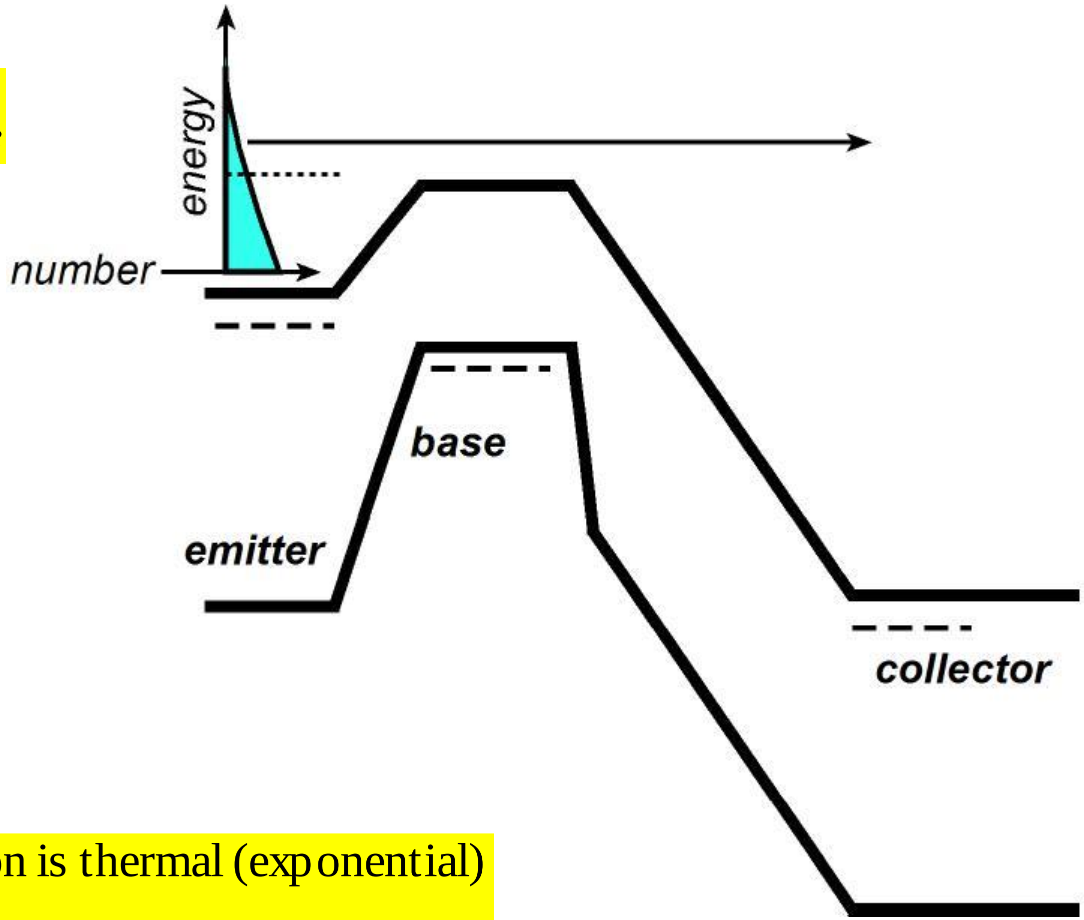
End

Appendix
(optional)

Bipolar Transistor Operation

Bipolar Transistor ~ MOSFET Below Threshold





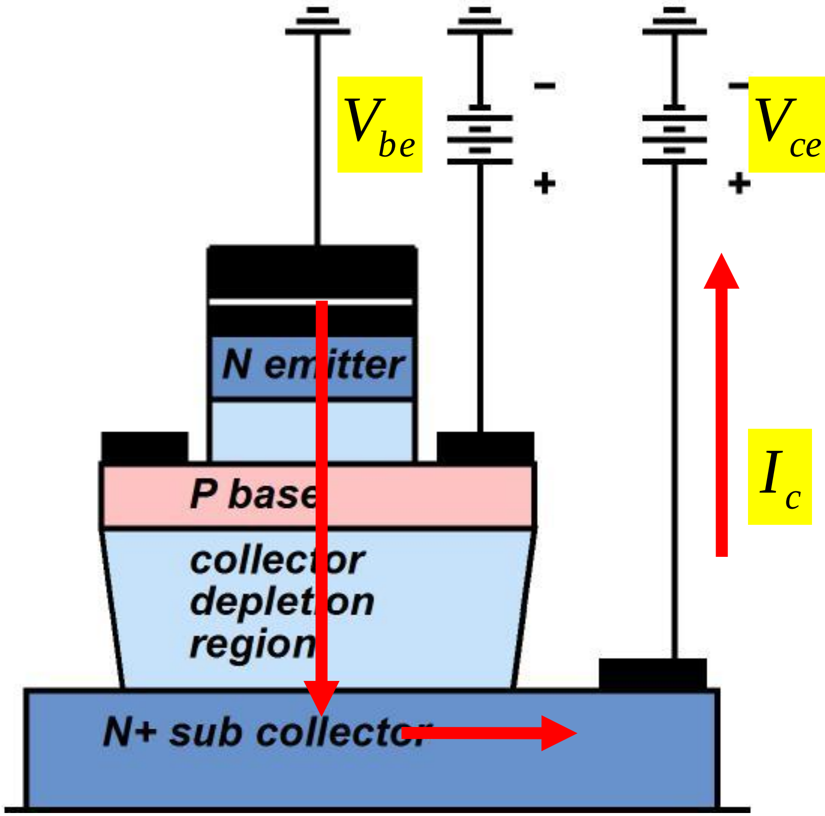
Because emitter energy distribution is thermal (exponential)

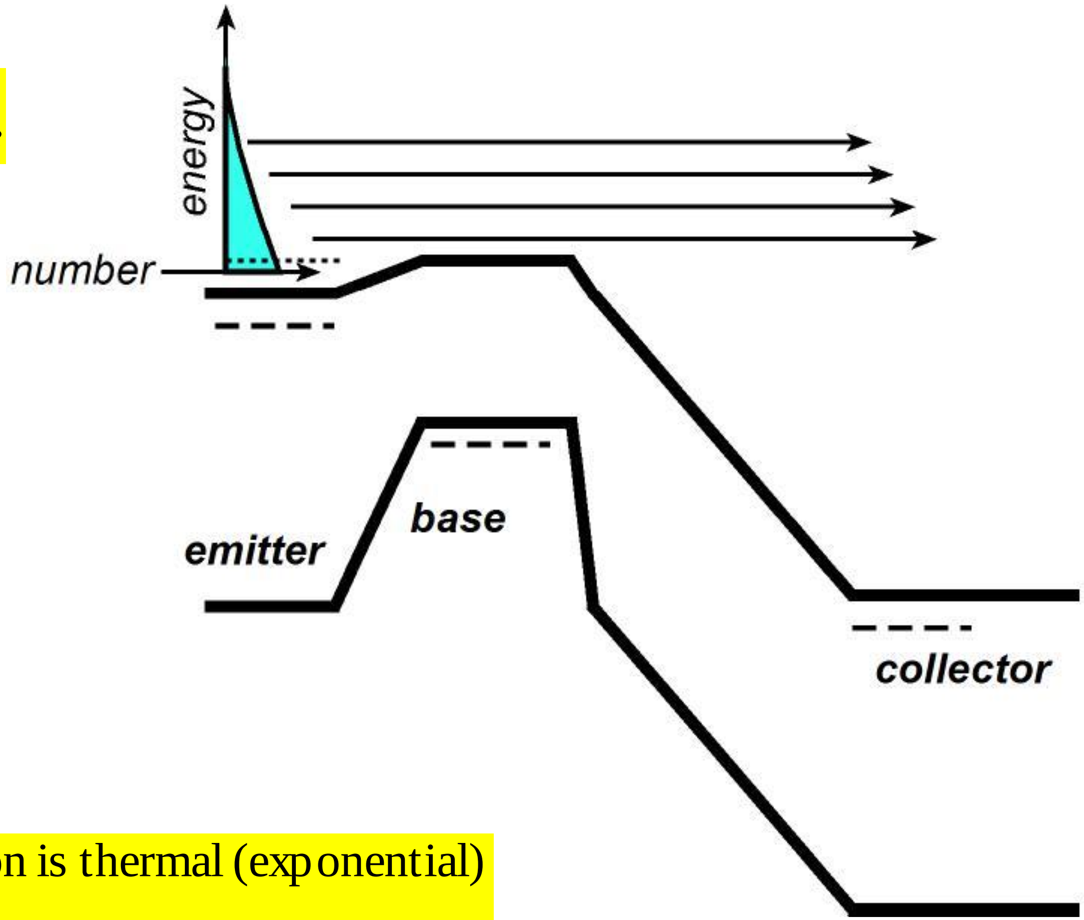
$I_c \propto \exp(qV_{be}/kT)$

Almost all electrons reaching base pass through it

$\rightarrow I_c$ varies little with collector voltage

Bipolar Transistor ~ MOSFET Below Threshold





Because emitter energy distribution is thermal (exponential)

$I_c \propto \exp(qV_{be}/kT)$

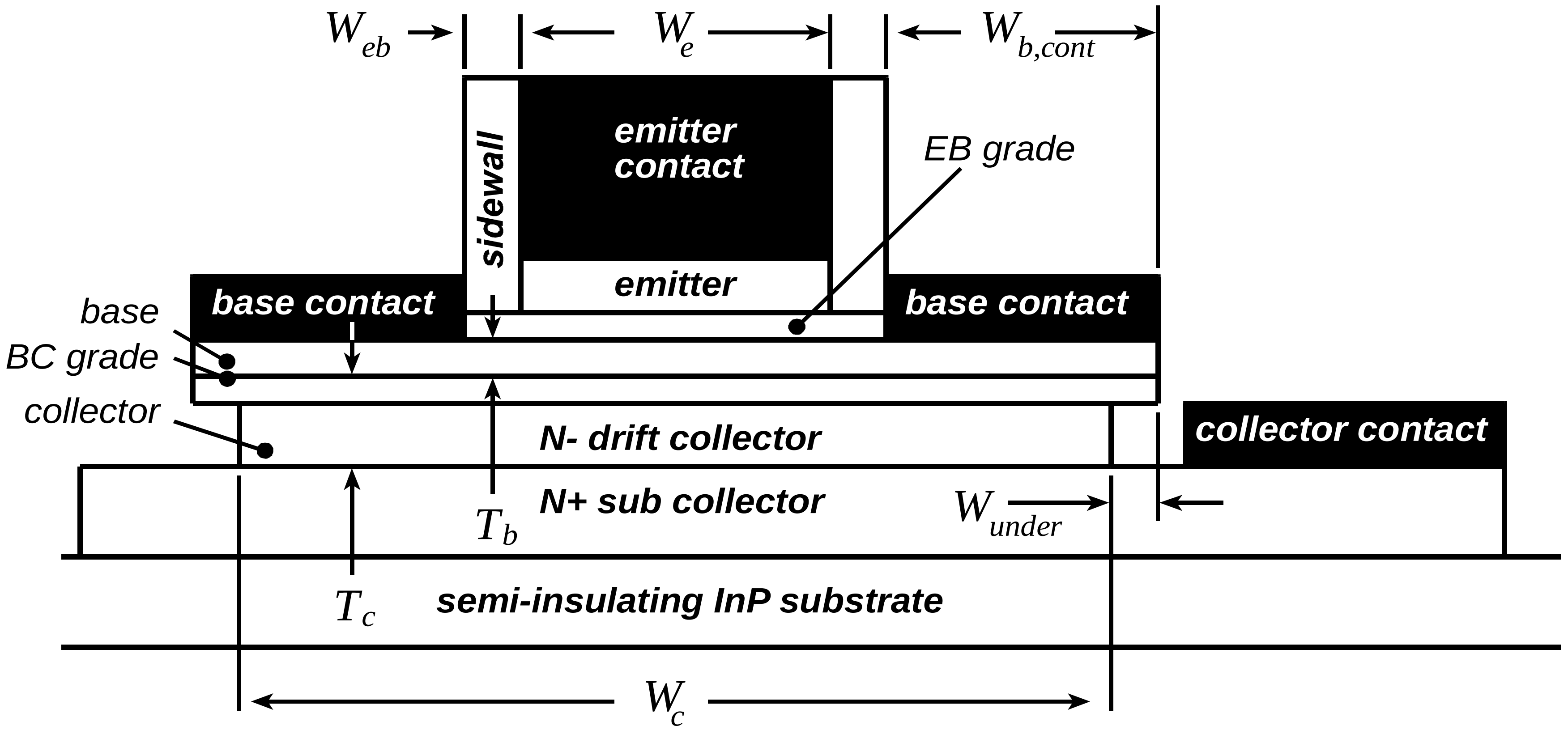
Almost all electrons reaching base pass through it

$\rightarrow I_c$ varies little with collector voltage

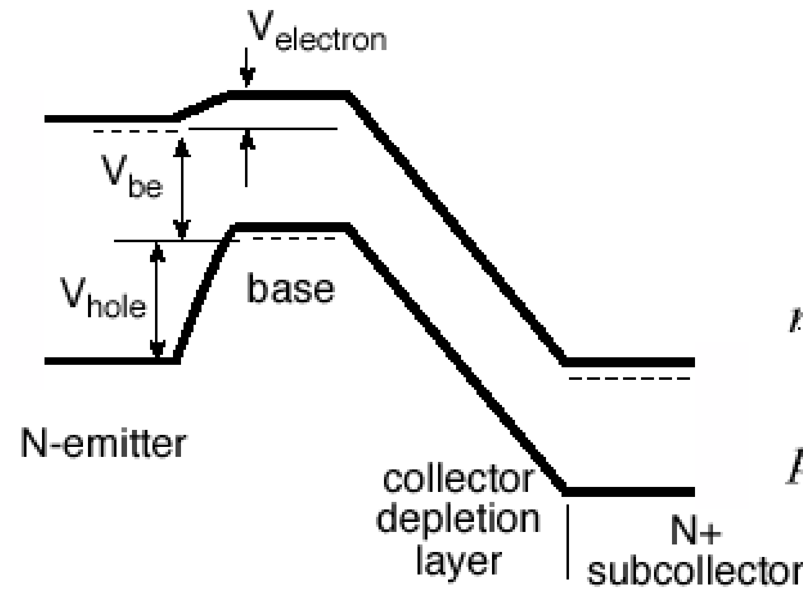
HBT Equivalent Circuit Model

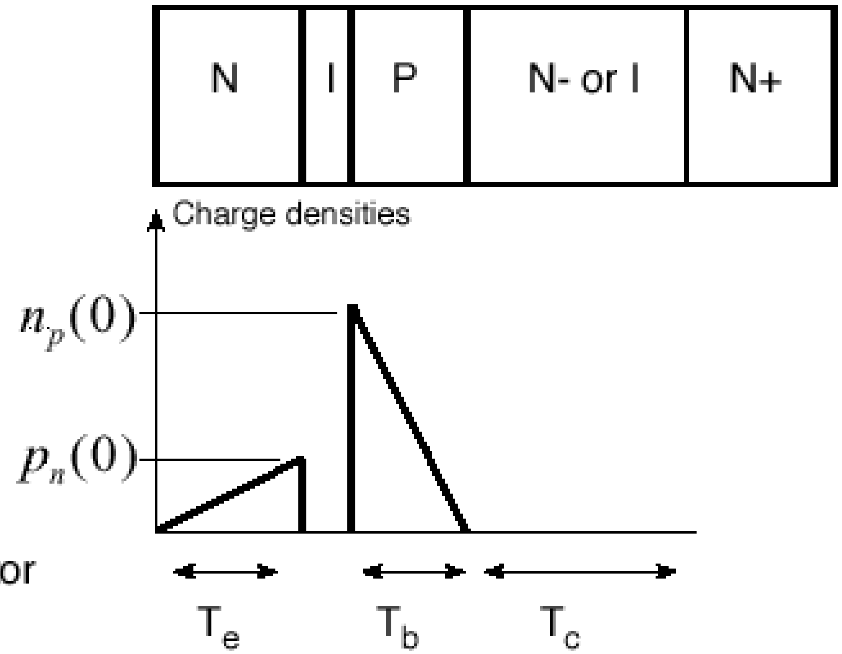
Physical structure, symbolic

$$\text{Device Stripe Length} = L_E$$
perpendicular to drawing



Bipolar Transistor DC-IV Characteristics





$$n_p(0) = qN_c e^{-qV_{electron}/kT} \propto e^{+qV_{be}/kT}$$

electron concentration at emitter edge of base

$$p_n(0) = qN_v e^{-qV_{hole}/kT} \propto e^{+qV_{be}/kT}$$

hole concentration at base edge of emitter
heterojunction makes this small

$$I_{electron} = \frac{D_n q A_e N_c}{T_b} e^{-qV_{electron}/kT} \propto e^{+qV_{be}/kT}$$

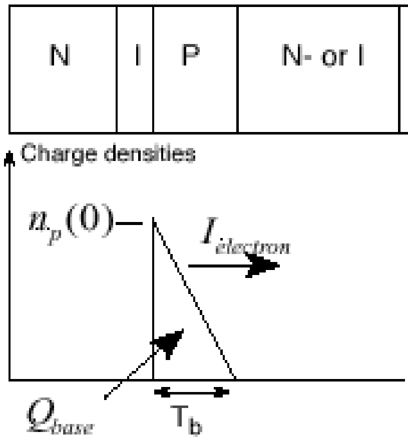
electron current from emitter to collector

$$g_m \equiv \frac{dI_c}{dV_{be}} = \frac{qI_c}{kT}$$

transconductance

Bipolar Transistor: Carrier Transit Times

Base Transit Time



electron concentration at emitter edge of base

$$n_p(0) = qN_c e^{-qV_{electron}/kT} \propto e^{+qV_{be}/kT}$$

electron current from emitter to collector

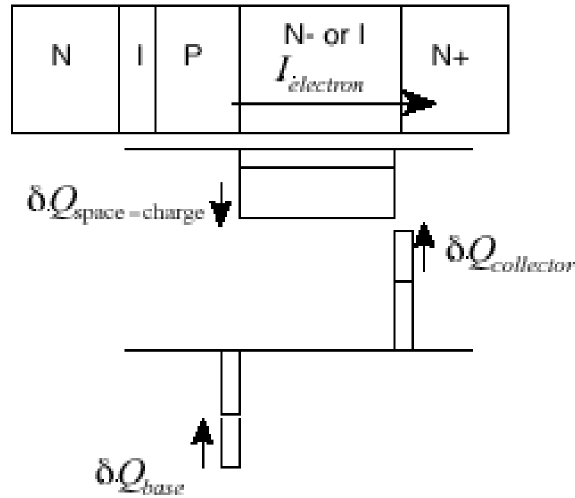
$$I_{electron} = qn_p(0)D_n / T_b$$

stored base charge

$$Q_{base} = qA_e n_p(0)T_b / 2$$

$$= I_{electron}T_b^2 / 2D_n = \tau_b I_{electron}$$

Collector Transit Time



depletion-layer space-charge

$$\delta Q_{space-charge} = \frac{T_c}{v_{sat}} \delta I_{collector}$$

change in base stored charge

$$\delta Q_{base} = \delta Q_{collector} = \delta Q_{space-charge} / 2$$

$$= \delta I_{collector}(T_c / 2v_{sat}) = \tau_c \delta I_{collector}$$

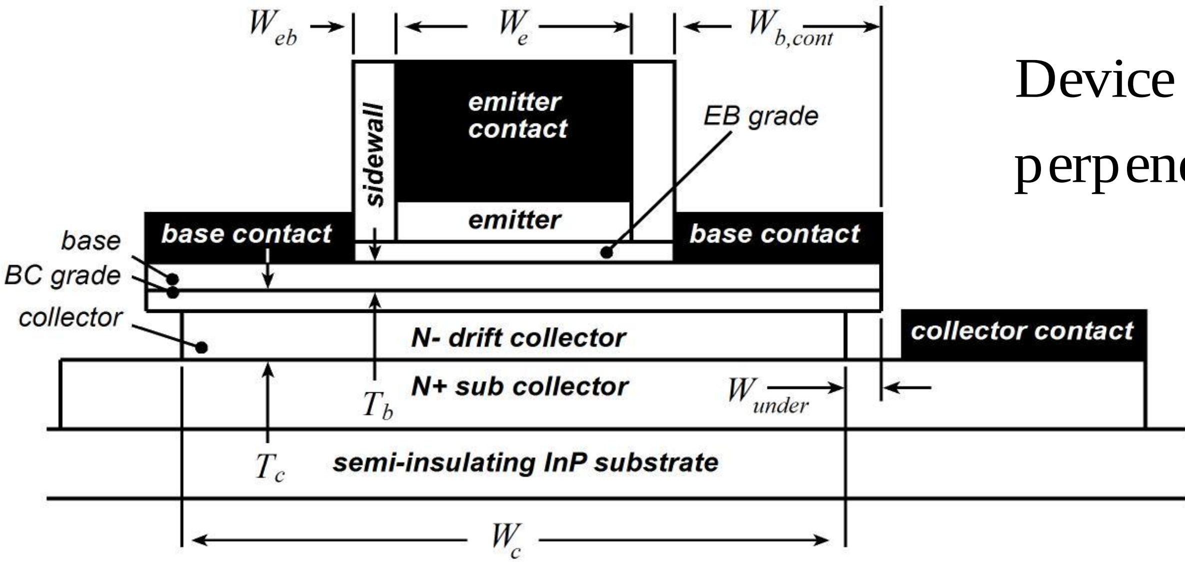
"Diffusion Capacitance"

$$C_{diffusion} \equiv \frac{dQ_{base}}{dV_{be}} = \frac{dQ_{base}}{dI_c}\frac{dI_c}{dV_{be}} = (\tau_b + \tau_c)g_m$$

$$C_{\text{be, diffusion}} = g_m(\tau_b + \tau_c)$$

fictitious capacitance between base & emitter modelling charge storage

Base resistance & collector-base capacitance



Device Stripe Length $= L_E$ perpendicular to drawing

$$R_{bb} \cong \text{contact term} + \text{spreading under contact} + \text{spreading under emitter}$$

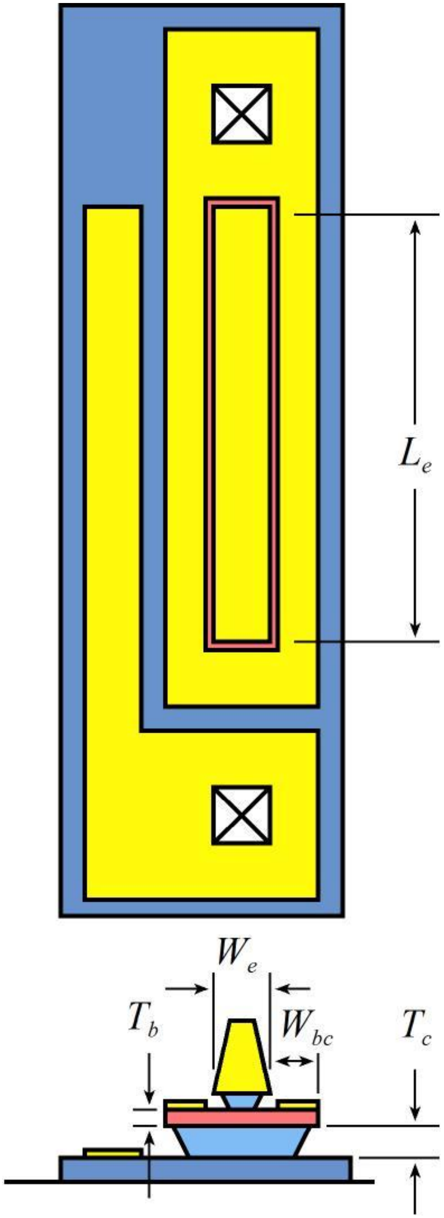
$$R_{bb} \cong \frac{\rho_{contact}}{2 \cdot L_E \cdot W_{b,cont}} + \frac{1}{6}\frac{W_{b,contact}}{L_E}\rho_{base\_sheet} + \frac{1}{12}\frac{W_E}{L_E}\rho_{base\_sheet}$$

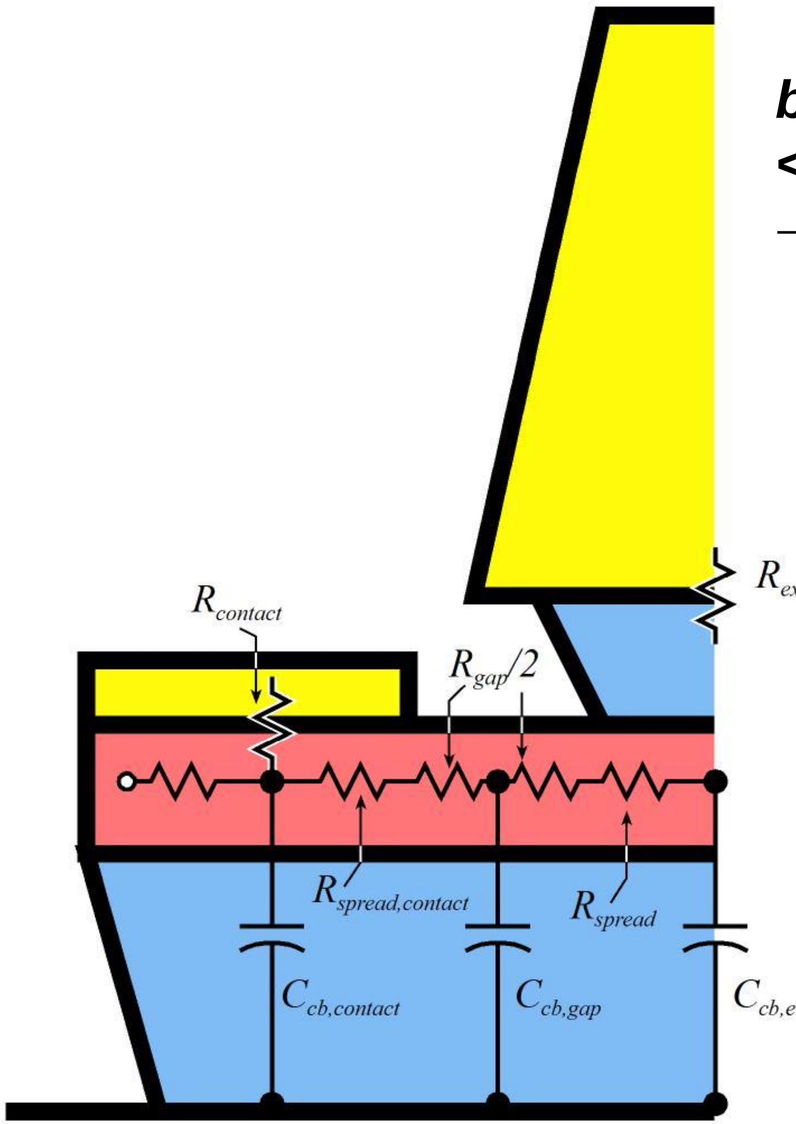
$$C_{cb} \cong \frac{\varepsilon_{\text{semiconductor}} W_c L_e}{T_c}$$

R_{bb} and C_{cb} are distributed $\rightarrow$ splitting of C_{cb} into C_{cbx} and C_{cbi}

Details beyond scope of class (see Rodwell IEEE EDL Nov. 2001, Proc. IEEE Feb. 2008

HBT RC Parasitics

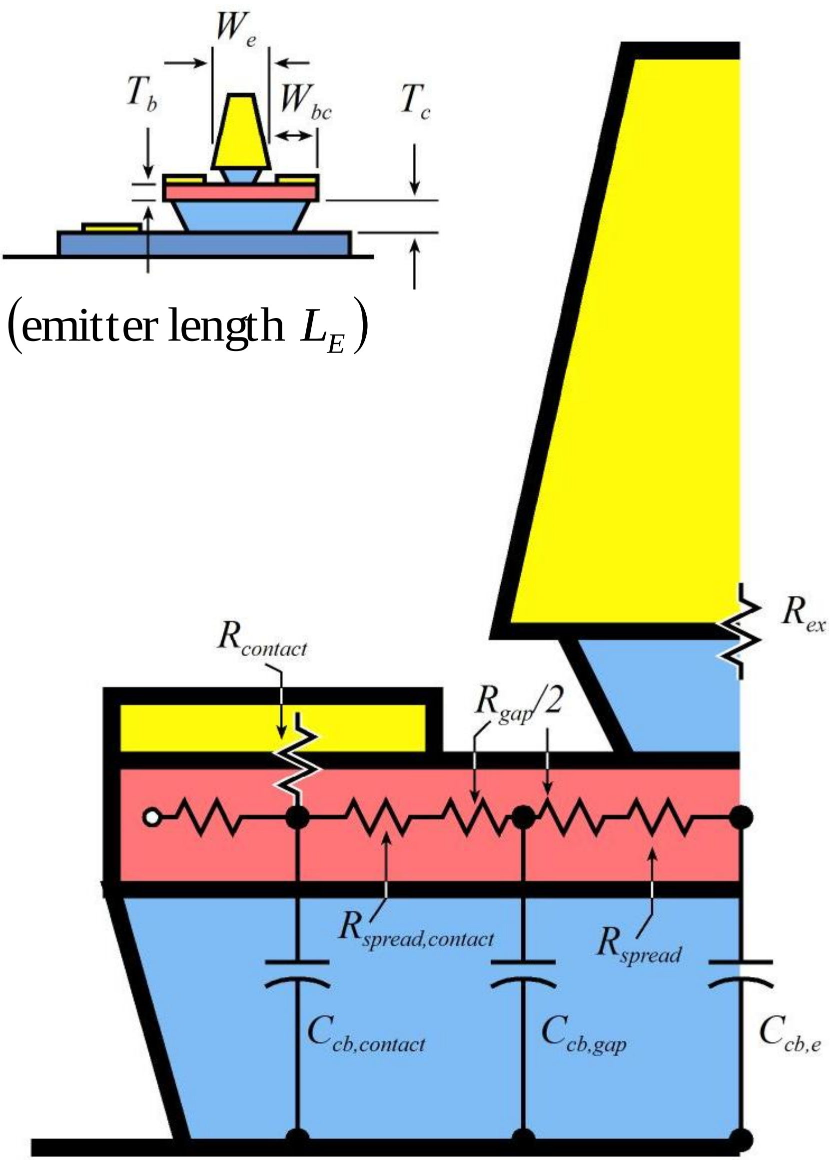




base contact width < 2 transfer lengths → simple analysis

Limiting case of Pulfrey / Vaidyanathan f_{max} model.

HBT RC Parasitics



$$R_{ex} = \rho_{contact,emitter} / A_{emitter}$$

$$R_{spread} = \rho_s W_e / 12 L_E$$

$$R_{gap} = \rho_s W_{gap} / 4 L_E$$

$$R_{spread,contact} = \rho_s W_{bc} / 6 L_E$$

$$R_{contact} = \rho_{contact,base} W_{bc} / A_{base\_contacts}$$

$$C_{cb,e} = \varepsilon A_{emitter} / T_c$$

$$C_{cb,gap} = \varepsilon A_{gap} / T_c$$

$$C_{cb,contact} = \varepsilon A_{base\_contacts} / T_c$$

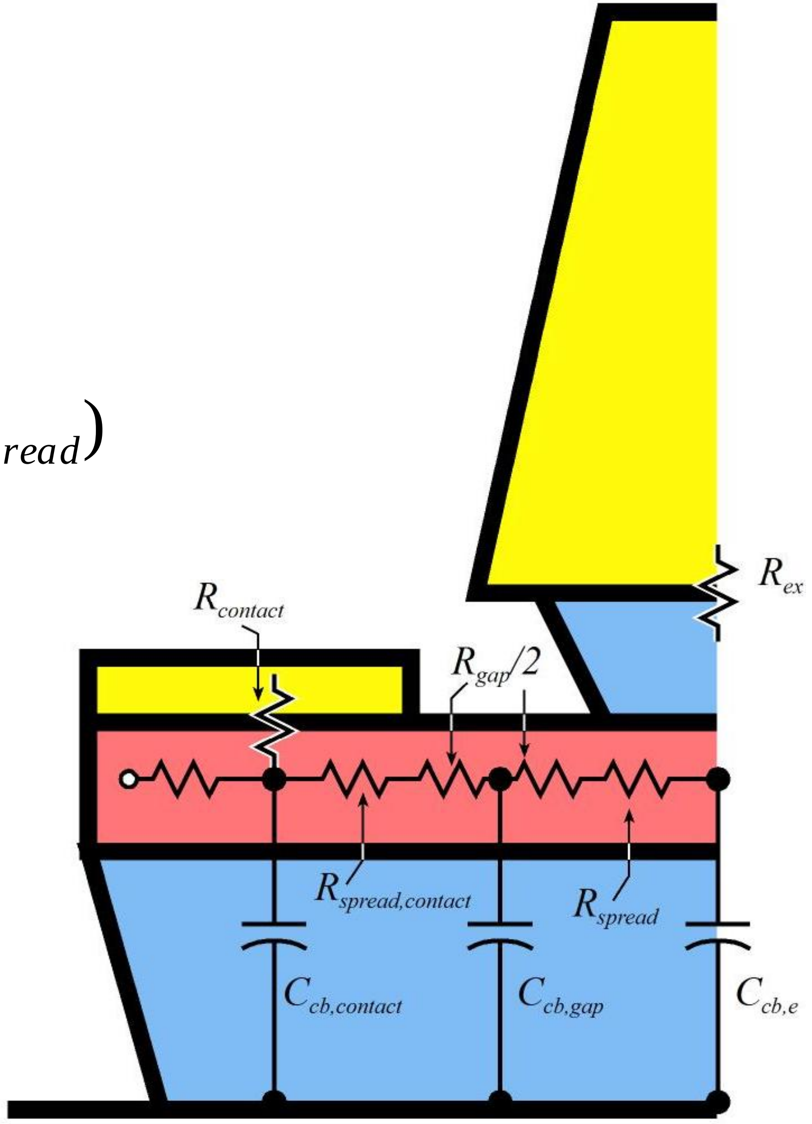
Base-Collector Time Constant & Fmax.

$$f_{\max} \cong \sqrt{\frac{f_\tau}{8\pi R_{bb} C_{cbi}}} \text{ where}$$

$$\tau_{cb} = R_{bb} C_{cbi} = C_{cb,contact} R_{contact}$$

$$+ C_{cb,gap}(R_{contact} + R_{spread,contact} + R_{gap}/2)$$

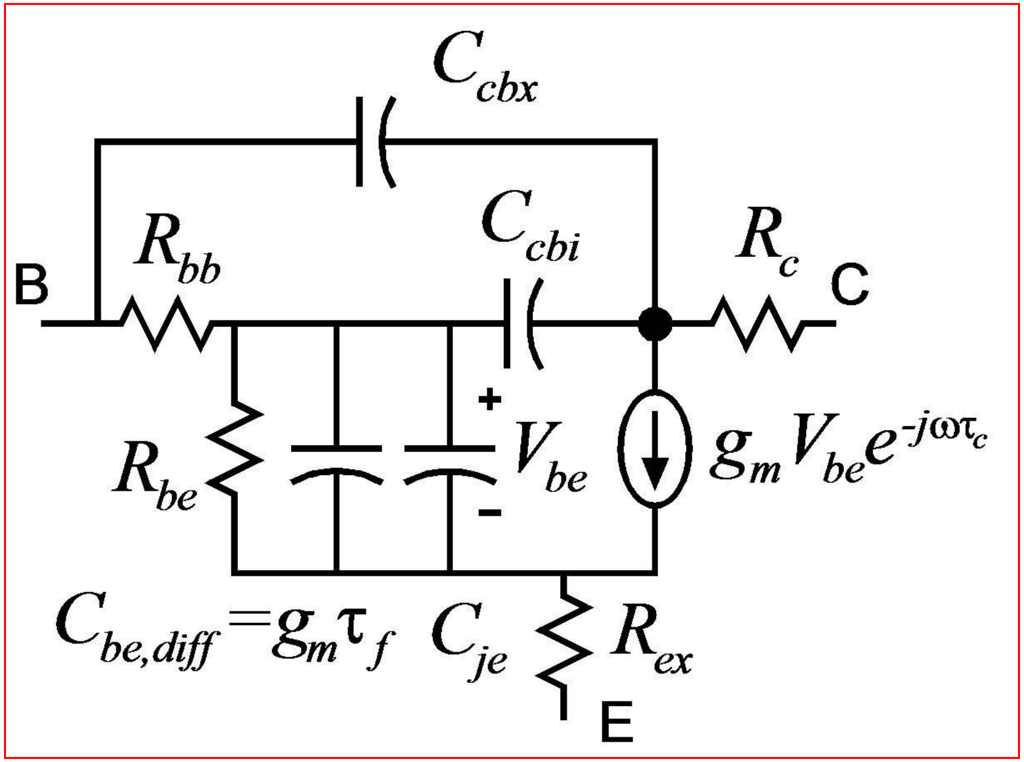
$$+ C_{cb,e}(R_{contact} + R_{spread,contact} + R_{gap} + R_{spread})$$

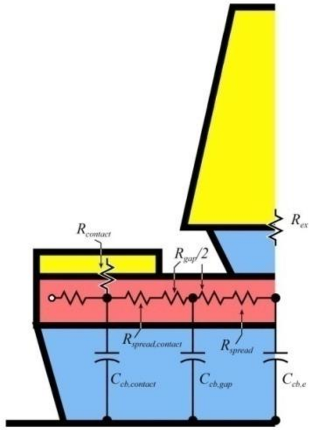


Relationship to HBT Equivalent Circuit Model

$$C_{cbx} + C_{cbi} = C_{cb,e} + C_{cb,gap} + C_{cb,contact}$$

$$R_{bb} = R_{spread} + R_{gap} + R_{contact,spread} + R_{contact}$$

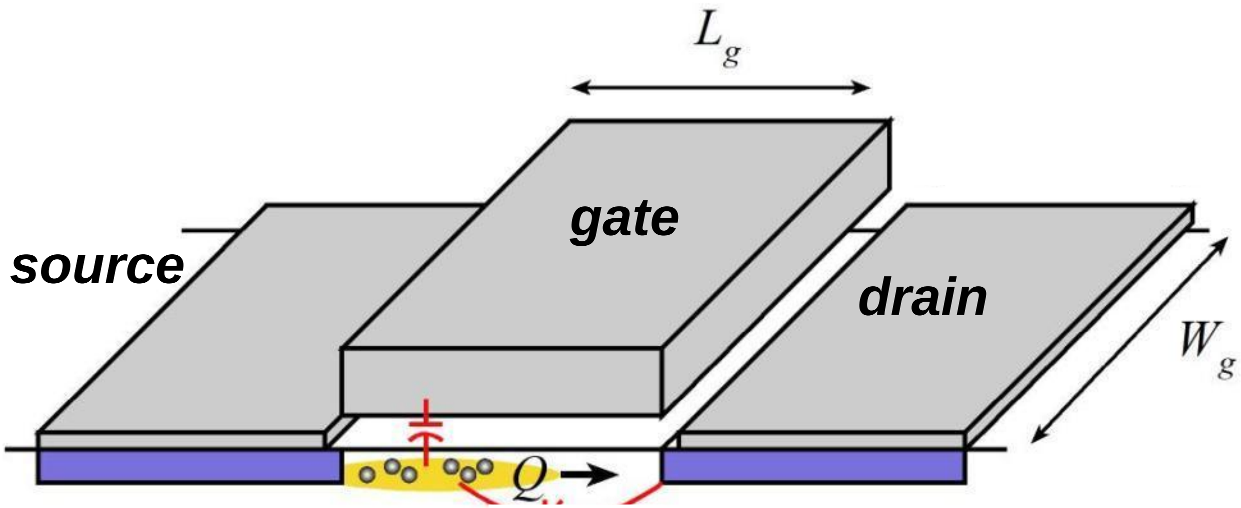


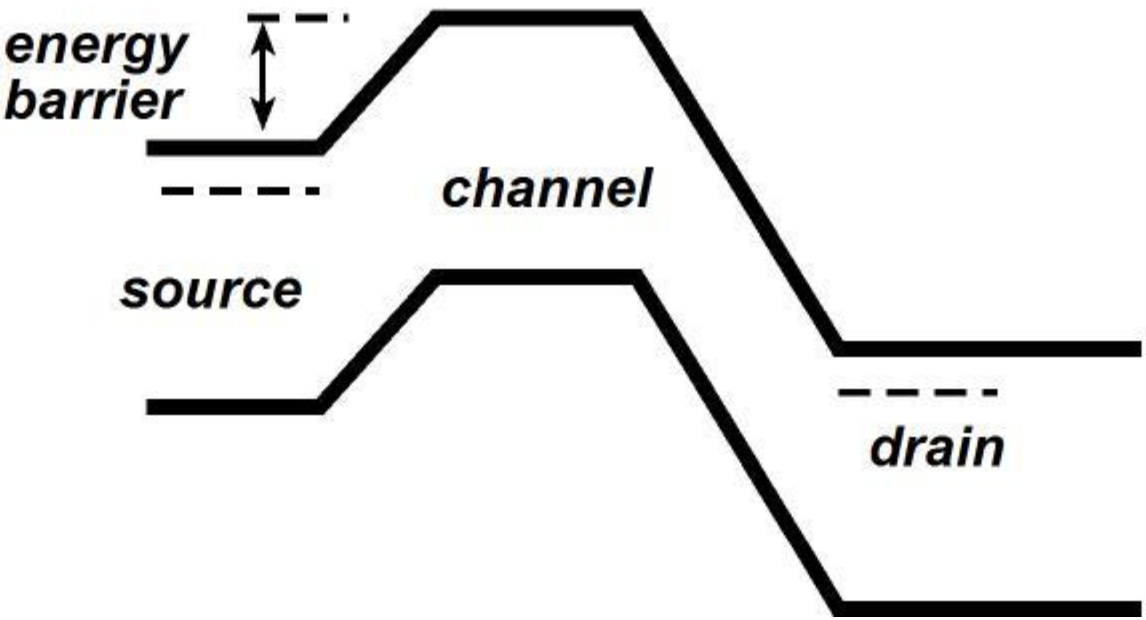


$$R_{bb}C_{cbi} = C_{cb,contact}R_{contact} + C_{cb,gap}(R_{contact} + R_{spread,contact} + R_{gap}/2)$$
$$+ C_{cb,e}(R_{contact} + R_{spread,contact} + R_{gap} + R_{spread})$$

Field-Effect Transistor Operation (Approximate)

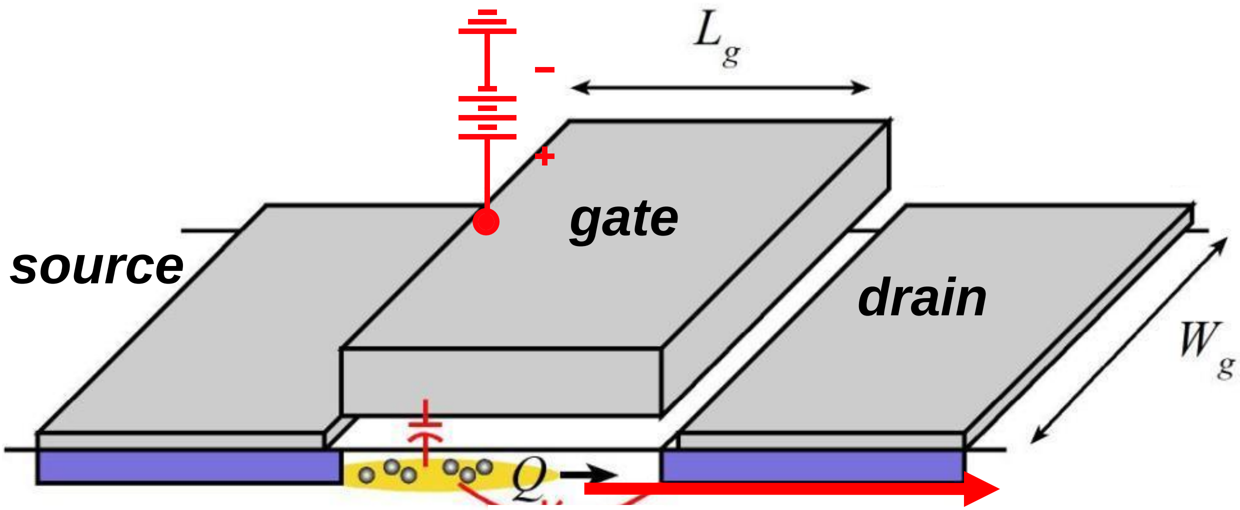
Field-Effect Transistor Operation

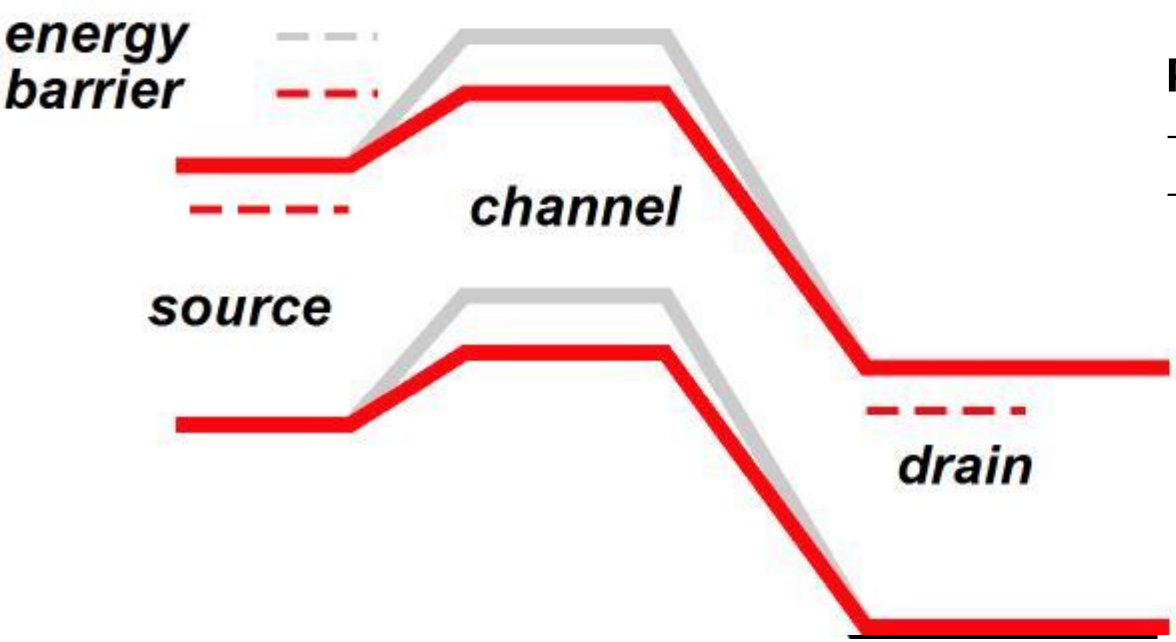




Positive Gate Voltage
→ reduced energy barrier
→ increased drain current

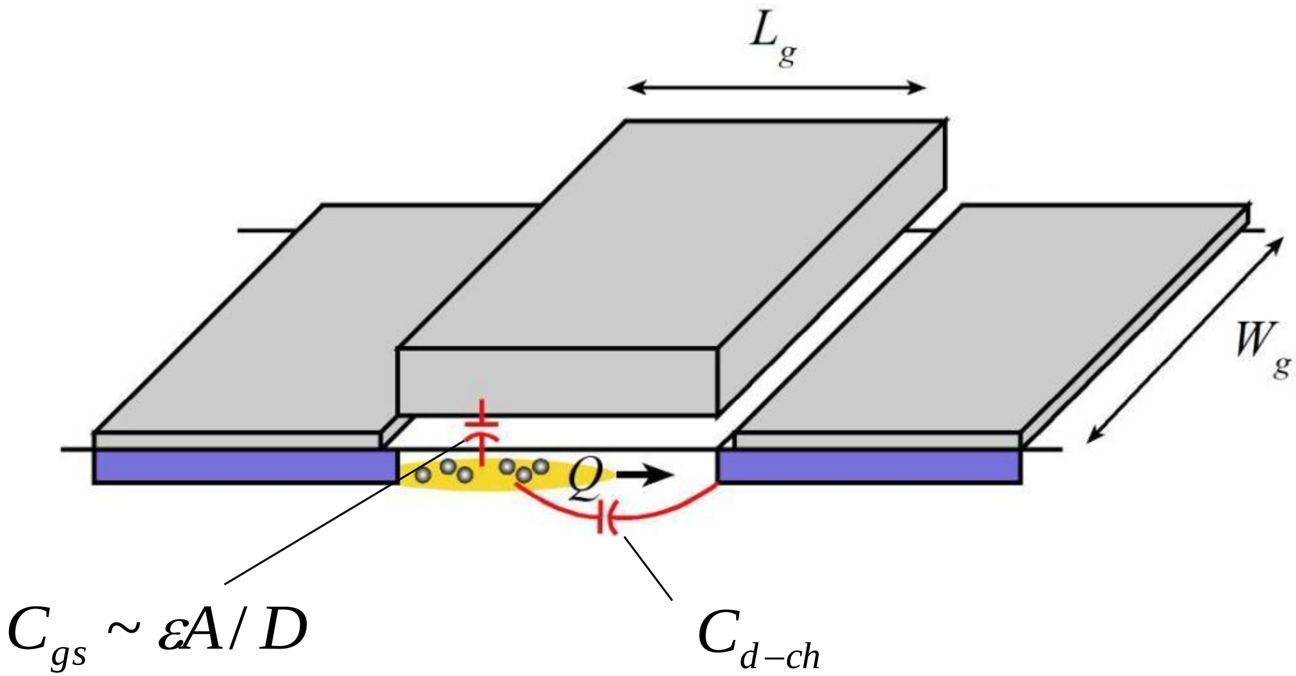
Field-Effect Transistor Operation





Positive Gate Voltage
→ reduced energy barrier
→ increased drain current

FETs: Basic Operation

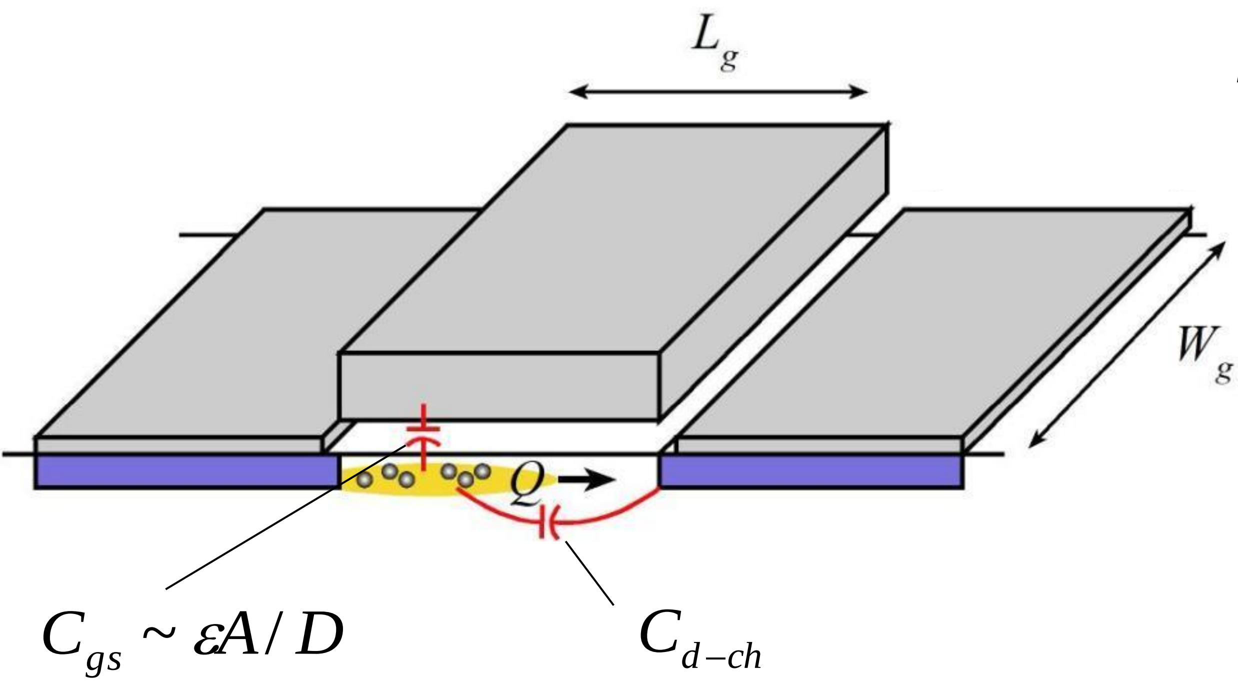


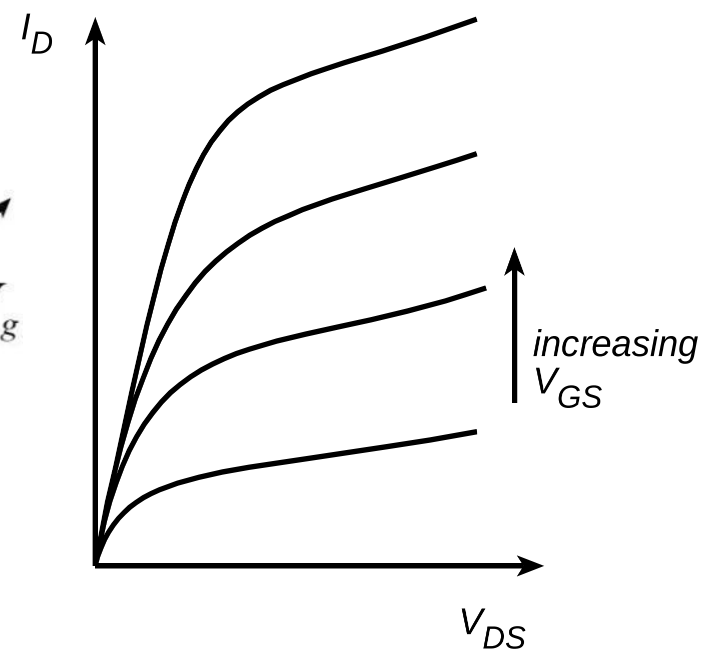
$$I_d = Q/\tau \quad \text{where} \quad \tau = L_g / v_{electron}$$

$$\delta Q = C_{gs}\delta V_{gs} + C_{d-ch}\delta V_{ds}$$

$$\delta I_d = g_m \cdot \delta V_{gs} + G_{ds} \cdot \delta V_{ds} \quad \text{where} \quad g_m = C_{gs}/\tau \text{ and } G_{gd} = C_{d-ch}/\tau$$

FET Characteristics

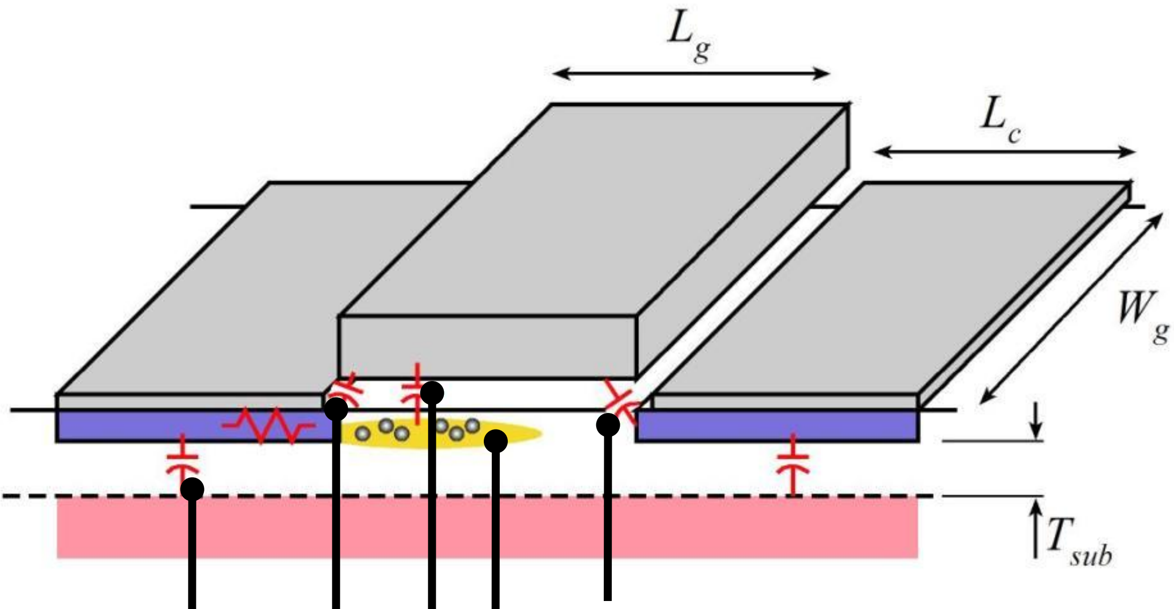




$$\delta I_d = g_m \cdot \delta V_{gs} + G_{ds} \cdot \delta V_{ds}$$

$$g_m = C_{gs} / \tau \quad G_{gd} = C_{d-ch} / \tau \quad \tau = L_g / v_{electron}$$

FET Parasitic Capacitances (Estimate)



$$C_{gd}/W_g \sim \varepsilon$$

$$g_m/W_g \sim v\varepsilon/T_{ox}$$

$$C_{gs}/W_g \sim \varepsilon \cdot L_g/T_{ox}$$

$$C_{gs,f}/W_g \sim \varepsilon$$

$$C_{sb}/W_g \sim \varepsilon \cdot L_c/T_{sub}$$