ECE ECE145B (undergrad) and ECE218B (graduate)

Final Exam. March 24, 2012

Do not open exam until instructed to.
Open notes, open books, etc
You have 3 hrs.

Use all reasonable approximations (5% accuracy is fine.) , ***AFTER STATING THEM.***
Hint: Stop and think before doing complicated calculations. ***For some problems, there is an easier way.***

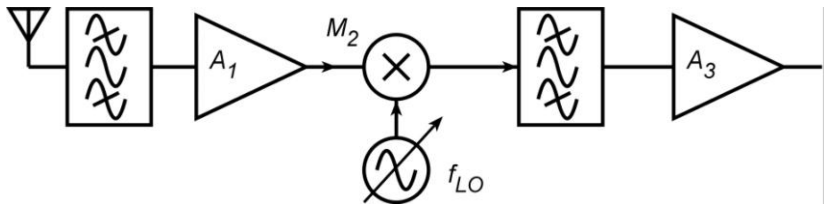
Problem	Points Received	Points Possible
1a		5
1b		5
1c		10
1d		5
2		30
3a		10
3b		10
4a		10
4b		10
4c		10

Name: __________________________

Problem 1, 20 points

receiver calculatoins.

Amplifier A_1 has gain G_1 =10 dB gain, noise figure F_1 =1.0 dB and input-referred third-order incercept $IIP3_1$ =0 dBm



Mixer M_2 has gain G_2 =0 dB gain, noise figure F_2 =3.0 dB.

Amplifier A_3 has gain G_3 =30 dB gain, noise figure F_3 =3.0 dB.

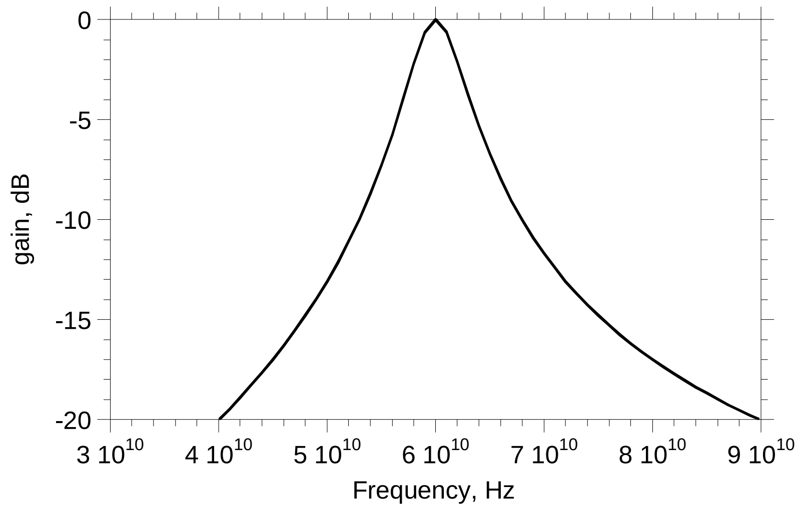
Neither M_2 nor A_3 produce and third-order distortion.

<u>part a, 5 points</u>

The receiver is operating with 1 Gb/s (10^9 bits/sec) digital radio on a 60 GHz carrier using *uncoded* QPSK modulation. Since we have not studied this, it is stated without proof that for a digital bit error rate of 10^{-9}, the signal (power)/noise(power) ratio in a 1 GHz bandwidth must be 36:1. Find the minimum received power.

part b, 5 points

The local oscillator is *above* the RF frequency. The IF is at 10 GHz. The attenuation-frequency characteristics of the RF pre-select filter are as shown to the right.

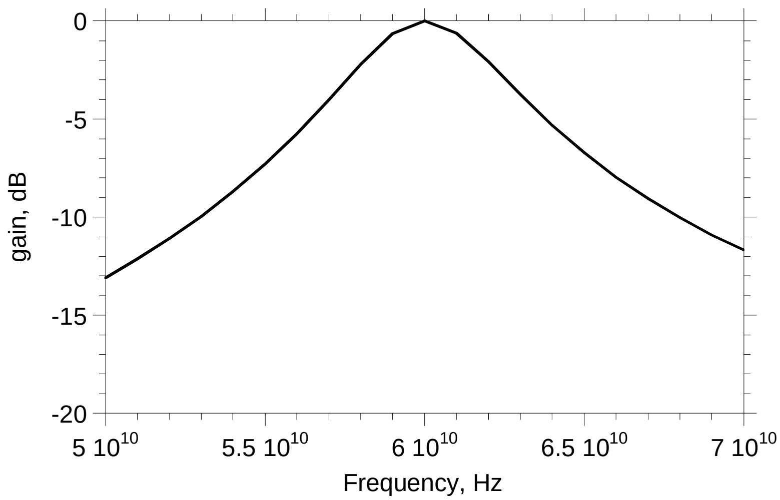


If the received signal power is -40 dBm, what interfering power at the receiver image frequency would result in a 20 dB signal/interference ratio ?

part c, 10 points

The transfer function of the RF pre-select filter is shown in more detail to the right.

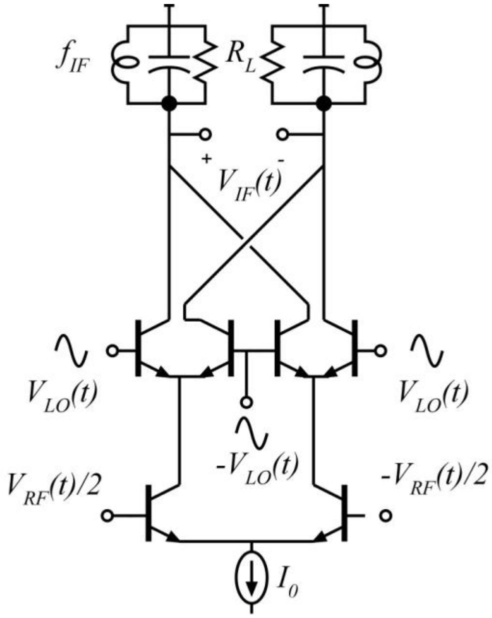
Interfering signals are present, both of power -30 dBm *at the antenna* terminals, at frequencies of 50 GHz and 55 GHz.



The IF filter is a brick-wall filter of 1 GHz bandwidth centered at 10 GHz, i.e. has 0 dB gain between 9.5 and 10.5 GHz, and infinite attenuation outside this bandwidth. If we require a 20 dB signal/ interference ratio, what must the 60 GHz RF signal power be ?

part d, 5 points

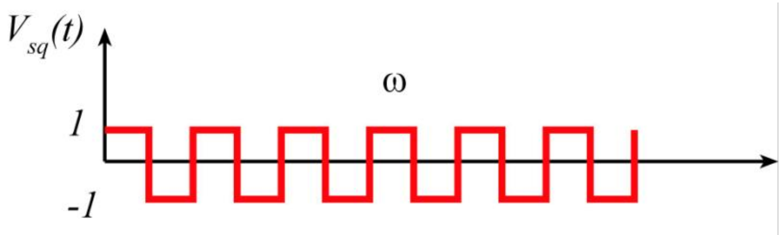
We instead use a fundamental mixer, as shown. The bipolar tranistors are ideal (zero parasitic resisitance, infinite current gain, no capacitances) , I_0 =2 mA, R_L =50 Ohms.



The LO is large and switches the upper transistor quad completely.

In units of voltage gain, not power gain, what is the conversion gain of the mixer ?

Hint: the Fourier series of a squarewave is given to the right.



$$V_{sq}(t) = \frac{4}{\pi}\left[\cos(\omega t) + \frac{\cos(3\omega t)}{3} + \frac{\cos(5\omega t)}{5} + ...\right]$$

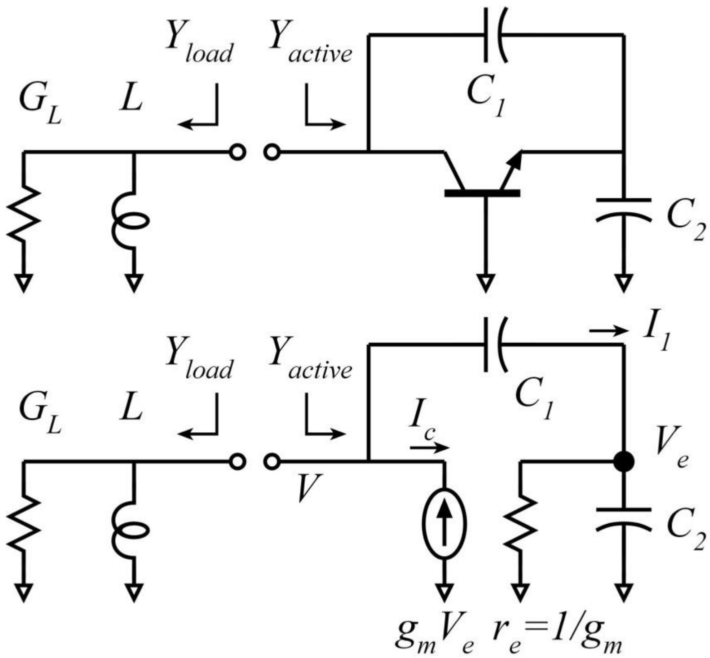
Problem 2, 30 points

The bipolar tranistor is ideal (zero parasitic resisitance, infinite current gain, no capacitances), and is biased at 1 mA emitter current.

You wish to design a 50 GHz oscillator (LO for problem 1).

Pick C_2 so that its capacitive reactance is 1/10 that of $1/g_m$.

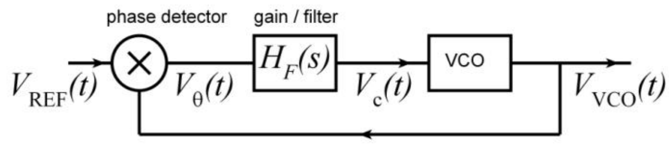
Pick C_1 so that the negative conductance presented to the resonator is maximized.



Find L, C_1, and C_2. Find the maximum tolerable value of load conductance.

Problem 3, 20 points

In the 50 GHz PLL at right, $V_\theta(t) = V_0 \sin(\Delta\theta)$ where V_0=1.0 V , $\Delta\theta$ is the phase difference between the reference and VCO singals. A_{mixer} =1.0 and $V_{RF}(t) = V_{RF}\cos(\omega_{RF}t + \theta_{RF})$.



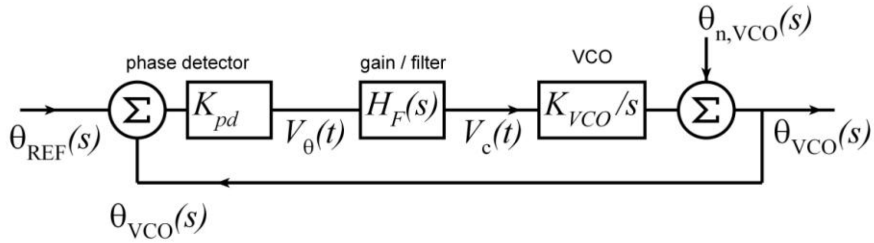
For zero control voltage, the VCO oscillates at 50 GHz, and it tunes at a rate of 1 GHz/Volt.

The loop filter has $H_F(s) = (1 + s\tau_z)/s\tau_i$.

part a, 10 points

The loop filter has $H_F(s) = (1 + s\tau_z)/s\tau_i$. We want a 1.0 MHz PLL loop bandwidth. The zero frequency $f_{zero} = 1/2\pi\tau_z$ is to be 1/5 of this. Find the integrator time constant τ_i and the zero freqeuency. Find the loop phase margin.

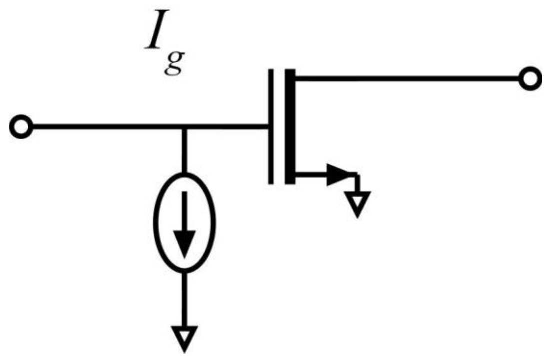
part b, 10 points



If the reference has phase noise of -120 dBc (1Hz) at 10 MHz offset from carrier, what would this contribute to the phase noise of the PLL output ? If the VCO has phase noise of -50 dBc (1Hz) at 100 Hz offset from carrier, what would this contribute to the phase noise of the PLL output ?

Problem 4, 30 points

The FET has g_m =100 mS and no other parastic elements----except a 100 nA gate leakage current I_g which has shot noise associated with it



<u>part a, 10 points</u>

Find the spectral densities of the short-circuit input noise voltage and the open-circuit input noise current.

part b, 10 points

Find the optimum generator impedance and the minimum noise figure.

part c, 10 points

Given the optimum generator impedance, find the generator available signal power that would give you 0 dB signal/noise ratio in a 1 Hz bandwidth.

Please compare this to $kT\cdot(1\,\text{Hz})$.

1 Hz receiver bandwidth is roughly equivalent to making a 1-second measurement. The answer may be quite suprising.