ECE 145B/218B, Lab Project 3: Transistor Oscillator

January 10, 2024

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Precautions

Precautions to avoid instrument damage

(a) Observe static precautions when working with the network analyzer or spectrum analyzer. Wear the wrist strap.

(b) Never connect a network analyzer or spectrum analyzer directly to a circuit carrying dc. Make sure your circuit is dc blocked, or you will destroy the instruments..

Safety precautions

(a) Safety note: please be very careful with the X-acto razor-blade knives. Use the same level of care you would use with a very sharp kitchen knife ! We want no injuries.

(b) Common solder is tin-lead and is toxic. If ingested, lead accumulates in your body and slowly and progressively causes brain damage as well as damage to other organs. The shop sells non-lead-containing solder. ***Do not bring lead-containing solder into the lab.*** That means, do not purchase solder at Radio-shack or other vendors unless you very carefully check its metal composition. The new non-lead solders have a higher melting point, which makes soldering harder, particularly soldering to ground planes. Use a higher-power (hotter !) iron for soldering to the ground plane.

(c) In case some student fails to follow the solder rules above, ***do not eat or bring food into the lab, wash your hands immediately after leaving the lab***, and sweep up and dispose of any solder debris. ***Do not use solder-suckers for desoldering, as these spray a fine powder of solder all over the room***. Horribly toxic if some fool uses them with lead solder ! Use desoldering wick (braid) instead; it is better anyway.

(d) Basic rules for electrical safety apply. Circuit voltages are low (~5-15 Volts) but avoid bringing in high-voltage DC supplies, use common caution in plugging in 120 V connections, do not stand in or work around water, and do not work with electrical equipment with bare feet.

(e) students who violate these precautions will receive a lab grade of zero.

Background and Suggested Approach.

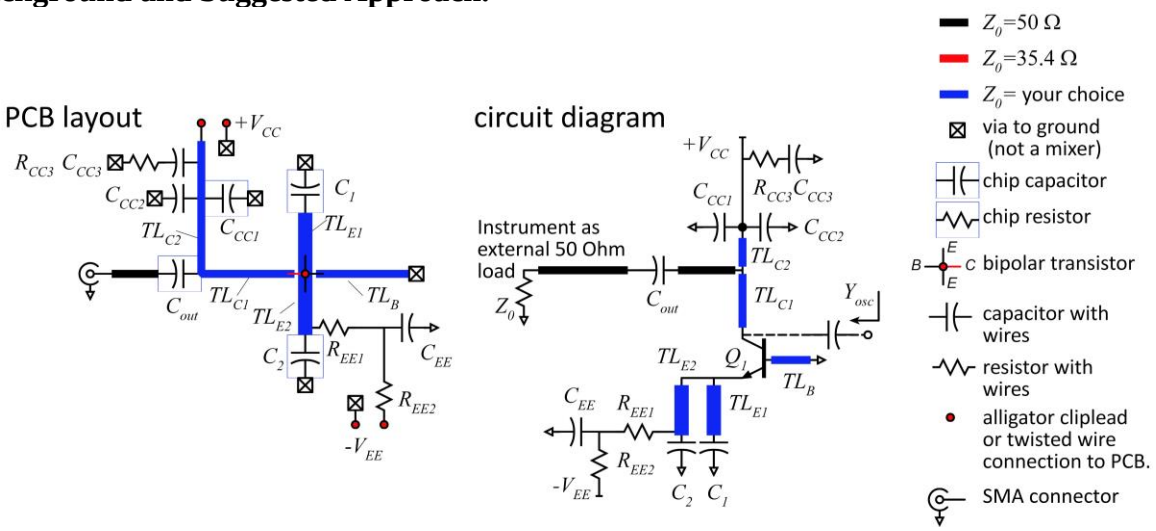

Figure 1: Schematic and PCB layout of the suggested lab project design. The point Y_{osc} is a simulation test point, not a physical connection point.

Your assignment is to build a transistor oscillator. Please use the MRF901 transistor and its model, noting again that the model we have is for a surface-mount package, but we will be using transistors in the micro-cross package, so there will be some small modeling error. I suspect that this error will be smaller than that associated with tolerances associated with construction by hand. Figure 1 shows both a suggested circuit diagram and a suggested physical layout. You are of course free to use whatever circuit diagram you would like. Further, you may design for any oscillation frequency you could like. Lower frequencies will likely give more accurate modeling, but it will be more difficult to fit the circuit on the PCB. 2 GHz might be a good design choice.

It would be wise to select a combination of DC collector current and DC collector-emitter voltage that is consistent with that use to specify ft or noise figure on the data sheet.

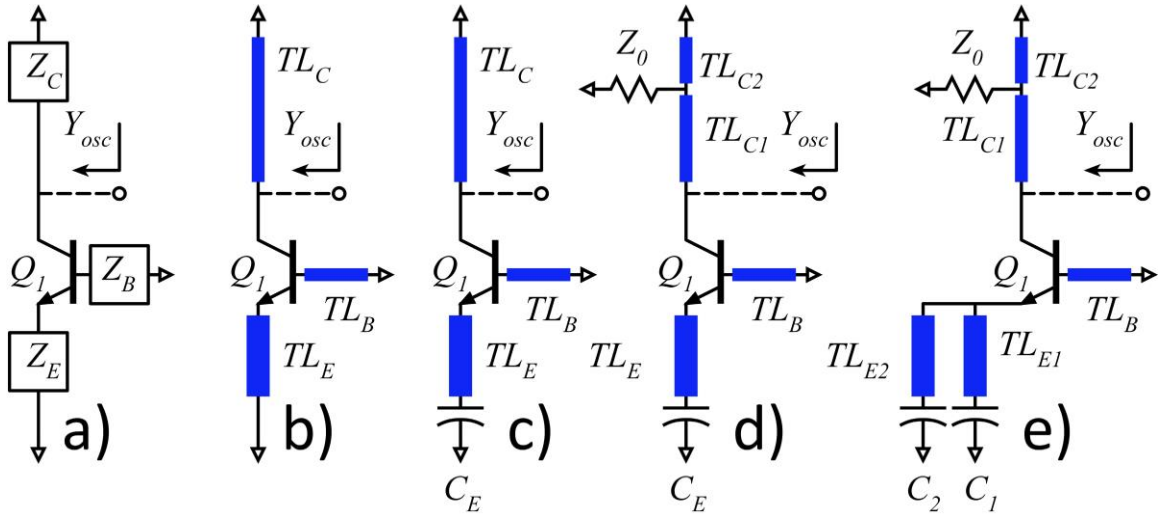

Figure 2: Oscillator design progression. The steps are described in the subsequent text.

Figure 2 shows the oscillator design progression. The basic series-tuned oscillator (a) presents impedances Z_C, Z_B, and Z_E to the transistor. These impedances can be synthesized (b) using three series lines TL_C, TL_B, and TL_E. However, once the emitter AC bypass capacitor C_E is added (c) , the desired impedance Z_E presented to the emitter can be obtained either with a very large C_E (presenting a short circuit) plus the appropriate length of TL_E, or with a smaller C_E. In either case, TL_E, C_E, and TL_B are tuned for maximum negative $G_{osc} = \mathrm{Re}\{Y_{osc}\}$ and TL_C is subsequently tuned for $jB_{osc} = \mathrm{Im}\{Y_{osc}\} = \mathrm{Re}\{Y_{osc}\}$ = zero Ohms. One then adds the output connection (d), with, to a first approximation, the length of TL_{C1} plus the length of TL_{C2} being the length TL_C; the smaller the ratio of the lengths of TL_{C2} to TL_{C1} to the lower the output power but the less output will load the oscillator, and the less sensitive the oscillation frequency to the load impedance. Given that the transistor package has two emitter leads, the emitter should be connected symmetrically (e), with TL_{E1}, TL_{E2}, C_1, and C_2 presenting impedance Z_E to the emitter.

For low phase noise, B_{osc} should show a very rapid variation with frequency near the desired frequency of oscillation, i.e. B_{osc} should be zero at $f_{oscillation}$ and $d(B_{osc})/df$ should be as large as possible at $f_{oscillation}$.

The full circuit (Figure 1) adds DC bias connections and supply bypass networks to the oscillator. On the emitter, splitting Ree into two equal parts (Ree1 and Ree2) will provide an effective RC bypass network for Vee, making the oscillator insensitive to the emitter supply impedance. On the collector, the chip capacitor Ccc1 is the functional RF bypass capacitor. The larger leaded capacitor Ccc2 provides bypassing at lower frequencies. The capacitor C_{CC3}=C_{CC2} , together with the series damping resistor $R_{cc3} \approx$ 1-5 Ω, ensures that the supply impedance never exceeds a few ohms even at the frequency at which the external supply lead inductance resonates with C_{cc2}. A DC blocking capacitor is necessary at the output port; another one is needed at the test port at which you simulate Y_{osc}.

Your simulation should sweep from DC to f_{max}, I suspect about 10 GHz for the MRF901, making sure that G_{osc} is negative only at and near the desired oscillation frequency. It is possible that the emitter bypass capacitors may cause the transistor to also show negative resistance at lower frequencies; this might cause oscillation at these undesired lower frequencies. Appropriate adjustment of Ree1 and Ree2 (while keeping the desired collector bias current) might well suppress this.

After simulating Y_{osc} vs. frequency using a small-signal swept-frequency 2-port S-parameter simulation (with port 1 being the point at which Y_{osc} connects and port 2 being the oscillator output connection), then remove the port 1 connection and perform a large-signal transient simulation of the oscillation start-up.

Second possible circuit configuration

The interaction of $TL_{E1,2}$ and $C_{1,2}$ in Figure 1 and Figure 2 might result in a strong negative resistance peak in the MHz range, resulting in an undesired low-frequency oscillation. This can be avoided in the alternate circuit configuration of Figure 3 and Figure 4. In this configuration, the resistor R_{ee1} introduces undesired parallel loading at the end of T_{LE2}, and should therefore be as large as possible. Consequently with $R_{EE1} + R_{EE2} = (V_{ee} - \phi) / I_C$, one should pick $R_{EE2} << R_{EE1}$, perhaps setting R_{EE2} to 50-100 Ohms.

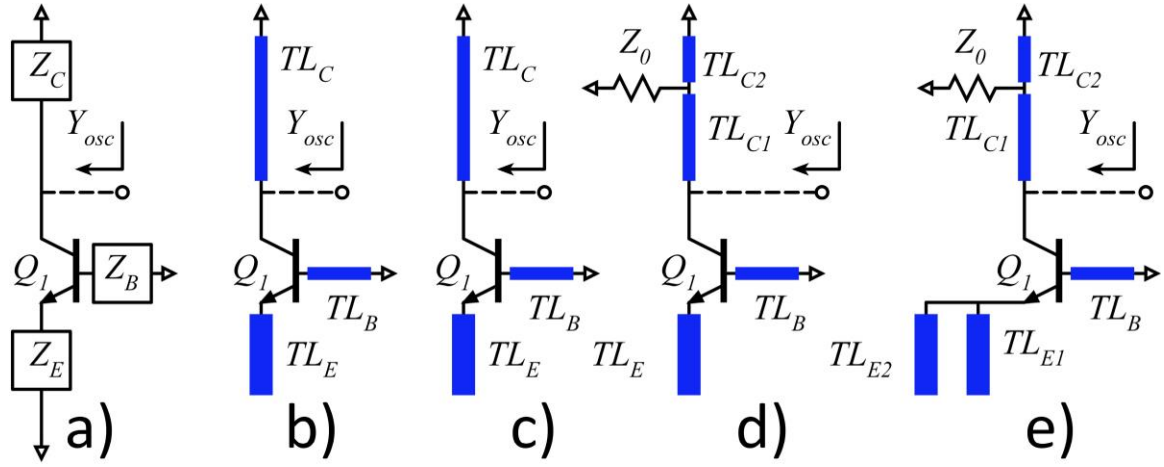

Figure 3: Alternate oscillator configuration avoiding the emitter bypass capacitance.

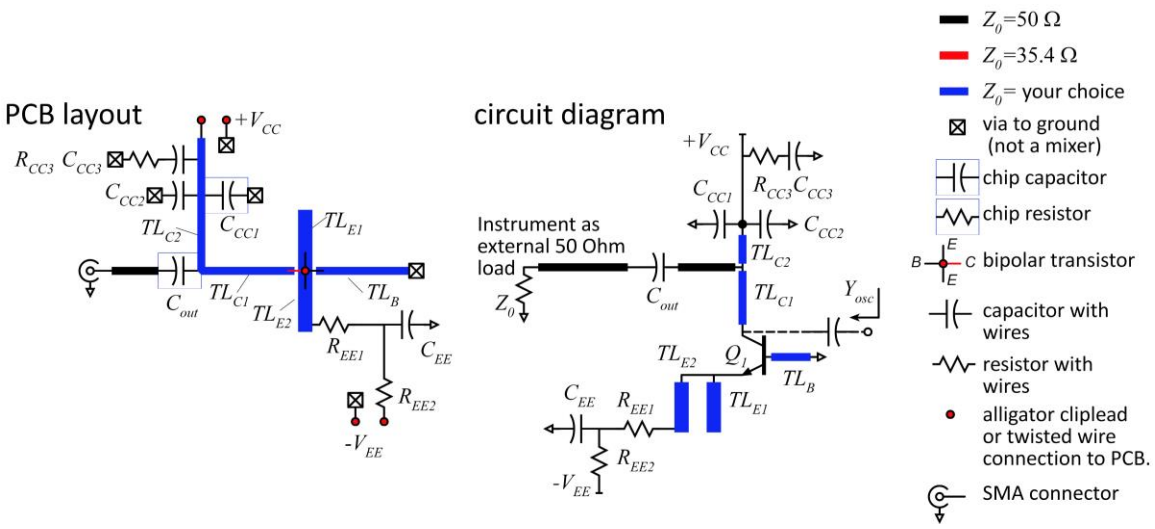

Figure 4: Alternate oscillator configuration avoiding the emitter bypass capacitance.

Hints on simulation

Figure 5 shows suggested simulation methods. First considering 2-port simulations, given that $I_1 = Y_{11}V_1 + Y_{12}V_2$, we have $Y_{11} = (I_1 / V_1)\big|_{V_2=0}$. So, temporarily placing the load resistance Zo, as shown, *internal to the port 2 node*, will result in the simulated Y_{11} being the admittance looking into port 1 (i.e. $Y_{osc} = G_{osc} + jB_{OSC}$) with port 2 connected to ground, i.e. with the junction of TL_{C2} and TL_{C1} being loaded, as desired, in Z_o. To then simulate the oscillator start-up transient and large-signal operation (output amplitude), you can move the load Z_o back outside the port 2 terminal. Make sure that the load is present in your schematic, as a transient simulation , unlike a 2-port S parameter simulation, does not provide one implicitly. A startup current $I_{start}(t) = I_o U(t)$, with I_0 being a few microamps, is applied to speed up the oscillator startup transient.

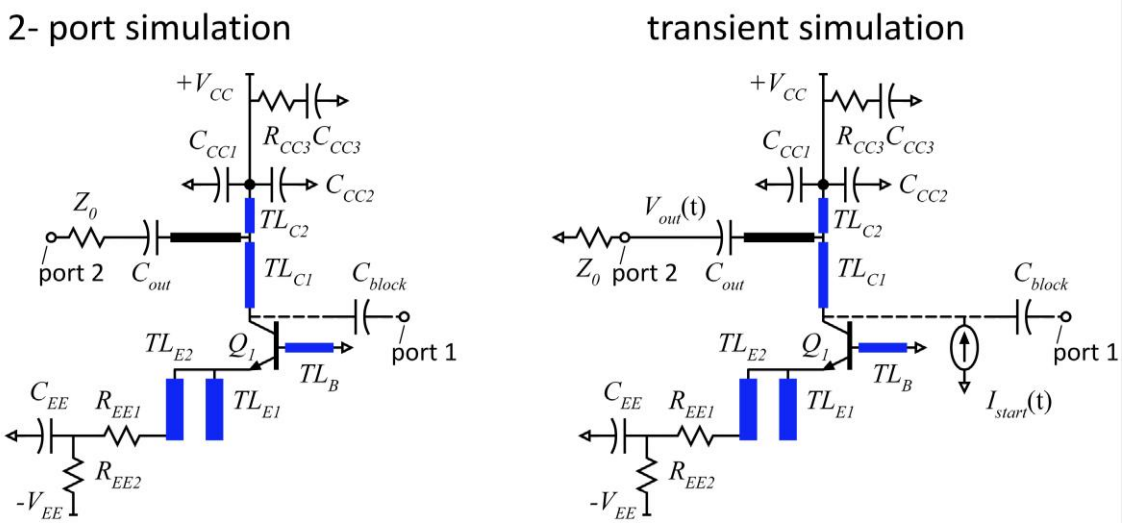

Figure 5: Suggestions for negative resistance and transient simulations.

The Assignment

Give the very short time available, and the complexity of the project, we will try to keep this project as simple as possible. ECE145B students will only do a simulation; ECE218B students will build the oscillator.

The initial steps are for both 145B and 218B students:

1) Create the circuit in ADS, simulate as a 2-port S-parameter analysis with port 2 being the oscillator output port and port 1 being the point labelled Y_{osc} in the above figures. Tune the circuit to maximize the negative conductance and to maximize $d(B_{osc})/df$ at the oscillation frequency. Note the effect of adjusting the output port coupling (TL_{C2} to TL_{C1} length ratio) on the port negative conductance.

2) Simulate the circuit with a transient analysis, giving it a very small step-function current input at the node Y_{osc} (as is shown in the notes) and observe the RF output voltage waveform, noting its amplitude and frequency.

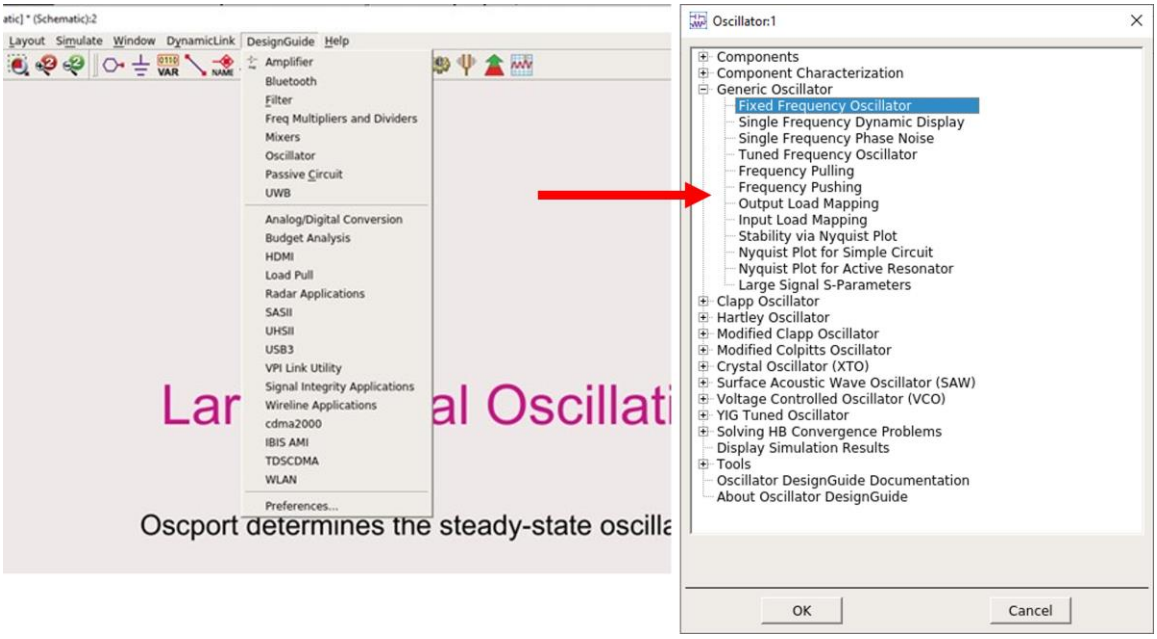

Figure 6: Accessing the oscillator design guide library in ADS

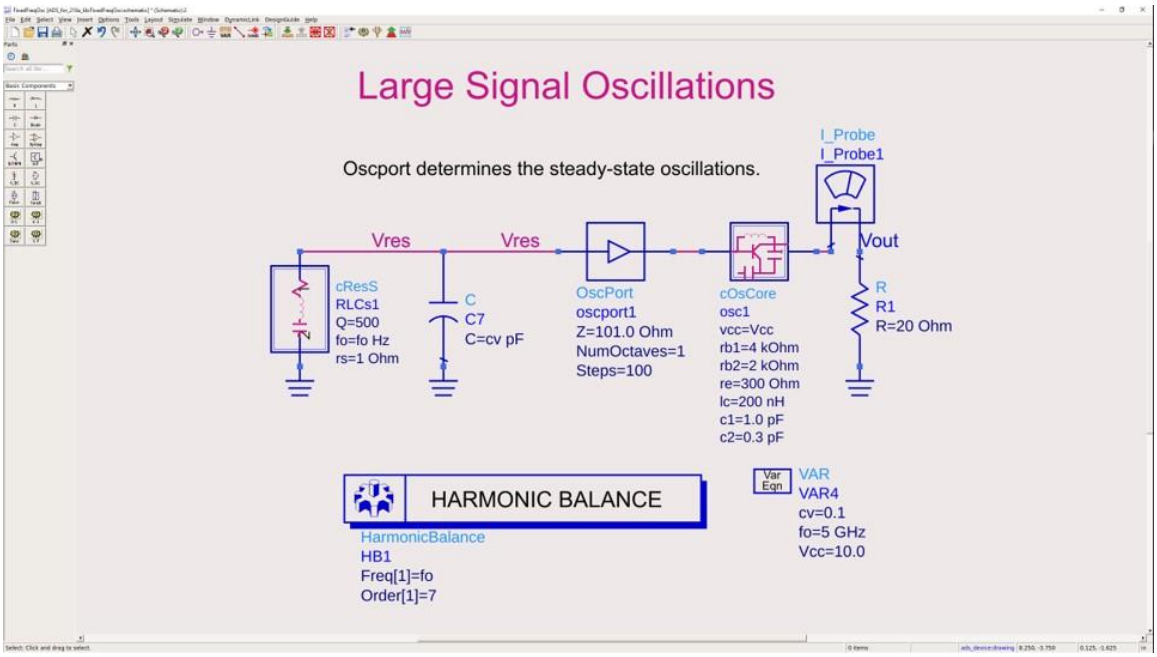

Figure 7: ADS "fixed frequency oscillator" test bench.

3) Optional: Using the ADC oscillator design guide (Figure 6, Figure 7), simulate the oscillator using the "fixed frequency oscillator" test bench. This test bench separates the main LC resonator (CResS and C7 in the ADS schematic; TL_{C2} and TL_{C1} in your circuit), the output load (R1 in the ADS schematic; Z_0 in your circuit), and the remainder of the circuit. It will take a little thought on how to map your design into this ADS file.

ECE145B: Write a report on the above simulations.

ECE218B: Construct the circuit on a Duriod board, with a launcher block and SMA connector for the output connection. Measure the output power, and phase noise using the spectrum analyzer. **BE SURE TO PLACE a 20 dB attenuator between the oscillator and the spectrum analyzer to avoid damaging the instrument with excess signal power**. Remove this attenuator only if the power level is sufficiently small for this to not damage the instrument. Measure the change in oscillation frequency for a +/- 5% change in the Vcc and -Vee power supplies. Grasp the power supply leads with your hand and observe the magnitude of the resulting frequency shift.