ECE 2C, notes set 4: Transistor Amplifiers ...basic considerations

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Goals of this note set:

Learn loadline analysis of transistor * circuits

Learn DC bias analysis of transistor * circuits

Learn AC small-signal analysis of transistor * circuits

* or any nonlinear circuit element
(diode, Vacuum tube, tunnel junction, ...)

Transistor Amplifiers: Comments

Expertise in multistage design requires much background

137AB: transistor circuits in great detail: 20 Weeks

Basic stages. device models DC vs small signal analysis.

Biasing techniques. AC vs. direct DC coupling.

Frequency response.

The best way to teach this involves long build-up of these concepts.

With this toolset mastered, real (complex multistage) ICs can be learned in a few weeks.

*** we cannot take this approach given the few weeks available in ECE2C.

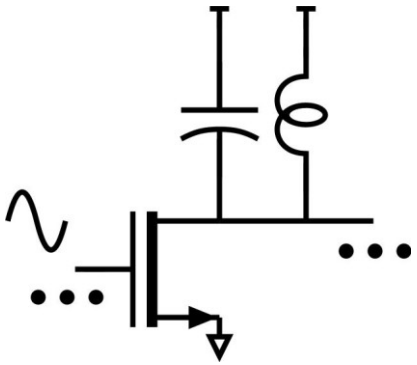
In ECE 2C: introduction to basic principles of active circuit design.

DC bias analysis. Loadlines. Small signal models. Small signal analysis.

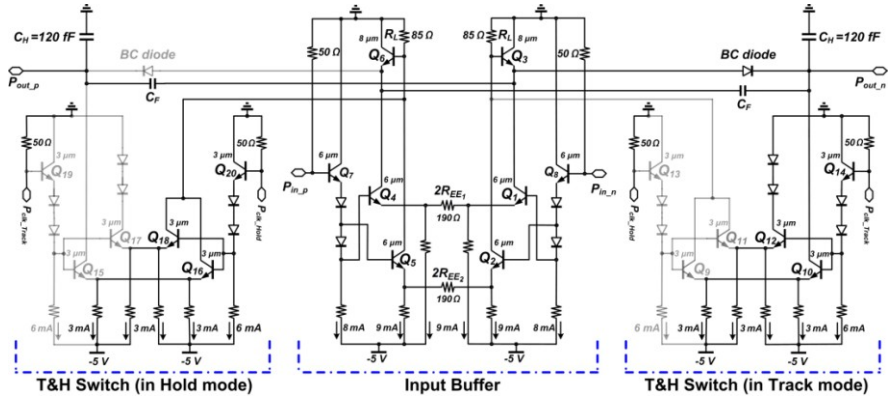
Transistor high-frequency models.

Fundmentals of frequency and transient response.

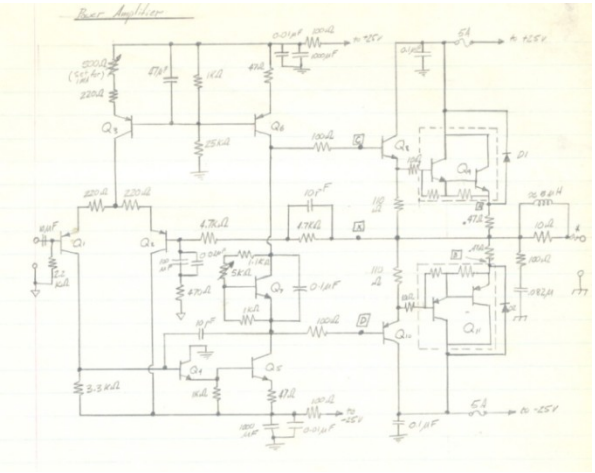
Transistor Amplifier Examples



Tuned amplifier
in radio receiver

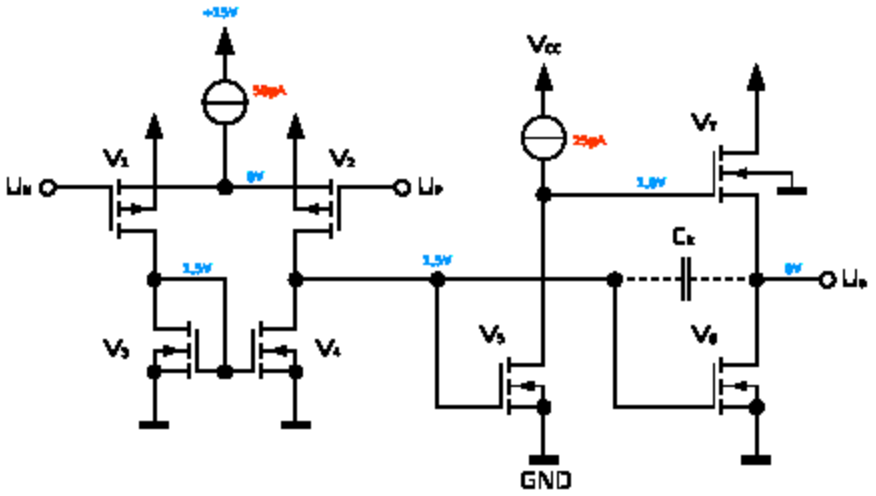


Track - hold circuit (part of analog - digital converter)



(Archaic 1980s) Audio Power Amp

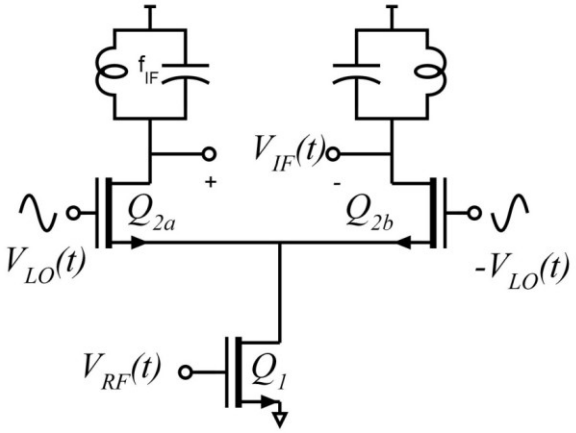
Simply, an op - amp with very high maximum output current



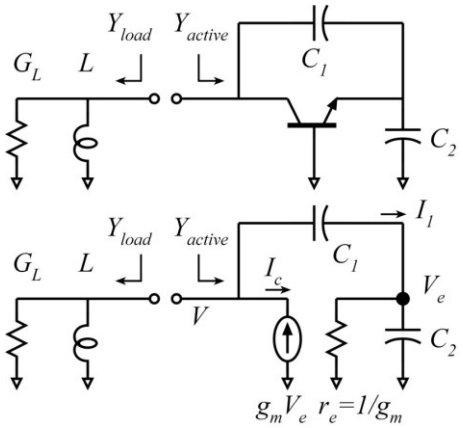
CMOSOP - AMP

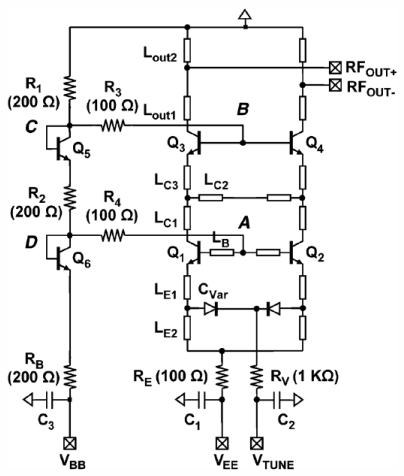
https://commons.wikimedia.org/wiki/File:Single_Supply_CMOS_OpAmp.svg

Transistor Circuit Examples

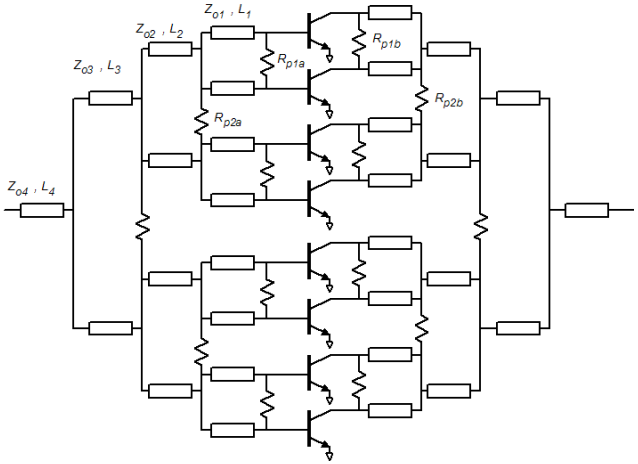


FET mixer
(frequency conversion in radios)

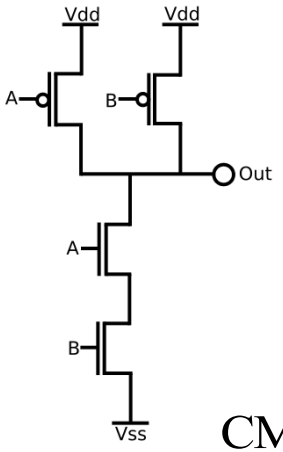




Transistor oscillator
(signal generation)



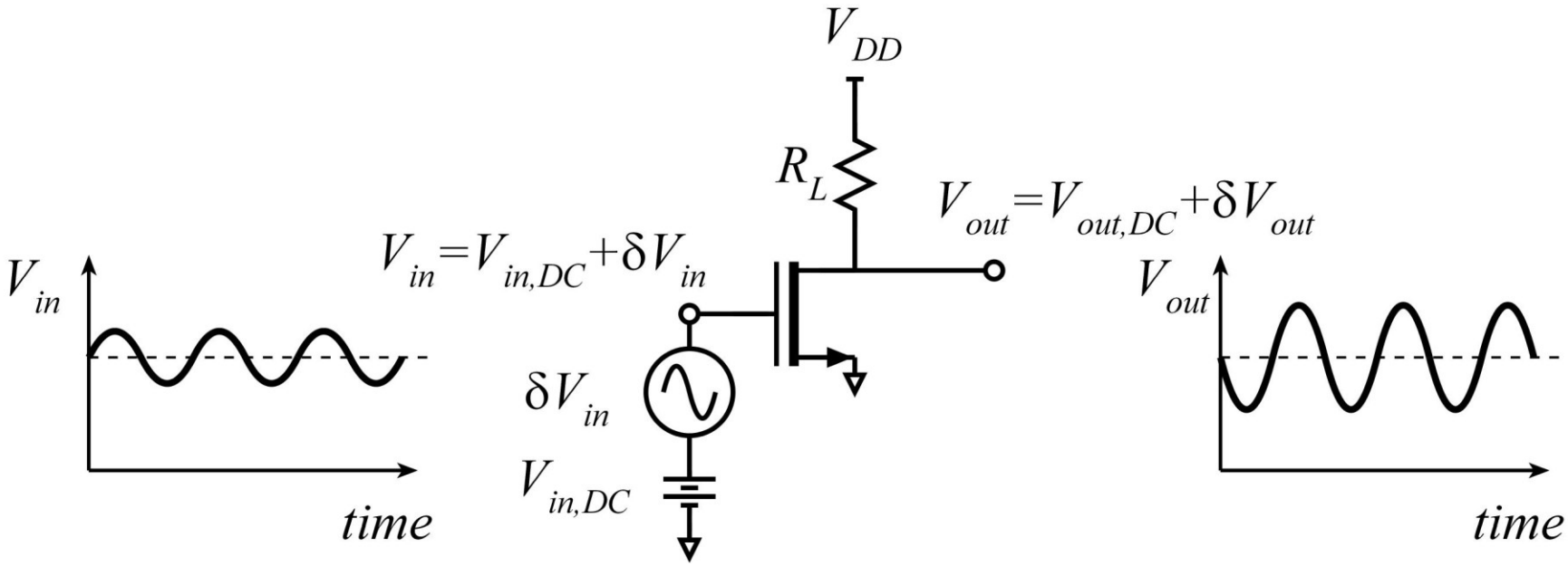
Radar transmitter power amplifier



CMOS logic gate

http://en.wikipedia.org/wiki/File:CMOS_NAND.svg

Elementary Common-Source Amplifier



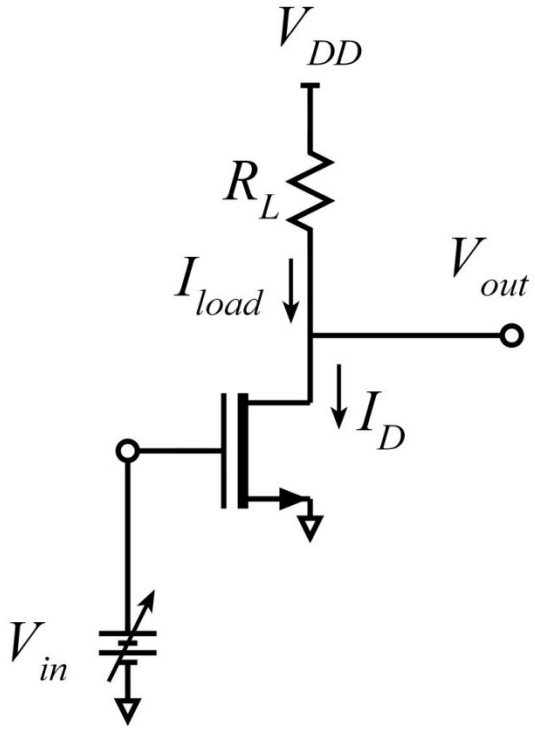
The amplifier is a transistor, a load, a power supply, and a DC bias network

An input signal is applied.

An amplified signal appears on the output.

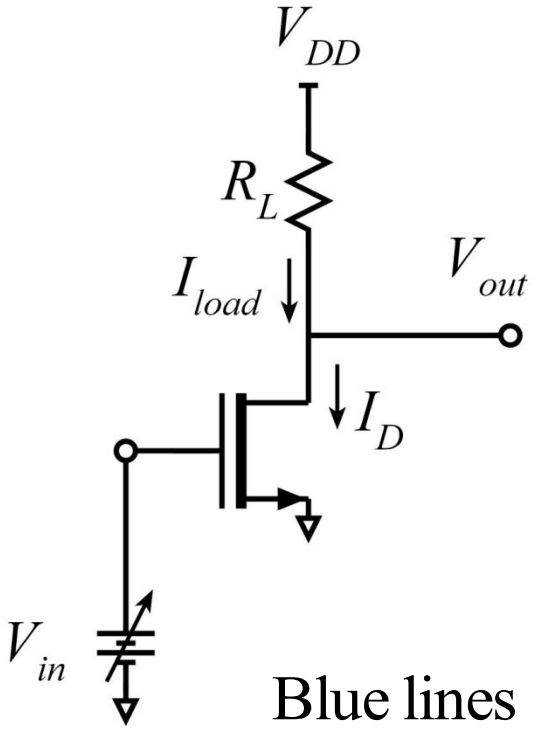
First: step-by-step analysis

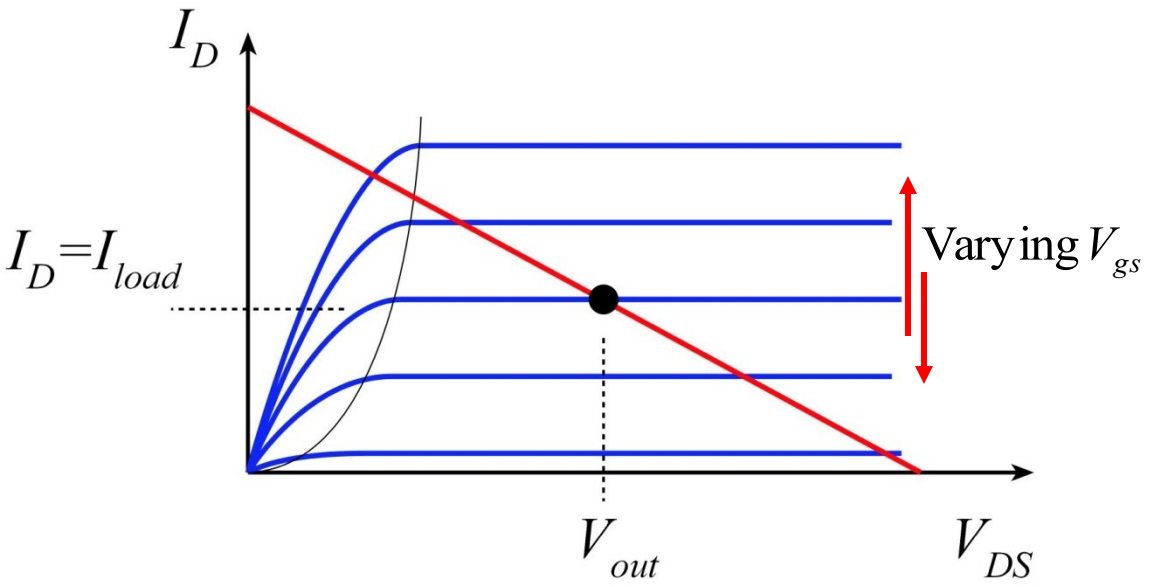
CS Amplifier: DC Transfer Characteristics



Let us compute V_{out} as a function of V_{in}

CS Amplifier: DC Transfer Characteristics





Blue lines : FET I - V characteristics

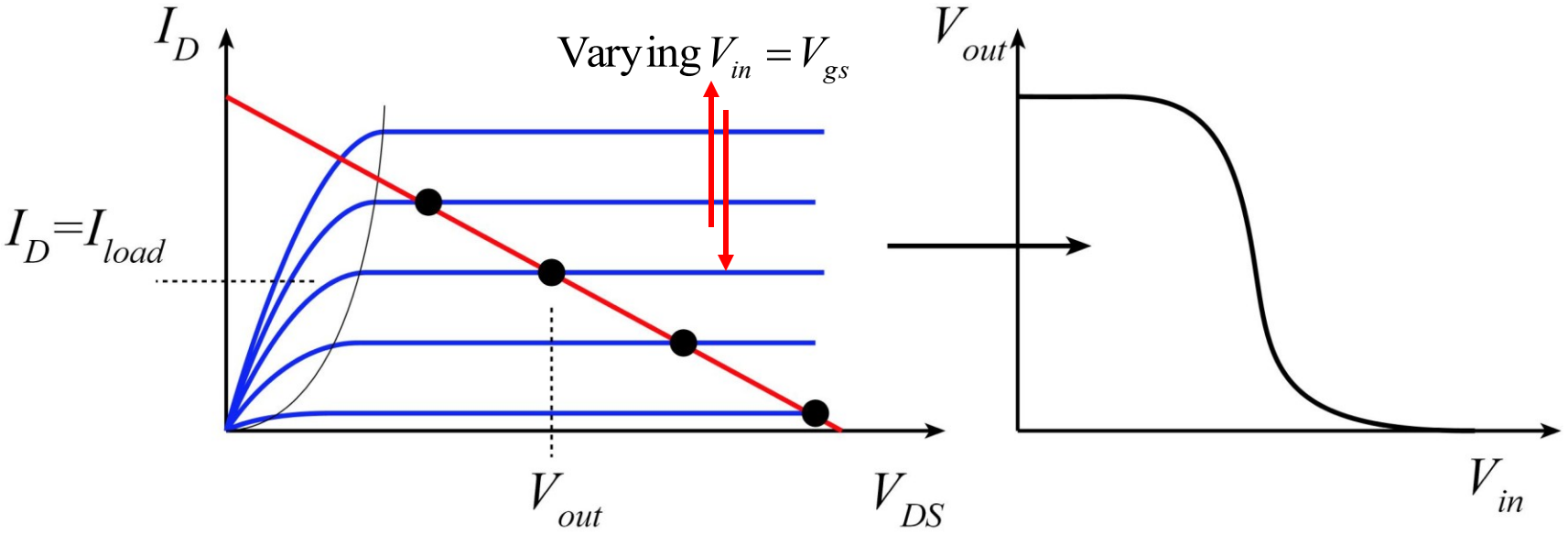
$$I_{D,\mu} = (\mu c_{ox} W_g / 2L_g)(V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$$

(old - fashioned mobility model suitable for long - channel FET)

Red line : the loadline

$$I_{load} = (V_{DD} - V_{out}) / R_L \quad \text{from Ohm's law.}$$

CS Amplifier: DC Transfer Characteristics

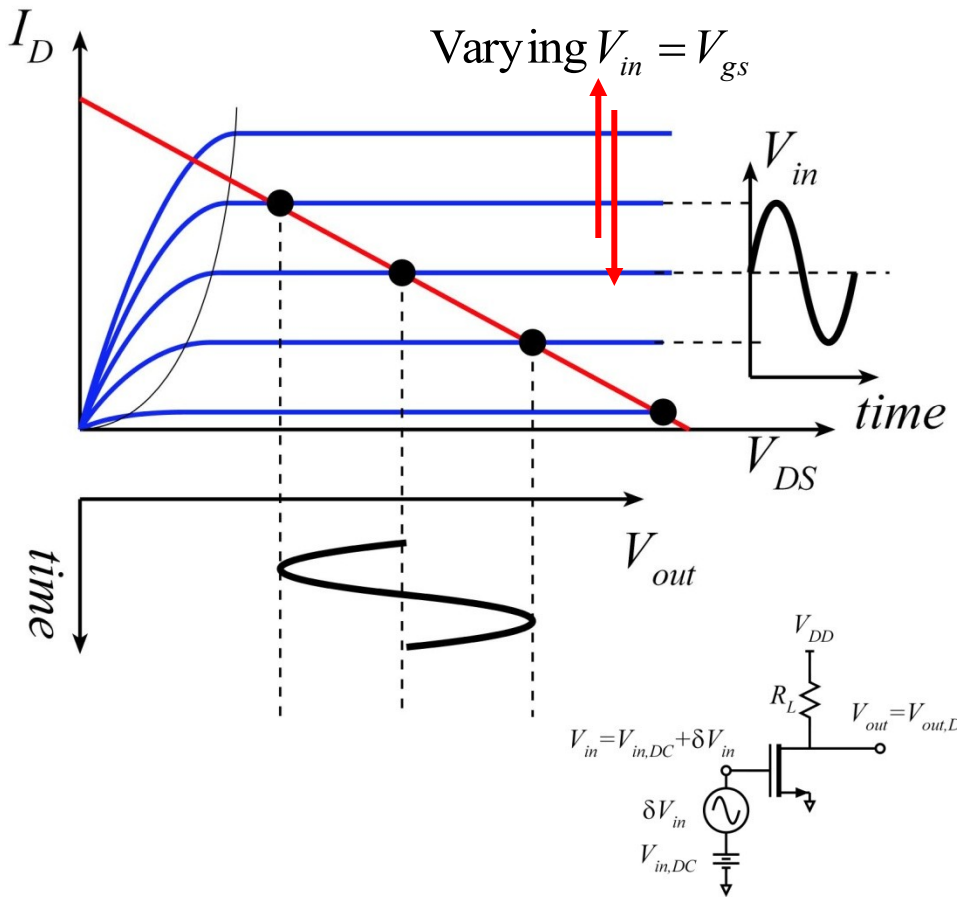


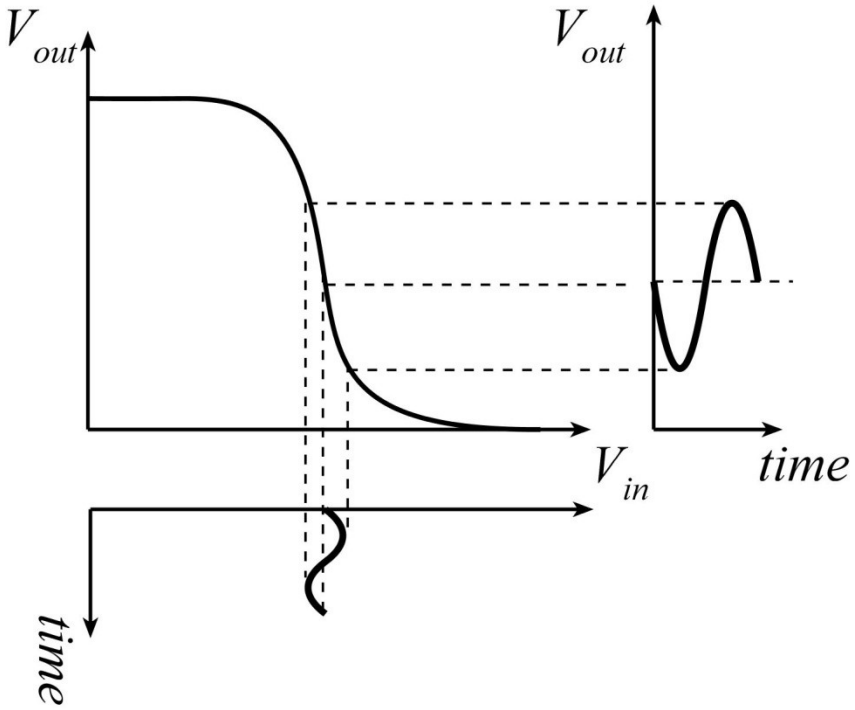
At any V_{in}, the output voltage V_{out} is found by setting $V_{in} = V_{gs}$ and finding the intersection of the FET characteristics and the loadline.

Allows us to plot the V_{in} vs. V_{out} transfer characteristics.

Conceptually clear and easy. But hard work mechanically.

CS Amplifier: S.S. Voltage Gain by Loadline Method



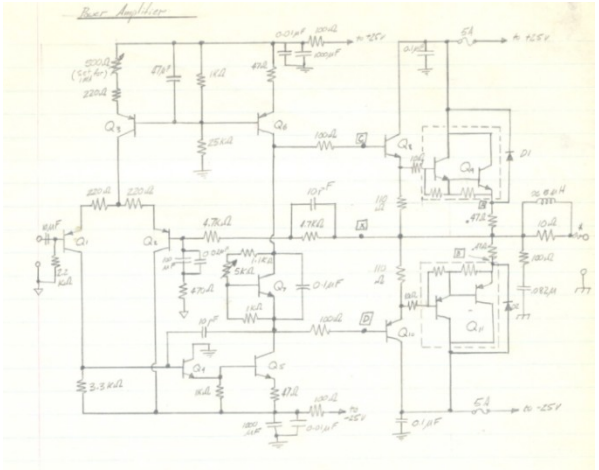


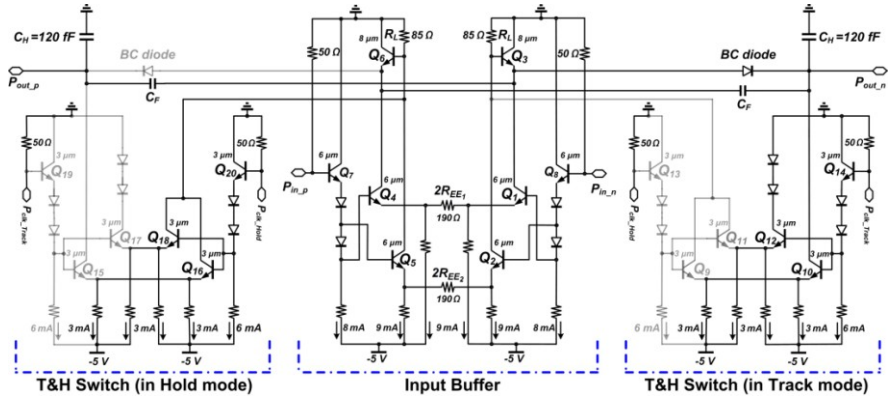
Here: using graphical method to find ΔV_{out} from ΔV_{in}.

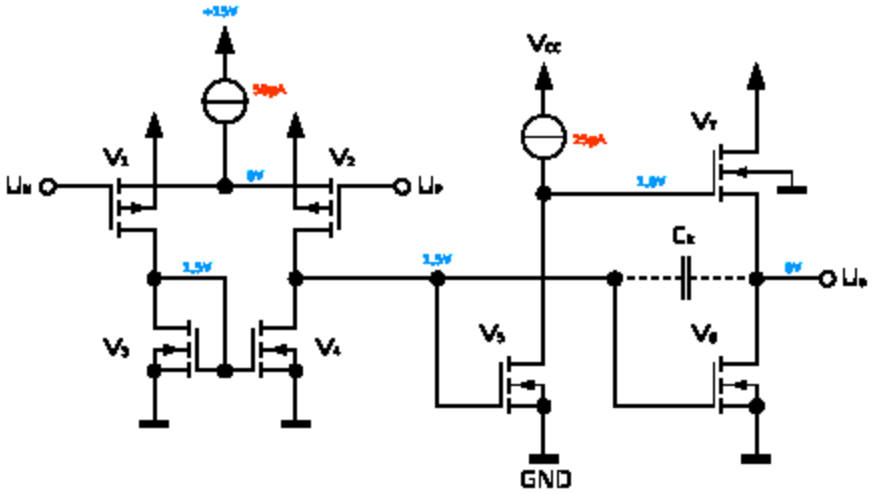
Two methods shown (left, right).

Conceptually clear and easy. But hard work mechanically.

Loadline methods: Intuitive but Inefficient.



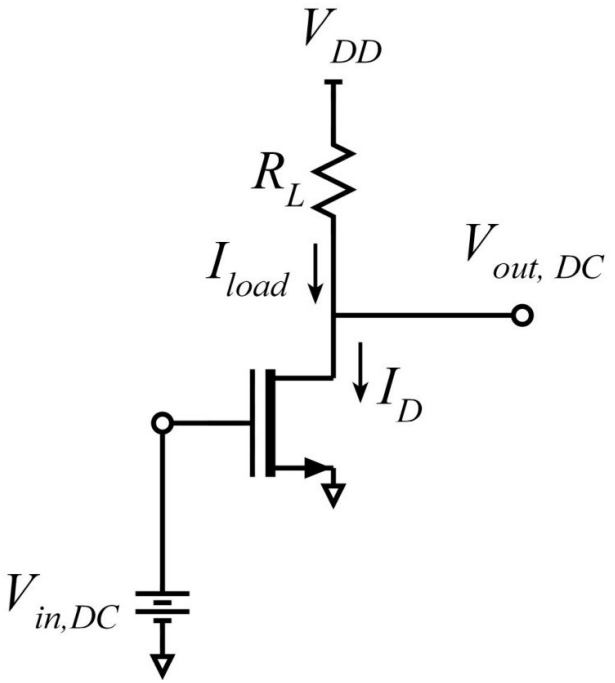




https://commons.wikimedia.org/wiki/File:Single_Supply_CMOS_OpAmp.svg

Real ICs are far too complex to analyze by loadline methods

Method #2a: Finding the DC Bias Conditions



* we are ignoring the $(1+\lambda V_{DS})$ term in the bias analysis.
Doing this causes some small error.

If we do not, the DC analysis involves solving quadratic formulas. Hard.

In ECE137A we will learn some tricks to calculate this quickly yet fairly accurately.

Do not ignore the $(1+\lambda V_{DS})$ term in the small signal analysis.

Example Parameters:

FET:

$(\mu c_{ox} W_g / 2L_g) = 1\text{mA/V}^2$

$V_{th} = 0.3\text{ V}$

$1/\lambda = 10\text{V}$

Circuit

$V_{dd} = 2.5\text{ V}$

$R_L = 1.1\,\text{k}\Omega$

$V_{in,DC} = 0.7\text{ V}$

Analysis:

$$I_D = (\mu c_{ox} W_g / 2L_g)(V_{gs} - V_{th})^2(1+\lambda V_{DS})$$

$$= (1\,\text{mA/V}^2)(0.7V - 0.3V)^2(\cancel{1+\lambda V_{DS}}) = 0.16\,\text{mA}$$

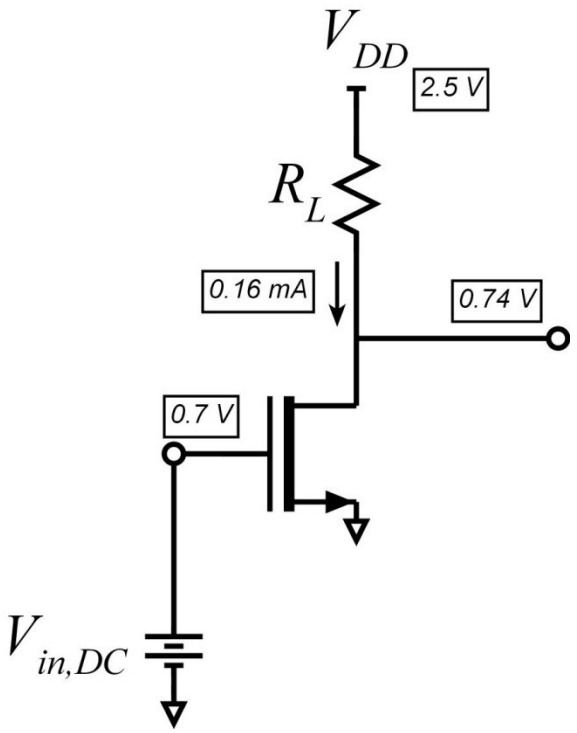
ignore *

$$V_{out,DC} = V_{DD} - I_D R_L$$

$$= 2.5\text{V} - (0.16\text{mA})(1.1\text{kOhm})$$

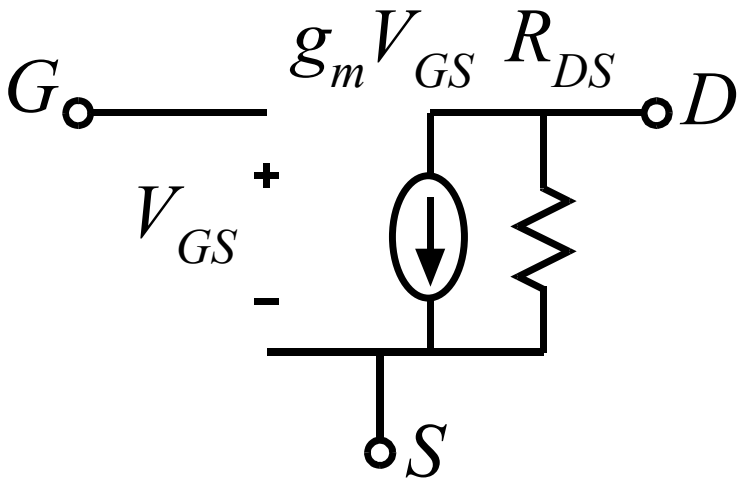
$$= 0.74\text{ V.}$$

Method #2a: DC Bias Solution



Method #2b: Find the FET Small-Signal Parameters

Recall :



Drain current

$$I_D = (\mu c_{ox} W_g / 2L_g)(V_{gs} - V_{th})^2 (1 + \lambda V_{DS})$$

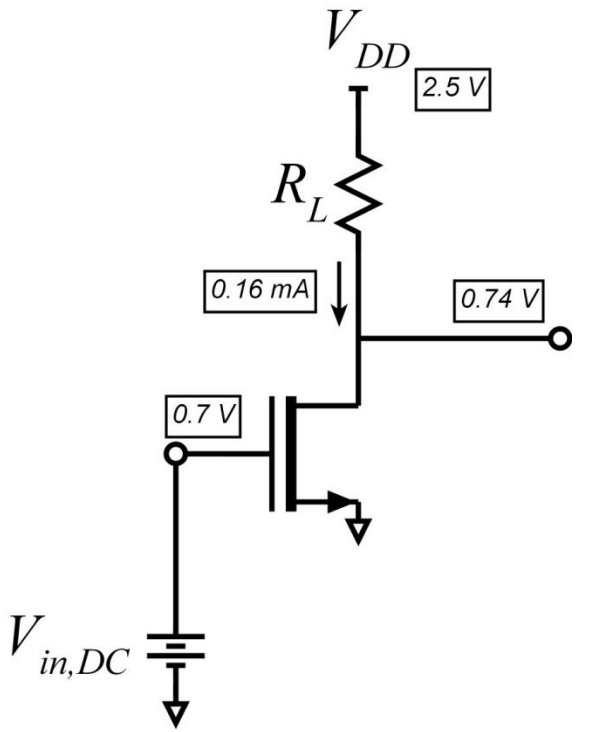
Transconductance

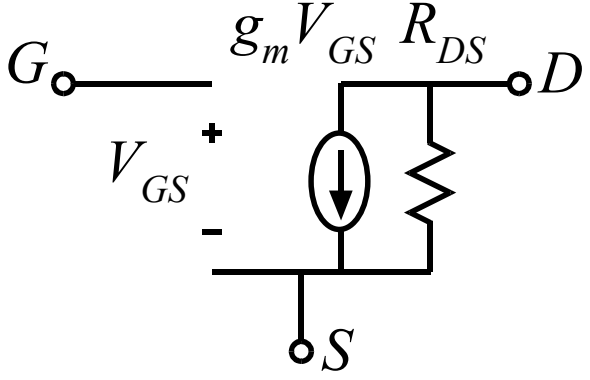
$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} = (\mu c_{ox} W_g / L_g)(V_{gs} - V_{th})(1 + \lambda V_{DS})$$

OutputConductance

$$G_{ds} = \frac{1}{R_{ds}} \equiv \frac{\partial I_D}{\partial V_{DS}} = \frac{\lambda I_D}{1 + \lambda V_{DS}} \cong \lambda I_D$$

Method #2b: Find the FET Small-Signal Parameters





Example Parameters:

FET:

$(\mu c_{ox} W_g / 2L_g) = 1\text{mA/V}^2$

$V_{th} = 0.3\text{ V}$

$1/\lambda = 10\text{V}$

Bias conditions

$V_{gs} = 0.7\text{ V}$

$V_{DS} = 0.7\text{ V}$

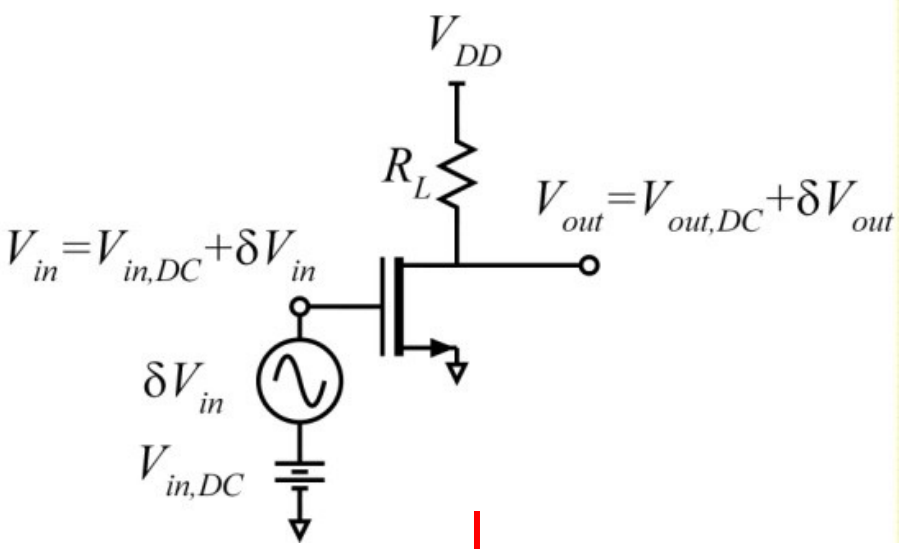
$I_D = 0.16\text{ mA}$

Analysis:

$$g_m = (\mu c_{ox} W_g / L_g)(V_{gs} - V_{th})(1 + \lambda V_{DS})$$
$$= (2\text{mA/V}^2)(0.7\text{V} - 0.3\text{V})(1 + 0.74\text{V}/10\text{V})$$
$$= 0.856\text{ mS}$$

$$G_{ds} = \frac{1}{R_{ds}} \cong \lambda I_D = \frac{0.16\text{mA}}{10\text{V}} = 16\ \mu\text{S} = \frac{1}{62.5\text{k}\Omega}$$

Method #2c: Find the Small-Signal Equivalent Circuit

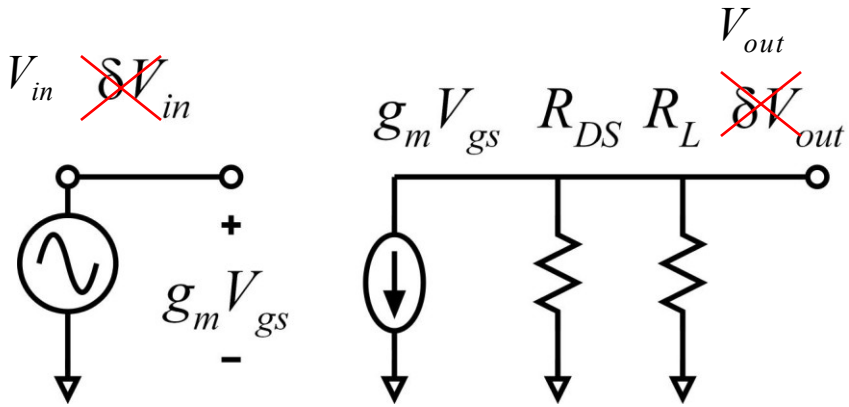


In this circuit

1) Replace the transistor with its small-signal model

2) Replaced constant (bias & supply) voltages with short-circuits

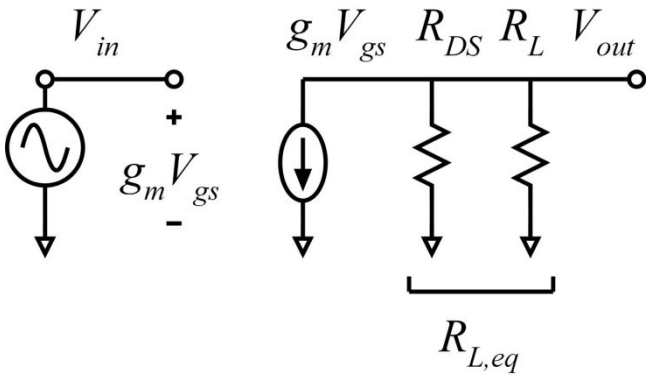
Because $\delta V = 0$ for a constant voltage.



This is the small-signal equivalent circuit.

The "δV" notation has been dropped: it is taken as implicit that these are small signals.

Method #2c: Find the small-signal gain



Example Parameters:

FET:

$g_m = 0.856\,\text{mS}$

$R_{DS} = 62.5\,\text{k}\Omega$

Circuit

$R_L = 11\,\text{k}\Omega$

Analysis:

equivalent load resistance

$$R_{L,eq} = R_L \parallel R_{DS} = 62.5\text{k}\Omega \parallel 11\text{k}\Omega$$
$$= 9.35\,\text{k}\Omega$$

From Ohm's law:

$$V_{out} = -g_m R_{Leq} V_{in} = -(0.856\text{mS})(9.35\,\text{k}\Omega)V_{in}$$

$$\frac{V_{out}}{V_{in}} = -g_m R_{Leq} = -8.0$$

The circuit has a voltage gain of -8.0

Comments

Loadlines are a good teaching tool...

...but are rarely used outside sophomore circuits.

(except : power amplifiers, logic gate transfer characteristics)

Active circuit analysis :

1) Find DC bias conditions (by math)

2) find transistor small signal models

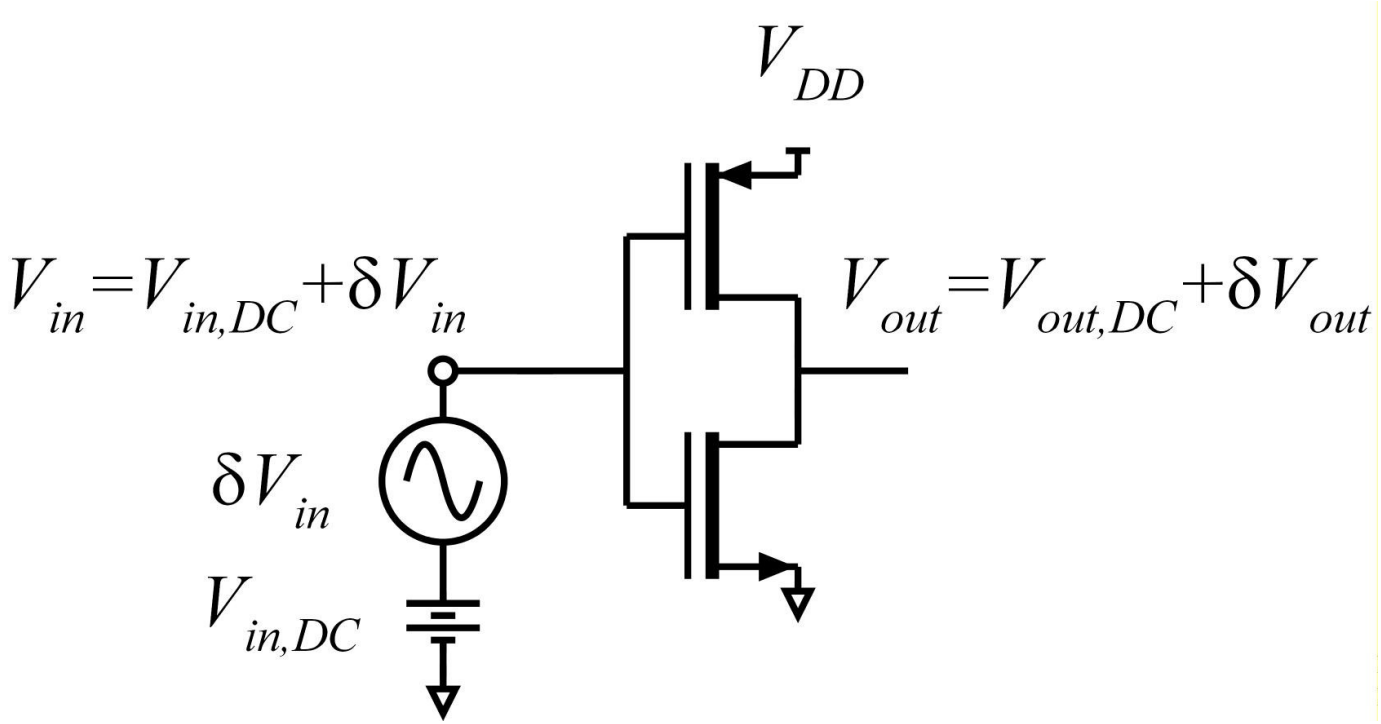
3) draw active circuit small signal equivalent circuit

4) analyze (to find voltage gain, other parameters of interest).

5) use other techinque to find maximum signal voltage, etc.

In ECE2C, we will focus on 1 - 4.

Example: Complementary MOS (CMOS) Amplifier



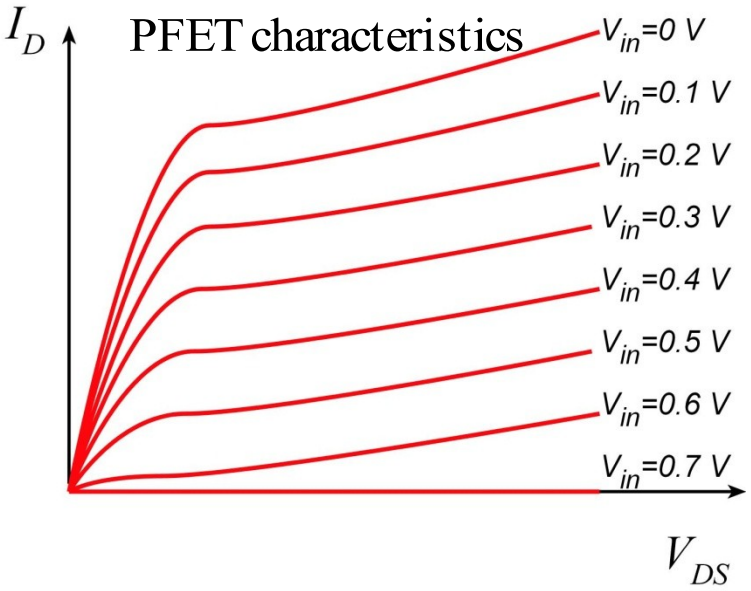
FET I-V characteristics*: $I_D = (1\,\text{mA/V}^2)(V_{gs} - 0.3\text{V})^2(1 + V_{DS}/10\text{V})$

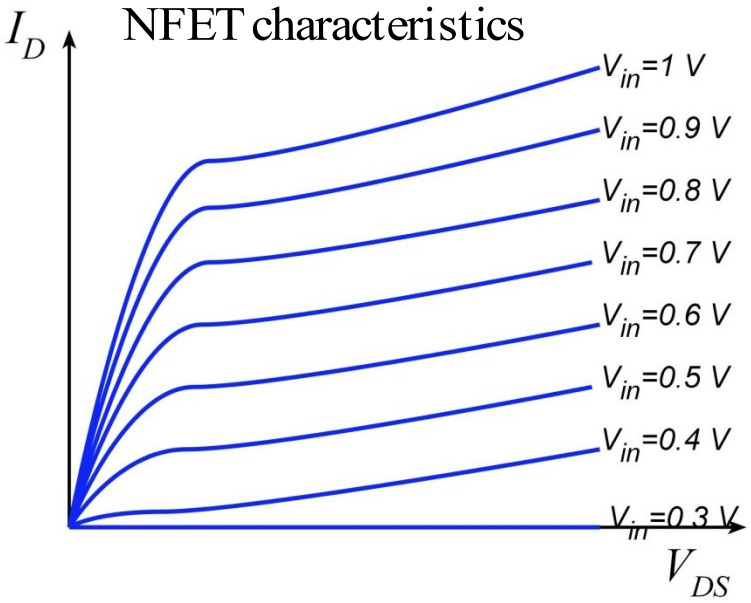
Supply: $V_{DD} = 1.0\,\text{V}$

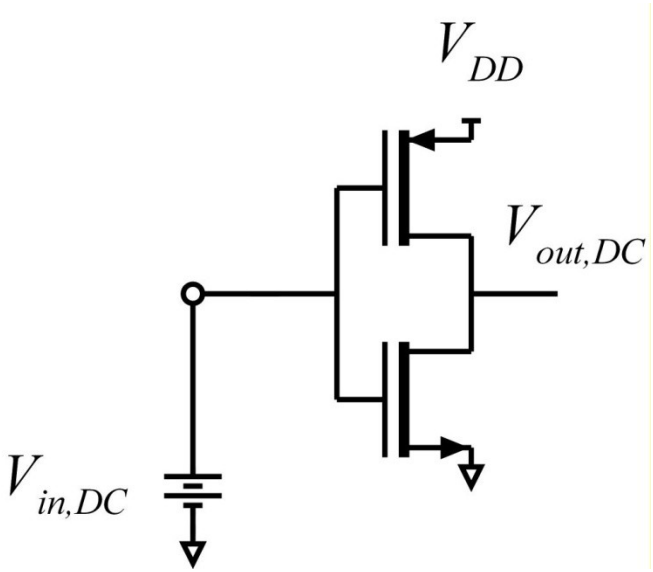
Bias: $V_{in,DC} = 0.5\,\text{V}.$

*For both FETs, ignoring sign changes needed for the P-FE

CMOS Amplifier: Graphical DC Bias Analysis







$$I_{D,NFET} = I_{D,PFET}$$

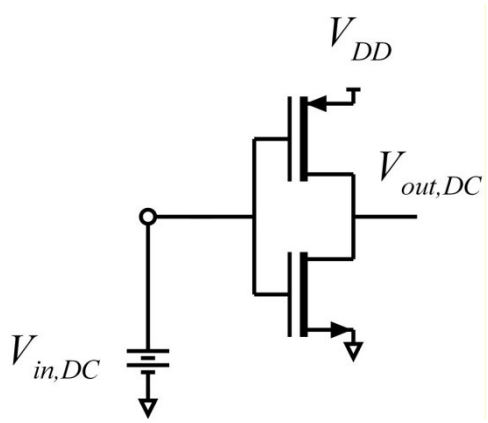
$$V_{gs,NFET} = V_{in,DC} \qquad V_{DS,NFET} = V_{out,DC}$$

$$V_{gs,PFET} = V_{DD} - V_{in,DC} \qquad V_{ds,PFET} = V_{DD} - V_{out,DC}$$

Next : represent these relationships on a single graph

CMOS Amplifier: Graphical DC Bias Analysis

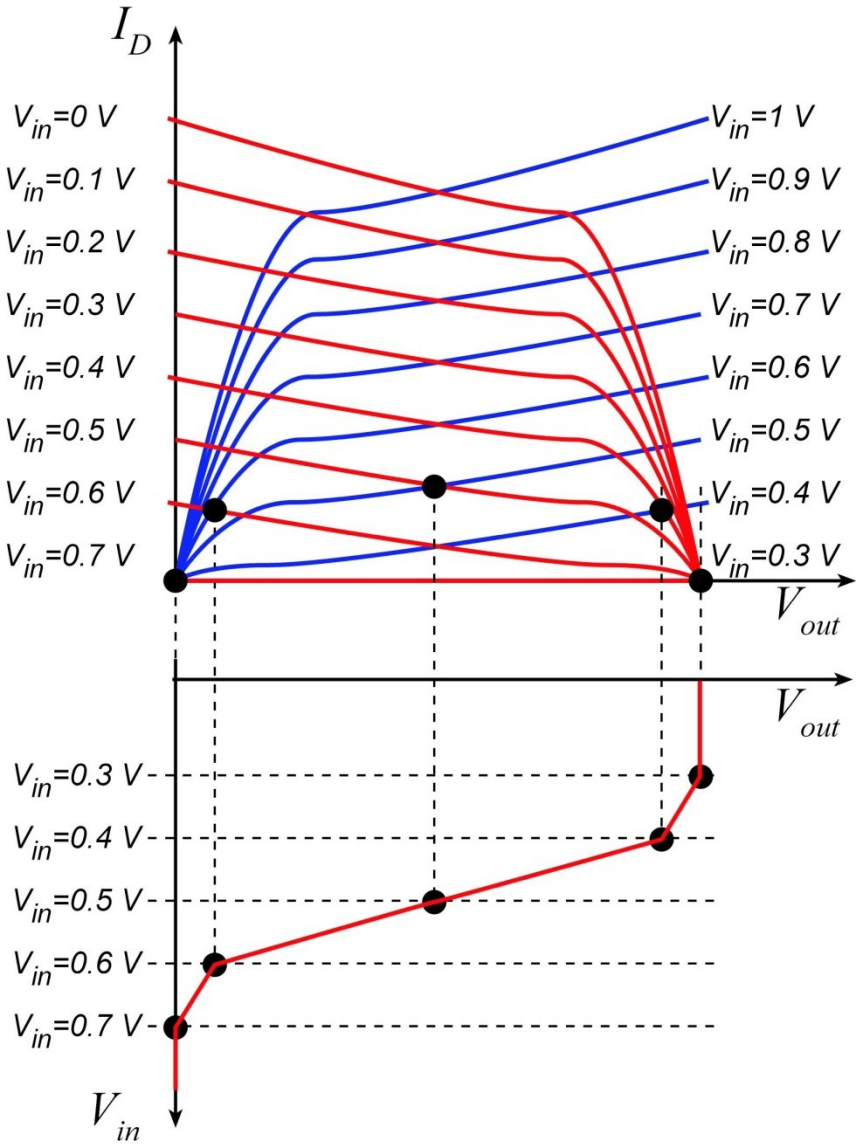
Represent these relationships on a single graph



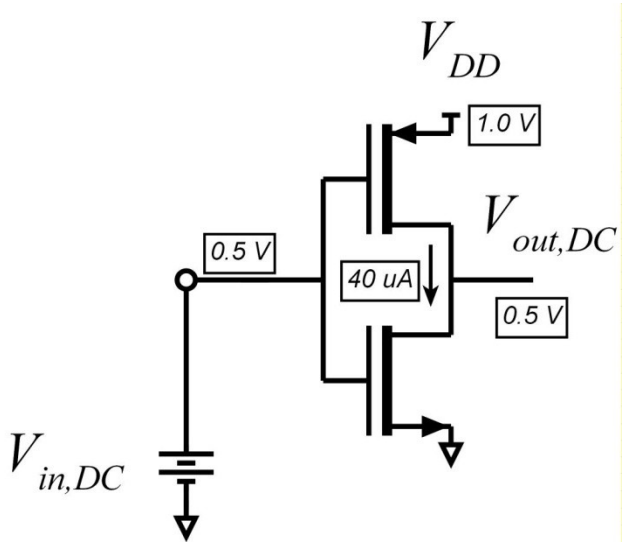
...and we can make from this a plot of V_{in} versus V_{out}.

Once again, the procedure is clear, but it is hard work.

Note: we have found that $V_{out} = 0.5$ Volts when $V_{in} = 0.5$ Volts.



CMOS Amplifier: FET Small-Signal Parameters



Example Parameters:

FET:

$(\mu c_{ox} W_g / 2L_g) = 1\text{mA/V}^2$

$V_{th} = 0.3\text{ V}$

$1/\lambda = 10\text{V}$

Bias conditions

$V_{gs} = 0.5\text{ V}$

$V_{DS} = 0.5\text{ V}$

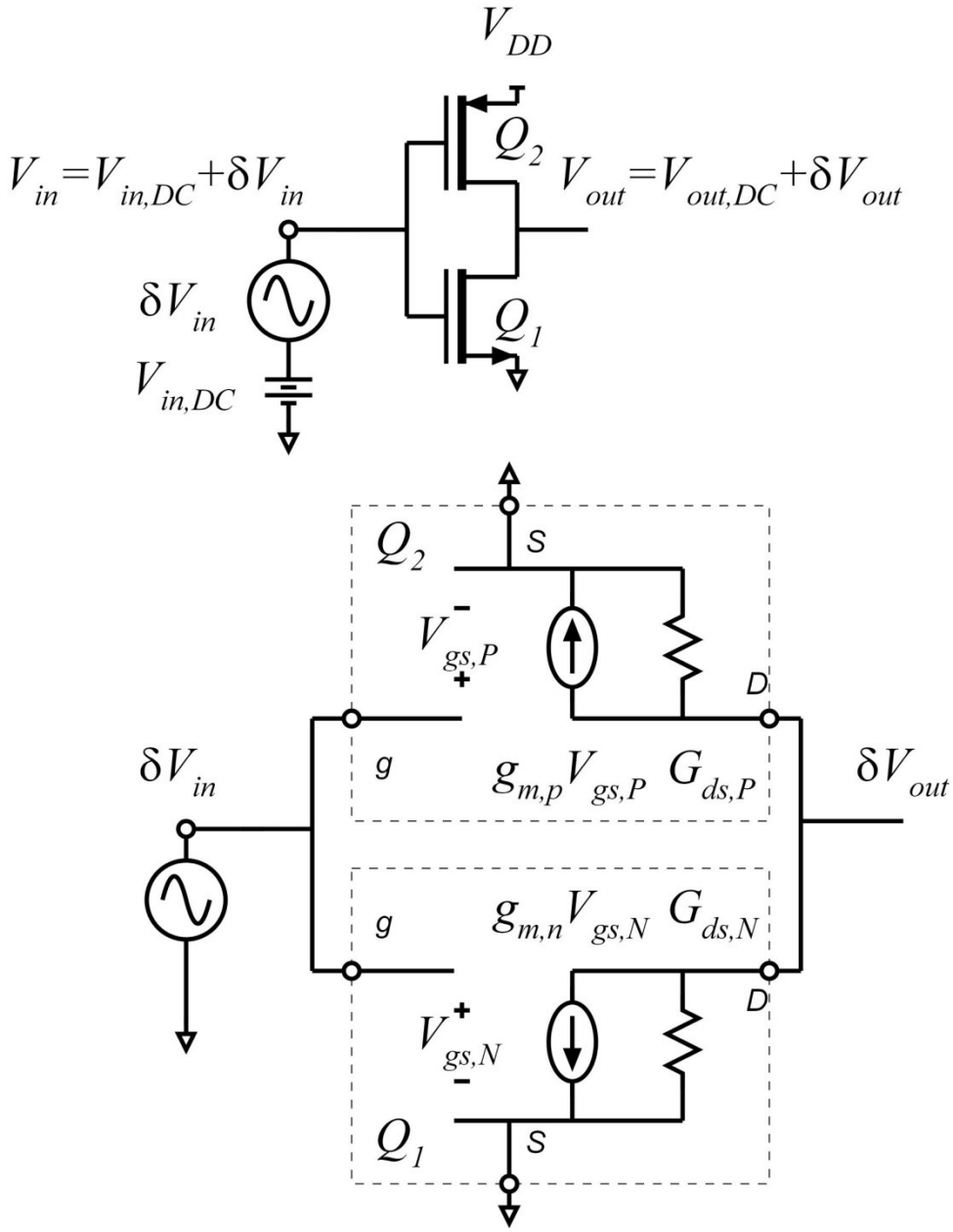
Analysis (same parameters for both FETs):

$$g_m = (\mu c_{ox} W_g / L_g)(V_{gs} - V_{th})(1 + \lambda V_{DS})$$
$$= (2\text{mA/V}^2)(0.5\text{V} - 0.3\text{V})(1 + 0.5\text{V}/10\text{V})$$
$$= 0.42\text{ mS}$$

$$I_D = (\mu c_{ox} W_g / 2L_g)(V_{gs} - V_{th})^2 \cdot (\text{skip the } \lambda V_{DS} \text{ term})$$
$$= (2\text{mA/V}^2)(0.5\text{V} - 0.3\text{V})^2 = 40\,\mu\text{A}.$$

$$G_{ds} = \frac{1}{R_{ds}} \cong \lambda I_D = \frac{40\ \mu\text{A}}{10\text{V}} = 4.0\ \mu\text{S} = \frac{1}{250\text{k}\Omega}$$

CMOS Amplifier: Small-Signal Equivalent Circuit



Steps:

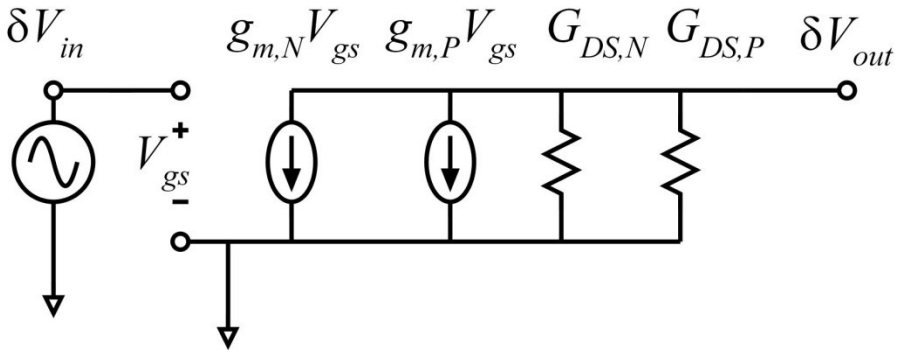
Replace each FET
with it small signal model.

Be careful: connect S-S, D-D, G-G
when replacing FET symbol
with SS model.

Replace Power supply and DC
sources with short-circuits.

Replace DC current sources
with open circuits.

CMOS Amplifier: Small-Signal Equivalent Circuit



Note that all NFET and PFET elements are in parallel.

Circuit thus simplies, as shown.

Analysis:

$$\delta V_{out} = -(g_{m,N} + g_{m,P})/(G_{DS,N} + G_{DS,P}) \cdot \delta V_{in}$$

$$\frac{\delta V_{out}}{\delta V_{in}} = -\frac{g_{m,N} + g_{m,P}}{G_{DS,N} + G_{DS,P}} = -\frac{0.42\ \text{mS} + 0.42\ \text{mS}}{4.0\ \mu\text{S} + 4.0\ \mu\text{S}}$$

$$\frac{\delta V_{out}}{\delta V_{in}} = -105$$