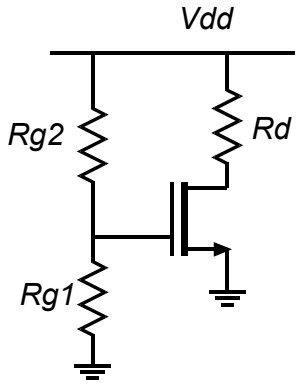
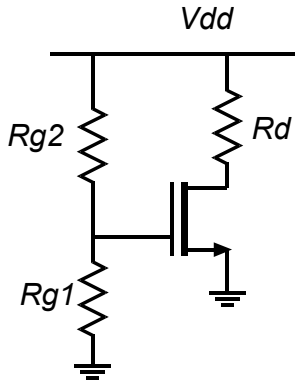
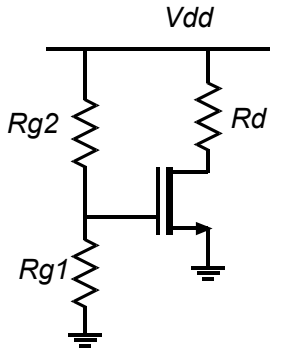
Example set #1:



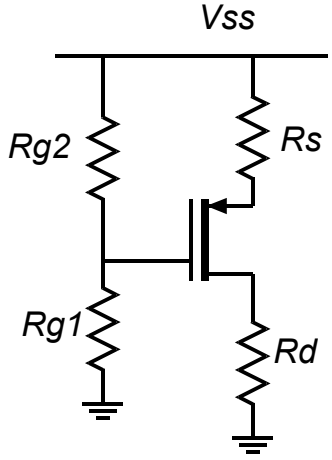
a) The MOSFET has a +0.3 Volt threshold voltage and $v_{sat}C_{ox}W_g$=1.5 mA/V (assume velocity-limited characteristics, i.e. $I_d = v_{sat}C_{ox}W_g(V_{gs}-V_{th})(1+\lambda V_{ds})$) , where we will assume $\lambda = 0\ \mathrm{V}^{-1}$
Rg1 is 1 MOhms. Vdd is 1.0 Volts.
lambda=0
We would like to bias the MOSFET at 0.1 mA drain current and 0.6 volts between drain and source.
Please find the required values of Rg2 and Rd.



b) Bias stability of the circuit of problem 1(a).
First, keeping the same values for Rg1, Rg2, and Rd you found above, compute the drain current and the drain voltage if $v_{sat}C_{ox}W_g$ is increased to 10%. Second, using the original value $v_{sat}C_{ox}W_g$, and keeping the same values for Rg1, Rg2, and Rd you found in 1(a), compute the drain current and the drain voltage if the power supply voltage is increased 10%.

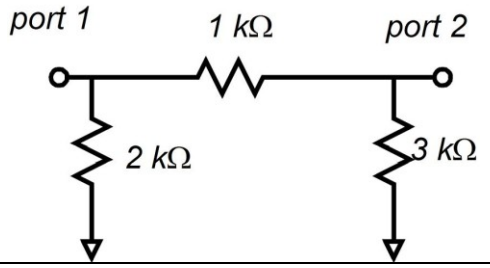
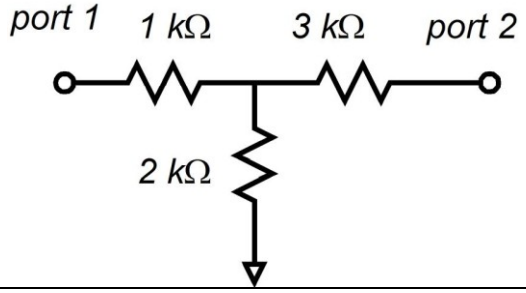
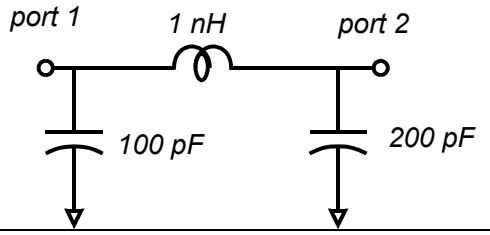
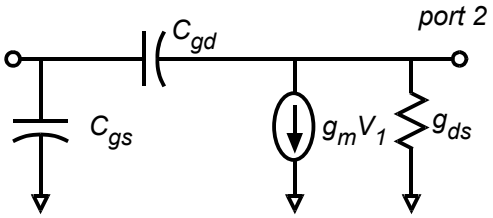
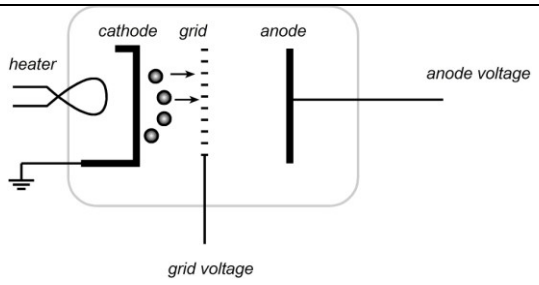


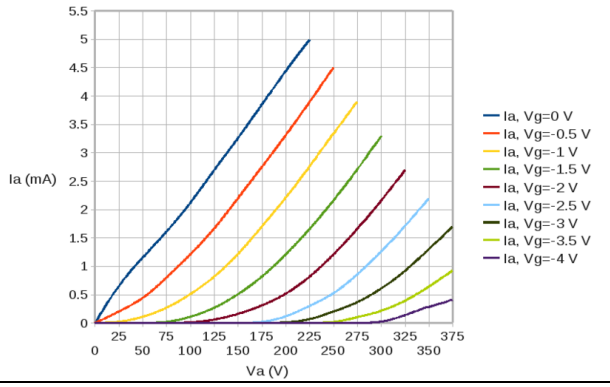
c) We will now consider a mobility-limited FET, ie. $I_d = (\mu C_{ox}W_g/2L_g)(V_{gs}-V_{th})^2(1+\lambda V_{ds})$ where $(\mu C_{ox}W_g/2L_g)$=1 $\mathrm{mA/V^2}$ and $\lambda = 0\ \mathrm{V}^{-1}$
The power supply is again 1 Volt. The threshold is 0.3 V. Pick Rg1 and Rg2 so that 5 microamps flow through them, and so that the drain current is 0.5 mA. Find Rd such that the drain is at 0.7 Volts.



d) The P MOSFET has a -0.3 V threshold voltage…meaning the gate is 0.3 V negative of the source at the onset of conduction. Use a constant-velocity model: $v_{sat}C_{ox}W_g = 0.25$ mA/V. λ=0 V^{-1}
V_{ss} =1 Volts and R_{g1} has 1 microamp flowing through it. We would like to bias the MOSFET at 50 μA drain current. We would like to have +0.8 volts source voltage and +0.2 V drain voltage. Find all 4 resistors.

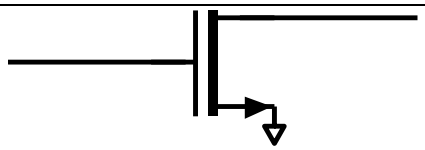
Example set #2 (2-port parameters, small signal parameters, loadlines)

Problem 1: (a) Compute the 2-port Y parameters of the circuit (b) Compute the Z parameters.	
Problem 2: (a) Compute the 2-port Y parameters of the circuit (b) Compute the Z parameters.	
Problem 3: At a signal frequency of 1 GHz, find the Y parameters	
Problem 3: This is a simple FET model (a) As function of frequency, find algebraic expressions for the Y parameters. (b) Now setting Cgd=0 fF, compute the impedance parameters as a function of frequency.	
Problem 4: meaning of small signal parameters. A triode vacuum tube is shown to the rigth. Typical IV characteristics are also shown...Va is the anode voltage and Vg is the Grid voltage. A tube's grid current is nearly zero as long as the grid is more negative than the cathode, and the anode current is given by $I_a = k_p(V_g + V_a/\mu)^{3/2}$ where μ is known as the amplification factor and k_p is a characteristic of the tube having units of amps per volt^3/2. (a) Defining the output conductance as	

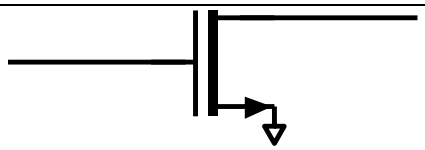
$\partial I_a / \partial V_a$ and the transconductance as $\partial I_a / \partial V_g$, derive expressions for these. (b) Working with the characteristics above, compute numerical values of the transconductance and output conductance at Va=200 V and Vg= -0.5 Volts	

Example set # 3 :

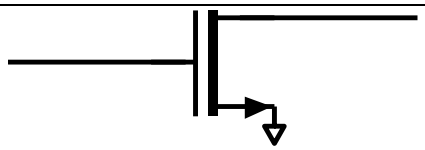
Problem 1: The MOSFET has a +0.3 Volt threshold voltage and $v_{sat}C_{ox}W_g$=0.5 mA/V (assume velocity-limited characteristics, i.e. $I_d = v_{sat}C_{ox}W_g(V_{gs}-V_{th})(1+\lambda V_{ds})$) , where we will assume λ=0.25 V^{-1}. If the device is biased with 1 Volts Vds and Vgs=0.5 Volts, find the transconductance and output conductance.



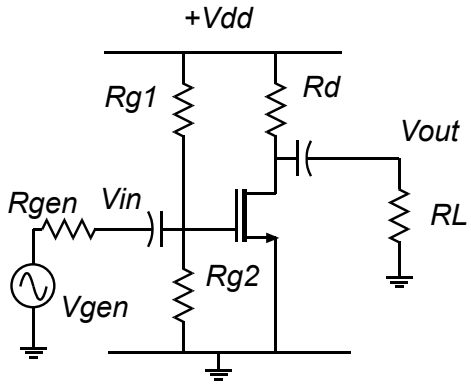
Problem 2: The MOSFET has a +0.3 Volt threshold voltage and $v_{sat}C_{ox}W_g$=0.5 mA/V (assume velocity-limited characteristics, i.e. $I_d = v_{sat}C_{ox}W_g(V_{gs}-V_{th})(1+\lambda V_{ds})$) , where we will assume λ=0.25 V^{-1}. If the device is biased with 1 Volts Vds and 0.25 mA drain current, find the transconductance and output conductance



Problem 3: We will now consider a mobility-limited FET, ie. $I_d = (\mu C_{ox}W_g/2L_g)(V_{gs}-V_{th})^2(1+\lambda V_{ds})$ where $(\mu C_{ox}W_g/2L_g)$=1 mA/V^2 and λ=0.25 V^{-1}. If the device is biased with 1.5 Volts Vds and 0.25 mA drain current, find the transconductance and output conductance



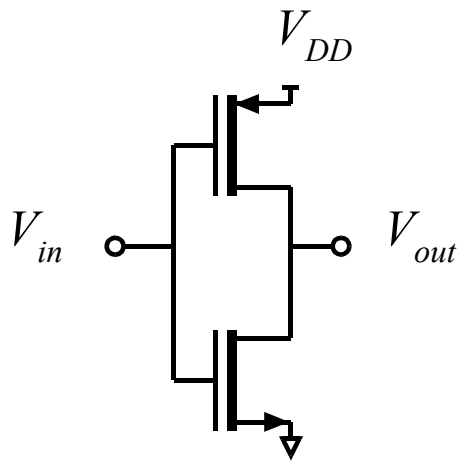
Problem 4



a) The transistor -constant mobility model- has a threshold of +0.3 Volts, and λ=0.1 V^{-1}.
The gate length is 130 nm, the oxide thickness 0.9 nm, the mobility is 300 cm^2/(V-sec).
Find the gate width necessary to carry 1 mA drain current at Vgs = 0.4 V.
b) Vdd is +2 volts. Rgen=50 kOhm, RL=100 kOhm Find the drain resistance Rd necessary to obtain Vd=1 V. We want the *input impedance (Rg1 and Rg2 in parallel) to be 1 MOhm.Find Rg1, Rg2
c) Find the following small signal transistor parameters: gm, Rds
d) draw the small-signal equivalent circuit of the amplifier, taking all capacitors as AC shorts and supplies as AC ground.
e) find the ac small signal input impedance, and the AC voltage gains Vout/Vin, Vin/Vgen and Vout/Vgen.

Problem 5: Another common-source amplifier

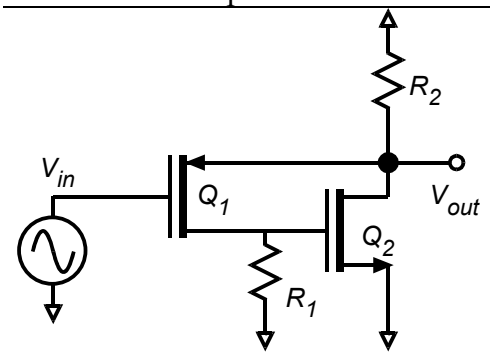
a) Use constant-velocity models.
Thresholds are +/- 0.3 V for the NMOS and PMOS FETs. λ=0.2 V^{-1}, the gate length is 65



nm, and the oxide thickness 0.9 nm. The NMOS FET has $v_{sat}=10^7$ cm/s; the value for the PMOSFET is half this. The NMOS FET has 5 microns gate width, the PMOS FET 10 microns. Vdd is 1.0 Volt. The input has 0.5 V DC bias, to which a small-signal input voltage is added. Compute the DC values of Vout and drain current.
b) Find the following small signal transistor parameters: gm, Rds for both transistors.

c) draw the small-signal equivalent circuit of the amplifier.

d) find the ac small signal voltage gain Vout/Vin



Problem 6 . Nodal Analysis exercise. This is a "super-buffer". Ignore DC bias analysis. You don't need it. The two transistors have transconductance gm1 and gm2 respectively. Their drain-source resistances Rds1 and Rds2 are both infinity.
a) Compute Vout/Vin by nodal analysis.
b) find numerical values of Vout/Vin given gm1=10 mS, gm2=100 mS, R1=5kOhm, R2=500 Ohms.

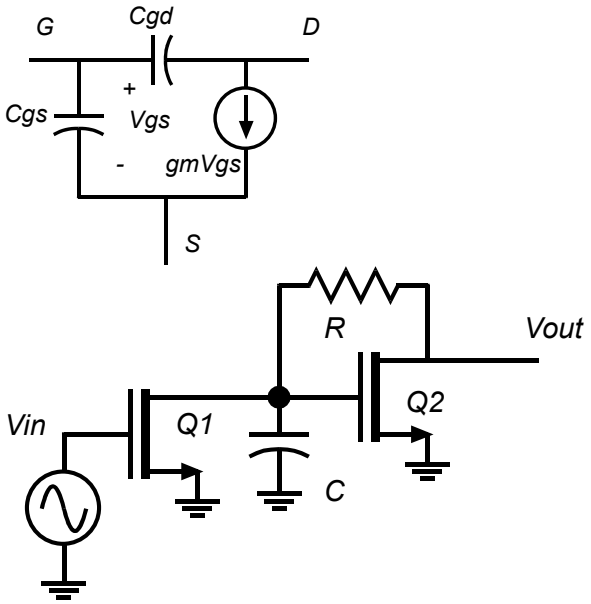
Example set #4:

Problem 1: The problem uses the MOSFET equivalent circuit to the right. Note the capacitances Cgs and Cgd which model high-frequency effects. This circuit is a transconductance-transimpedance amplifier. Ignore DC bias; you don't need it.

Q1: $C_{gs}=C_{gd}$=0. R_{ds}=infinity.

Q2: $C_{gs}=C_{gd}$=0. R_{ds}=infinity

gm1= 10 mS. gm2=20 mS. R=1000 Ohms. C=1 pF. (a) Draw an accurate small-signal equivalent circuit model of the circuit Do not show components whose element values are zero or infinity.



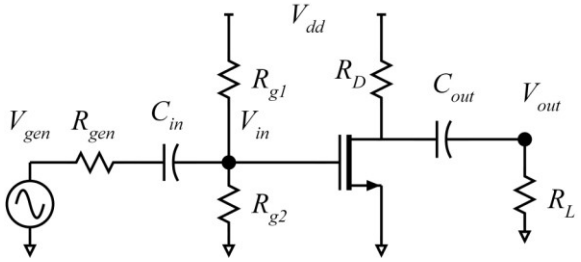
(b) Using NODAL ANALYSIS, find the transfer function Vout(s)/Vgen(s). The answer must be in standard form

$$\frac{V_{out}(s)}{V_{gen}(s)}=\frac{V_{out}}{V_{gen}}\bigg|_{DC}\frac{1+b_1s+b_2s^2+...}{1+a_1s+a_2s^2+...}$$

(c) Find any/all pole and zero frequencies of the transfer function, in Hz. (d) Draw a clean Bode Plot of Vout/Vin. On the plot, LABEL AXES, LABEL all relevant gains and pole or zero frequencies, Label Slopes. The plot should be drawn on printed semilog paper, and should have axes of Hz, (not rad/sec) and dB. (e) Vin(t) is a 100 mV amplitude step-function. Find Vout(t). Draw a clean graph

Problem 2:. Rg1=Rg2=1 MΩ. R_{gen}=100 kOhm. Rd=RL=10 kΩ. $C_{out}=C_{in}$=infinity, The transistor has g_m = 10 mS R_{ds}=100 Ohms, C_{gs}=100 fF, C_{gd}=0 fF.

(a) Draw an accurate small-signal equivalent circuit model of the circuit. Do not show components whose element values are zero or infinity.



(b) Using NODAL ANALYSIS, find the transfer function Vout(s)/Vgen(s). The answer must be in standard form

$$\frac{V_{out}(s)}{V_{gen}(s)}=\frac{V_{out}}{V_{gen}}\bigg|_{DC}\frac{1+b_1s+b_2s^2+...}{1+a_1s+a_2s^2+...}$$

(c) Find any/all pole and zero frequencies of the transfer function, in Hz. (d) Draw a clean Bode Plot of Vout/Vin. On the plot, LABEL AXES, LABEL all relevant gains and pole or zero frequencies, Label Slopes. The plot should be drawn on printed semilog paper, and should have axes of Hz, (not rad/sec) and dB. (e) Vgen(t) is a 10 mV amplitude step-function. Find Vout(t). Draw a clean graph

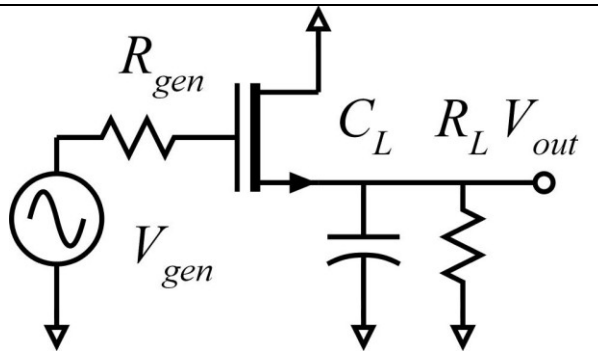
Problem 5: Same circuit diagram and values as problem 4, except C_{out}=10 μF and C_{gs}=0

(c) Find any/all pole and zero frequencies of the transfer function, in Hz. (d) Draw a clean Bode

fF** (a) Draw an accurate small-signal equivalent circuit model of the circuit (b) Using NODAL ANALYSIS, find the transfer function Vout(s)/Vgen(s). The answer must be in standard form	Plot of Vout/Vin. On the plot, LABEL AXES, LABEL all relevant gains and pole or zero frequencies, Label Slopes. The plot should be drawn on printed semilog paper, and should have axes of Hz, (not rad/sec) and dB. (e) Vgen(t) is a 10 mV amplitude step-function. Find Vout(t). Draw a clean graph

Example set #5:
These are exercises in nodal analysis, real and complex poles, and finding (and plotting) the frequency and transient response of circuits. .

Problem 1: The problem uses the MOSFET equivalent circuit to the right. Note the FET input capacitance Cgs.



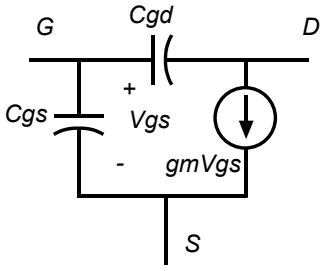
Ignore DC bias analysis. You don't need it. The transistor has transconductance gm. Its output resistance Rds is infinity.
(a) Draw a small-signal equivalent circuit of the circuit. (b) gm=20 mS. Cgs=1 pF, C_L=20 pF. R_L=200 Ohms, R_{gen}=500 Ohms Find, by nodal analysis, a small-signal expression for Vout(s)/Vgen(s), with the answer given in dimensionless ratio-of-polynomials form:

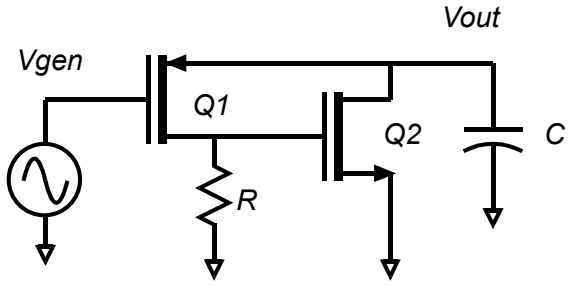
$$Ks^m \frac{1+a_1 s+a_2 s^2+\ldots}{1+b_1 s+b_2 s^2+\ldots}$$

(c) Find any/all pole and zero frequencies of the transfer function, in Hz: Draw a clean Bode Plot on semilog paper of Vout/Vin, LABEL AXES, LABEL all relevant gains and pole or zero frequencies, Label Slopes

(d) Vgen (t) is a 100 mV amplitude step-function. Find Vout(t), and plot it below. Label axes, show initial and final values, show time constants

Problem 2: The problem uses the MOSFET equivalent circuit to the right. Note the capacitances Cgs and Cgd which model high-frequency effects.
The circuit is called a super-buffer. Ignore DC bias; you don't need it.
Q1: $C_{gs}=C_{gd}$=0. R_{ds}=infinity.
Q2: C_{gs}= 100 fF, C_{gd}=0. R_{ds}=infinity
$g_m 1=g_m 2$=50 mS, R=2000 Ohm, C=200 fF
(a) Draw a small-signal equivalent circuit of the circuit.
(b) Compute by nodal analysis the small signal transfer function Vout/Vgen , with the answer given in dimensionless ratio-of-polynomials form:





(d) Plot an accurate root locus. (e)

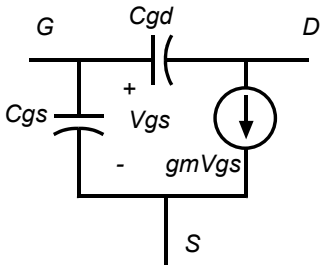
$$Ks^m \frac{1 + a_1 s + a_2 s^2 + \ldots}{1 + b_1 s + b_2 s^2 + \ldots}$$

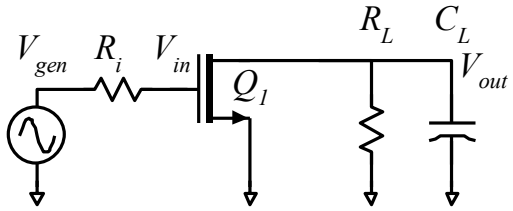
(c) Find the damping factor ζ and the resulting natural resonant frequency f_n.

Accurately plot the Magnitude of the frequency response in Bode Form on semilog paper. (f) If Vgen(t) is a 1 mV step-function, plot Vout(t).

Problem 3: The problem uses the MOSFET equivalent circuit to the right. Note the capacitances Cgs and Cgd which model high-frequency effects.
The circuit is a standard common-source stage. Ignore DC bias; you don't need it.
(a) Draw a small-signal equivalent circuit of the circuit.
(b)Compute by nodal analysis the small signal transfer function Vout/Vgen , with the answer given in dimensionless ratio-of-polynomials form:

$$Ks^m \frac{1 + a_1 s + a_2 s^2 + \ldots}{1 + b_1 s + b_2 s^2 + \ldots}$$



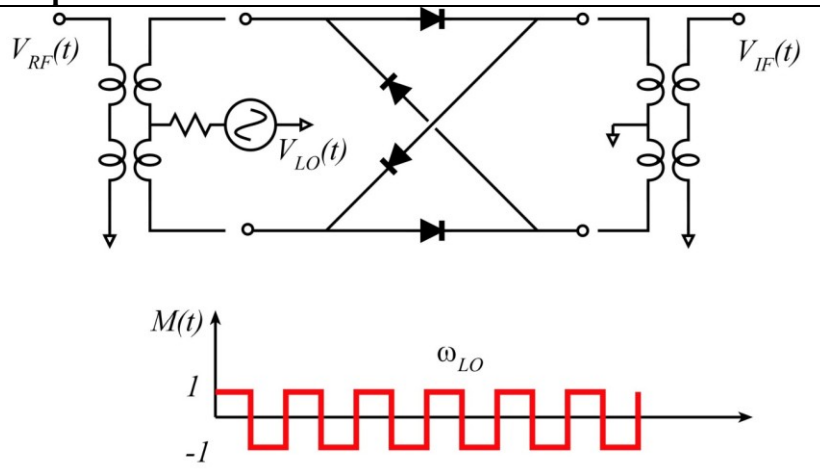


(c) C_{gs} = 100 fF, C_{gd}=10 fF R_{ds}=infinity. g_m=50 mS, RL=2000 Ohm, Ri=1000 Ohms, C_L=10 fF. Find the poles of the transfer function.

(d) Find any/all pole and zero frequencies of the transfer function, in Hz: Draw a clean Bode Plot on semilog paper of Vout/Vin, LABEL AXES, LABEL all relevant gains and pole or zero frequencies, Label Slopes
(e) Vin(t) is a 100 mV amplitude step-function. Find Vout(t), and plot it below. Label axes, show initial and final values, show time constants

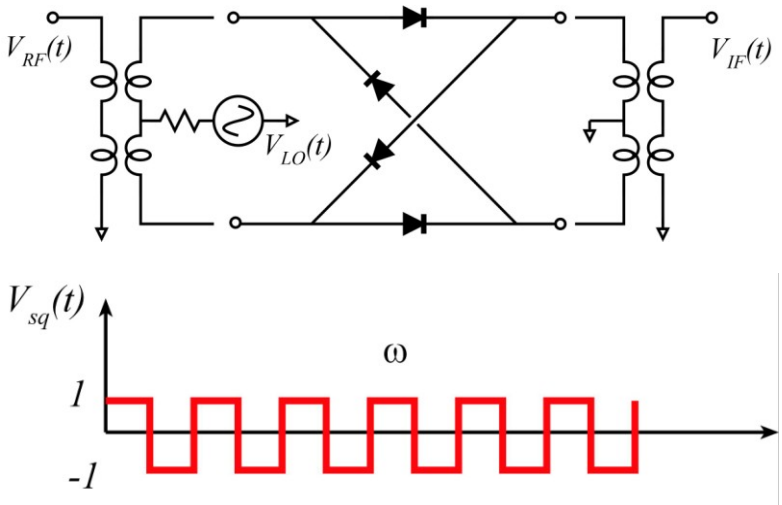
Example set #6: A few more problems on mixers

Problem 1: The diode bridge mixer has ideal diodes (zero on-resistance, infinite off-impedance). The transformer ratios are all 1:1. The LO is a cosine wave at 1.0 GHz. The IF port is loaded in 50 Ohms. If $V_{RF}(t)$ is a 100 MHz sine wave of 1 mV peak amplitude, (a) make a graph of $V_{IF}(t)$.



(b) find the Fourier amplitudes of the mixer output at the sum and difference frequencies

Problem 2 : (possibly too hard for ece2c) In the mixer at right, the LO power is sufficient to drive the diodes into zero ohms in forward conduction and infinity ohms in reverse bias. The Fourier series of a squarewave is given to the right.



The RF frequency is 60 GHz, while the IF frequency is 10 GHz.

$$V_{sq}(t) = \frac{4}{\pi}\left[\cos(\omega t) + \frac{\cos(3\omega t)}{3} + \frac{\cos(5\omega t)}{5} + \ldots.\right]$$

In order to save cost on the LO design, we choose to use the $\cos(3\omega t)$ term for mixing of the 60 GHz received signal to the 10 GHz IF. Given this, there are two possible choices for LO frequency. Again, to save cost pick the lower of these. What would it be ? What would be the effect upon the *voltage gain* of the mixer by using the $\cos(3\omega t)$ term instead of the $\cos(\omega t)$ term ?