Mask Layout Design Guide

For ECE218C, UCSB

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After the design of an integrated circuit, we need to layout all the active, passive components and interconnection wires and generate GDSII bit file in some computer program (such as Cadence's virtuoso or ADS layout utility) in order to fabricate it. When you look at a fabricated chip, there is a top view (horizontal direction) and cross-section view (vertical direction). See Fig.1. Layout is to draw the geometry only for the top view (or layout view), which usually consists of multiple layers from the substrate all the way up to the top metal. You don't have control over the cross-sectional geometry. For example, you can draw a wire's width and length, but you cannot determine its thickness. The cross-sectional geometry is automatically controlled in the process line.

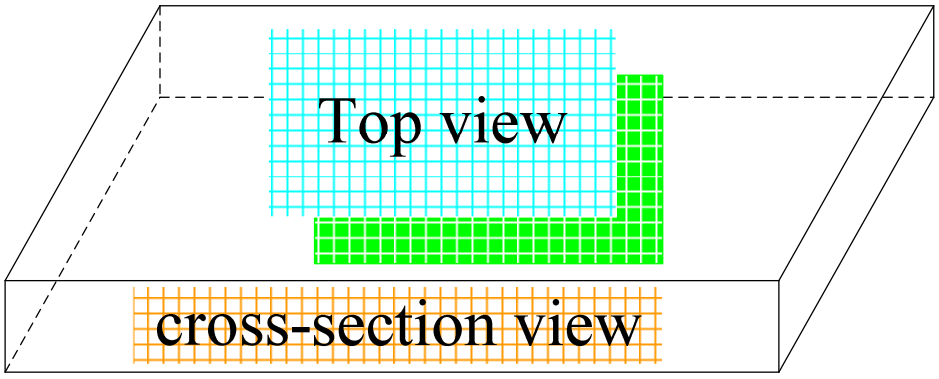

Fig.1 top view and cross-section view of an integrated circuit

It's a good idea to look at the cross-section view of a process to learn which layers are available to draw the layout. In this course, the entire layout is based on UCSB's Mesa InP HBT process, which consists of 3 metal layers, inter-layer Vias, semiconductor layers, and so on. See Fig. 2. The top metal (metal3) is used as a continuous ground plane for microstrip interconnects, so we cannot use this layer for interconnection. Pads for connection from the chip to the outside world are however also drawn in this layer. But we can and should connect any ground node in our circuit to metal3 through M2-M3 via (or for bypass capacitors, capmetal-M3 via), as the use of a continuous ground plane eliminates ground return inductance and provides a predictable inductance/length and capacitance/length for all interconnects. Metal1 and Metal2 are free to be used for interconnection. If one needs to go from one layer of interconnection to another, we need to use Vias for inter-layer connection. Vias are basically holes in the dielectric, which are filled with conducting material. When Vias are made, BCB or Si3N4 dielectric will etched out in the area where Vias are laid out. The etching is finally stopped by the underneath metal. The detailed design rules for HBT, resistor, capacitor, wire, and pads will be explained in the following.

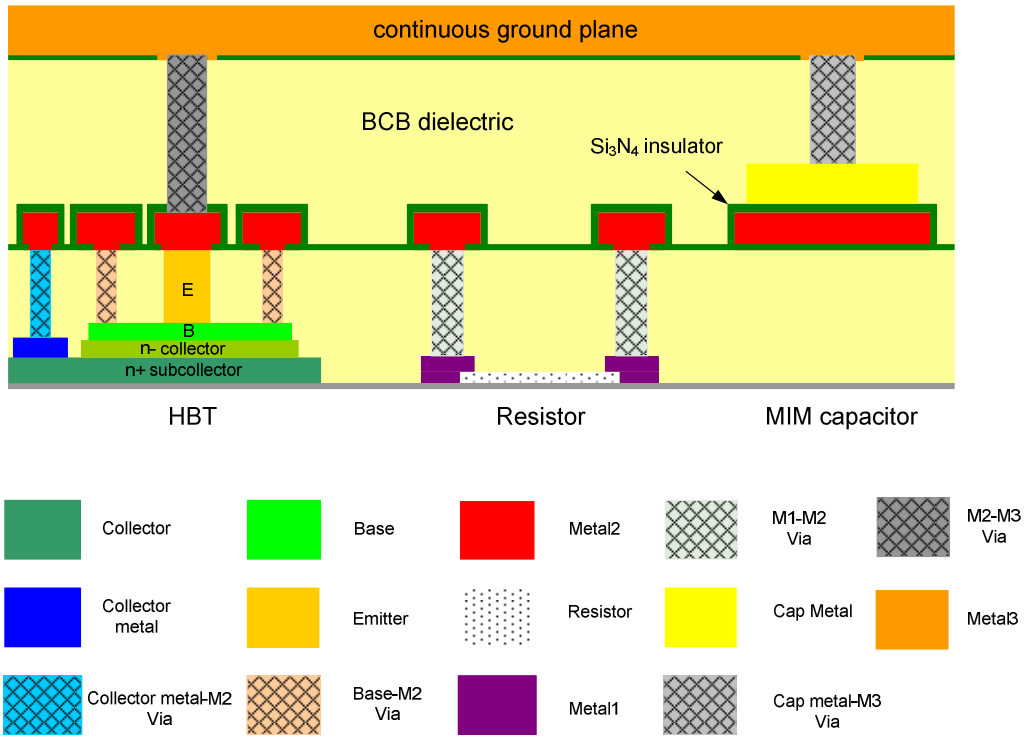

Fig. 2 Cross-section view of UCSB's Mesa process

The mask design rules for this process are a mix of 0.25µm and 0.5µm. For emitter and base layout, 0.25µm design rules are used. For all the remaining layers, including collector, resistor, capacitor, wire, via, and pad, 0.5µm design rules should be used. For instance, consider the following two traces of metal1 which are parallel to each other (Fig. 3), the width of each metal1 trace and the spacing between them should be greater than 0.5µm. Metal conductor width must be sufficient to carry the current: the maximum DC current is 2 mA/µm times the conductor width. If this value is exceeded, the wire may be moved physically by the current: electro-migration. Varying the conductor width will also change the characteristic impedance of the interconnect. If the two metal traces are on different layers, then generally there is no spacing requirement between them.

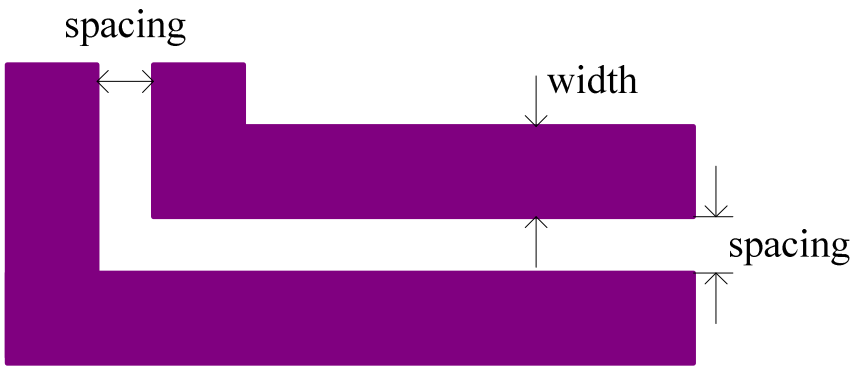

Fig. 3. two traces of metal1

The process design rules (of all layers except the emitter and base) are 1/2 micron. This means that there may be a 1/2 micron relative misalignment of any two layers. Consequently, vias should be placed with their outside edges at least 1/2 micron inside the metal regions which they contact. Additional design rules for Vias are explained in Fig. 4. So Vias has a minimum geometry of 0.5μm by 0.5μm and a maximum geometry of 10μm by 10μm or in between. The spacing between the same kinds of Vias is 5μm. Generally speaking, assume a maximum current density of 1 mA/(square micron) in each via. But one cannot use arbitrarily large number of Vias. Design rule requires a maximum Vias density of 50%, which is the ratio of total area of Vias to area of each surrounding metal pieces.

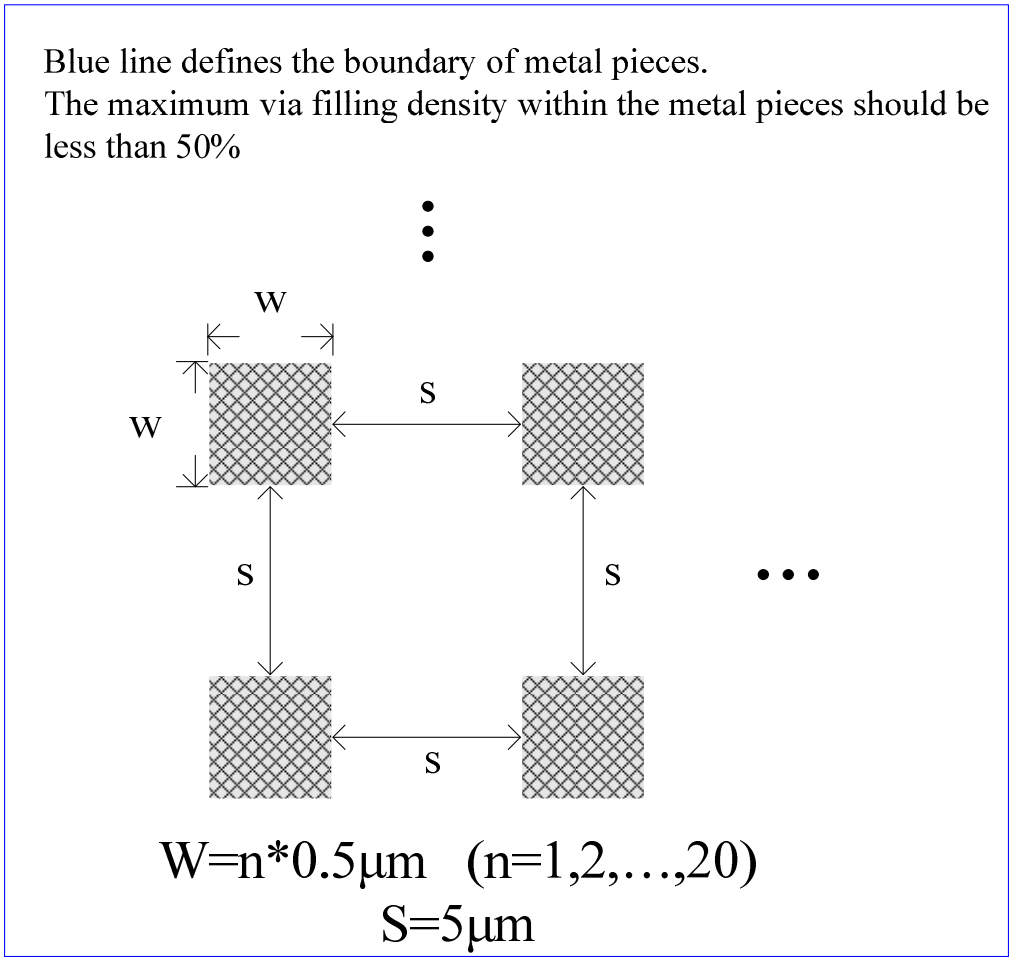

Fig. 5 design rules for Vias array

In order to layout a large Vias array (such as 10 by 10), one doesn't need to draw each Via one by one. A common method is to use "copy & paste" or create "instance". In "copy & paste", you draw a single via, copy it, and paste to another location 5μm away horizontally or vertically. In ADS, there is advanced "copy & paste" feature (step and repeat) which allows you to copy a Via to a Vias array in one command. You can also create a "Via instance" and insert multiple copies of this instance into your layout. A nice feature about the "instance" method is that when you make change to the instance file it will automatically be reflected to all the copies. That's different than the "copy & paste" method, where you have to change each copy one by one, or delete the copies and do the procedure again. The above discussion applies to other types of components as well.

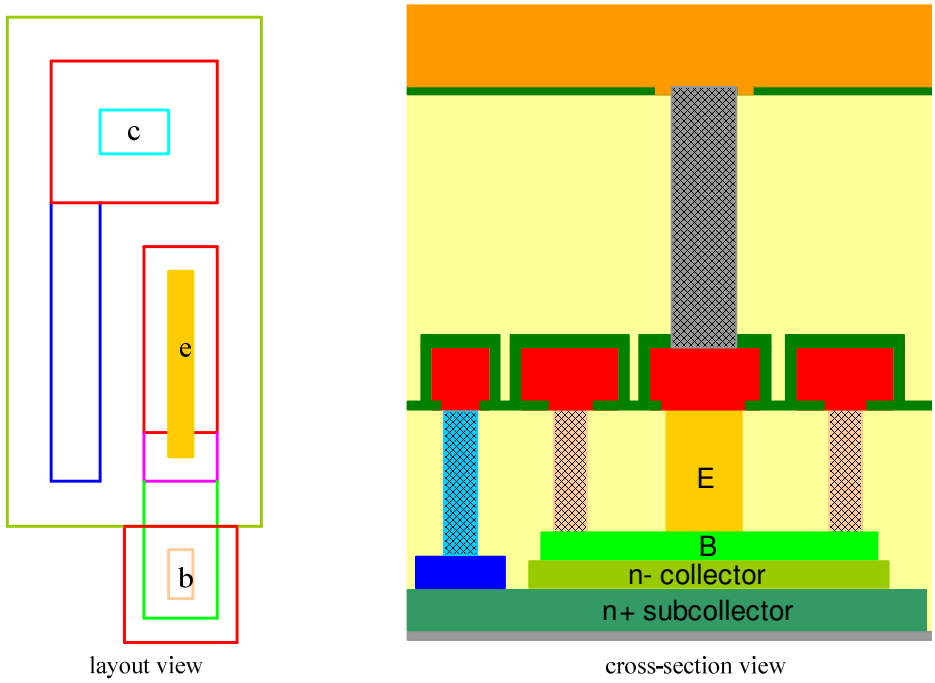

Fig. 6 layout view and cross-sectional view of HBT (not to scale)

In the process design kit (PDK) library, there are HBT mast layout of 0.25 x M μm (M=1, 2, 4, 8) available for use. The numbers tell about emitter's geometry. Base and collector's geometry scale according to emitter's size. BaseMesa is vertically etched base semiconductor. The top of emitter has the same height as the bottom of metal2, so no via is needed to bring them together. There is no layout layer for n- collector, which is automatically patterned in the same step as the base. The mix of 1/4 and 1/2μm design rule needs to be followed in the layout. The key point here: it is better not to draw HBTs yourself; instead simply place copies of the HBT layouts already provided.

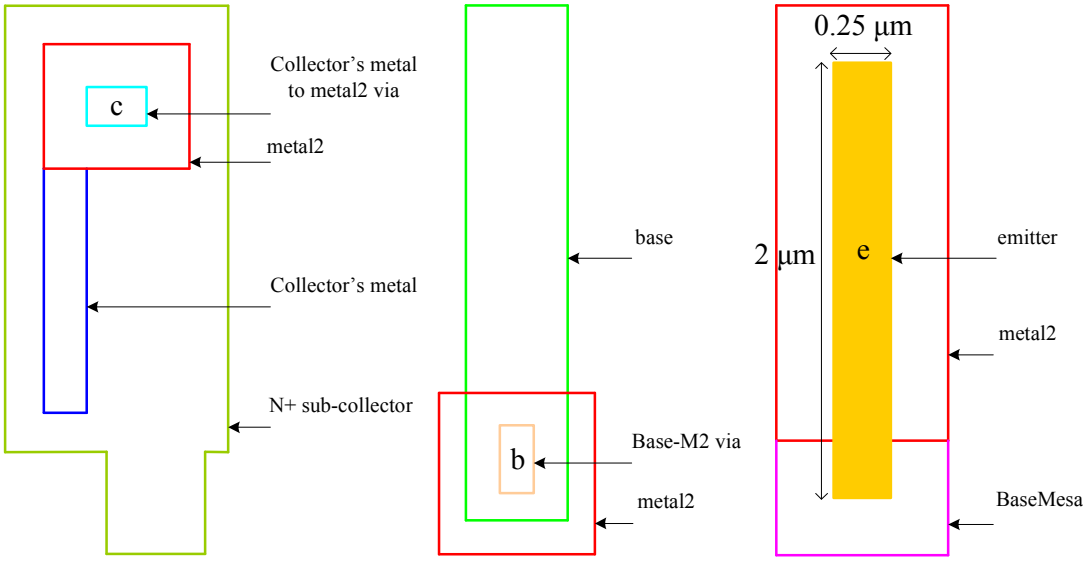

Fig. 7 layer explanation for HBT

Resistor

Resistor's layout consists of two layers, of which one is NiCR material and the other is metal1 contact. Width of resistors can be set for different currents through them. Like W=10μm can carry max of current=10 mA. NiCR layer has a sheet resistivity of 50 Ω/□, so the resistance can be calculated as 50Ω * length/width. That is to say, a 10μm by 10μm resistor has the same resistance as a 1μm by 1μm resistor, but they have different current carrying capability. The library provides a series of resistor layout models for use, but is likely you will need different resistor sizes, which you will need to draw on your own. Again, and 1/2μm design rules should be applied in the layout. Again, it is smart to draw, and then place multiple instances, rather than to draw, copy, and paste.

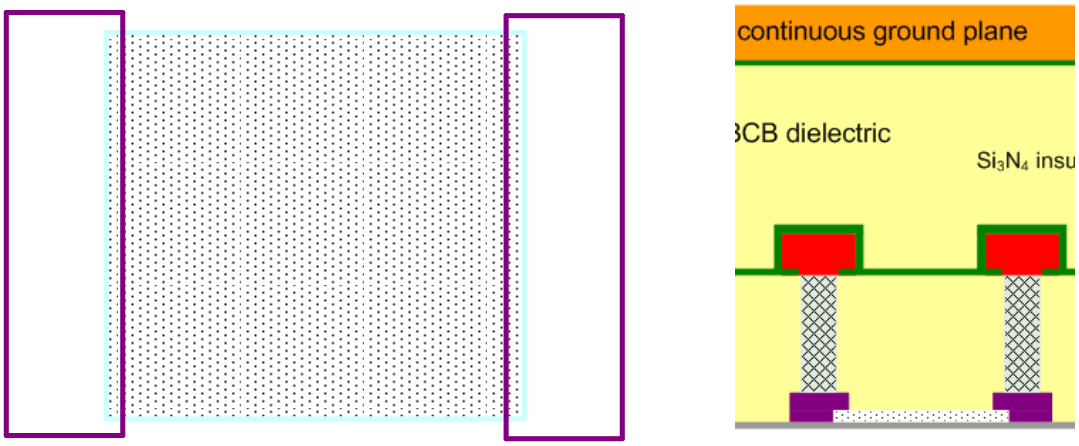

Fig. 8 layout view and cross-sectional view of a 10μm by 10μm resistor

Capacitor

The IC process is simple and does not provide general-purpose capacitors. Instead, the only capacitors available are those in which one terminal of the capacitor is connected to ground. These are used for AC grounding of nodes within circuits, and for power-supply bypassing. In this process, MIM (metal-insulator-metal) capacitor can be made with Metal2, Silicon Nitride insulator, and Capmetal. Since Capmetal can only be connected to Metal3 (the continuous ground plane). The capacitance can be calculated as C=A*ε/d. A is the area of the capacitor, d is the thickness of the insulator (d = 100nm), and ε is the electrical permittivity of Si_3N_4 material (≈$6.6x10^{-17}$F/μm). The design library provides one or two capacitor layout models for use, and you can use multiple instances of these to make larger values.

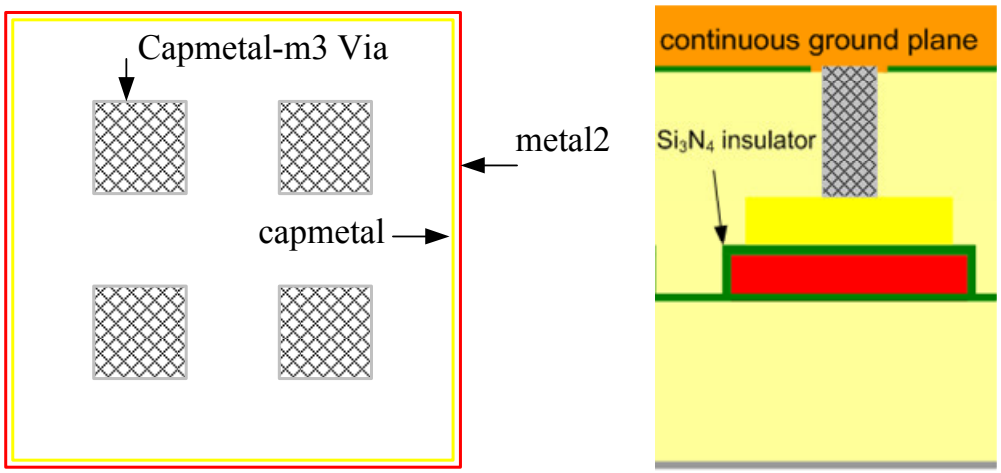

Fig. 9 layout view and cross-sectional view of a 1pF capacitor

Testing Pad

This is a GSG pad layout. G stands for ground and S stands for signal. Two of these can be put together to make GSGSG testing configuration.

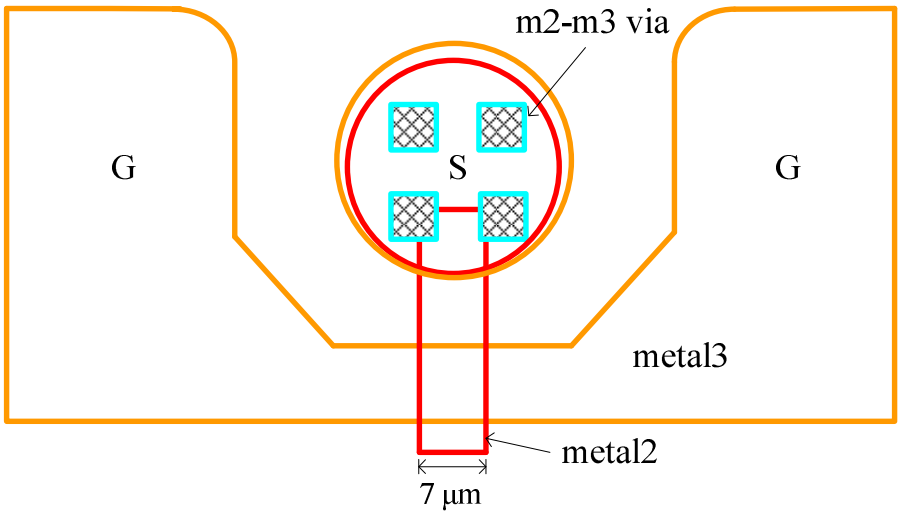

Fig. 10 layout view of GSG pad