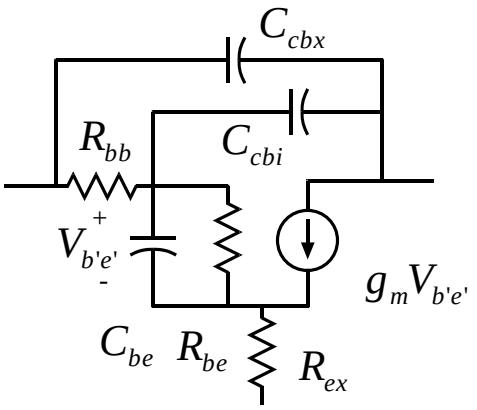
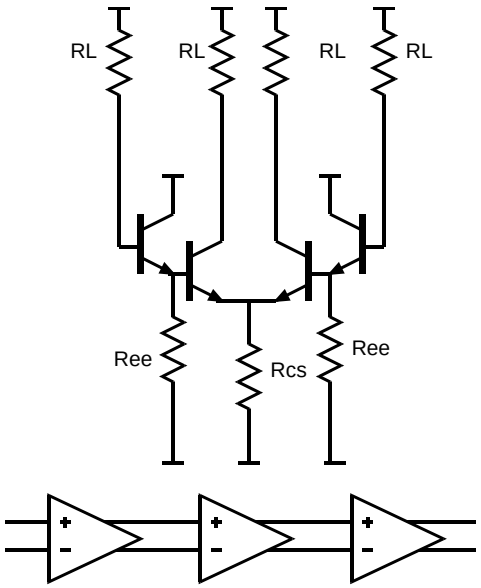


ECE194J/594J PS 3. Above is a device model . Recall that $C_{be} = C_{be,depl} + g_m \tau_f$. Let us take Cje=5.67 fF, beta=50, Ccbi=1.86 fF, Ccbx=1.34 fF, Rbb=14.7 Ohms, Rex=8 Ohms, and tau_f=0.244 ps. Lets use this device model in circuit calculations below. $g_m = qI / nKT$, where n=1.0. This is the model of a transistor having Ae=0.25 um x 4.0 um emitter area and biased at 1 mA/micron current density (4 mA total); the ft is 470 GHz ft and the fmax 825 GHz. It operates at a maximum of 2.5 mA/um at Vce=1.0 volts.

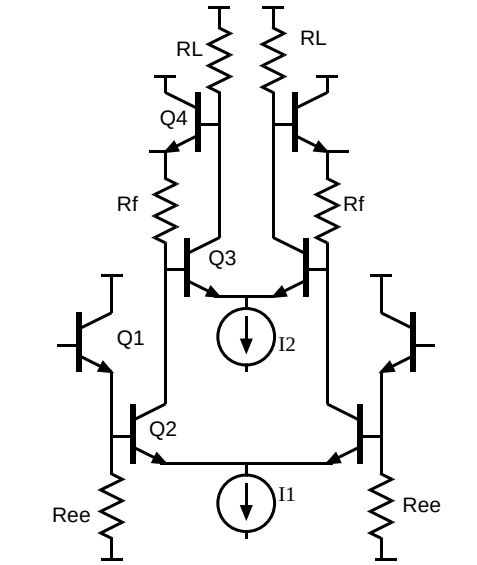
In the hand analysis ONLY (for problems 1 and 2), we will simplify by making Ccbi=(1.86+1.34) fF/micron*Le, and making Ccbx=0

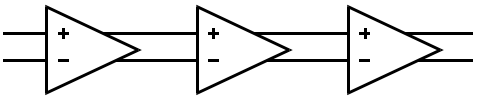


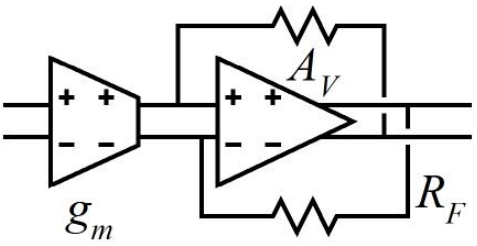
Problem 1: The circuit to the left is one stage in a string of identical differential stages. The positive supply is zero volts and the negative supply is -4.2 volts. Use the device model above, but scale the device area--and hence the model element values-- so that all the DC bias voltage drops across RL are 150 mA and the transistors are biased at 1 mA/micron current density. ***Note critically in this analysis that the load of each stage is RL/2 because of the input impedance of the input impedance of the cascaded stage.*** (this will determine Rcs, Ree). note that because we are dealing with a string of such stages, that will also set the DC input voltage of the stage to -150 mV. a) Find the differential voltage gain of one stage. b) Assuming an AC current

Please be very careful in the boundary conditions of the simulation to ensure that

the correct AC impedances and DC bias conditions are applied at both input and output. This will not happen automatically if you simply place the circuit into the simulator without addition of proper termination impedances and bias components.







generator input to the base of the emitter follower, find a1 and a2 of the transfer function (4 capacitor problem) and the resulting bandwidth and damping factor . c) Simulate using ADS (AC small-signal voltage gains) and compare with your hand analysis.

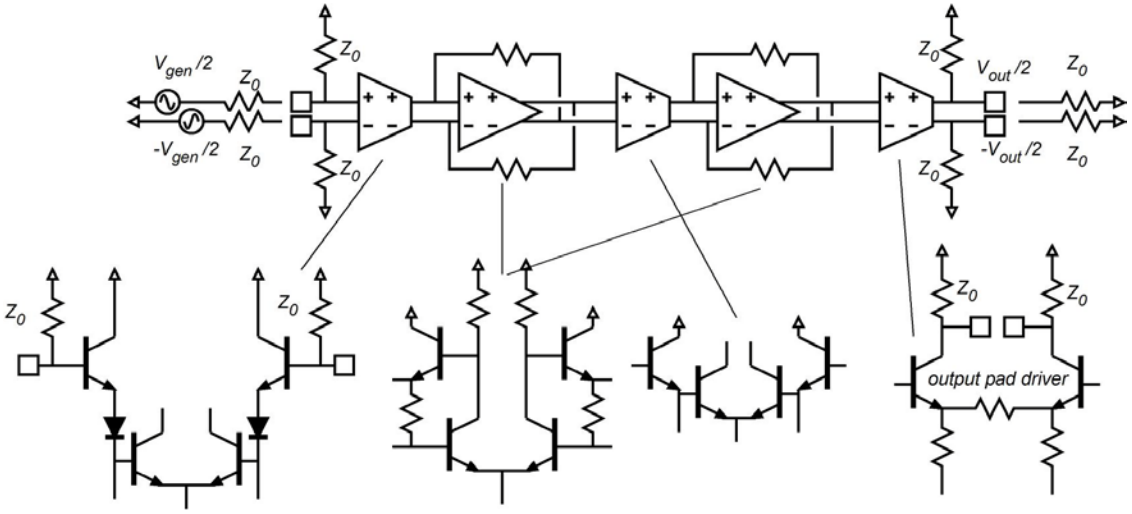
Problem 2: The circuit to the left is one stage in a string of identical differential stages. The positive supply is zero volts and the negative supply is -5.2 volts. Use the device model above, with transistors biased at 1 mA/micron and with 2 mA DC bias currents in all components. Choose RL so that its DC voltage drop is 150 mV and choose Rf so that its DC voltage drop is 100 mV. Note that because we are dealing with a string of such stages, that will also set the DC input voltage of the stage to ~ -1.1 V. a) Hand analysis: assume that Q1 and Q2 have no parasitic capacitances, change beta to infinity, and assume zero ohms drive impedance to the base of Q1. Then find a1 and a2 of the transfer function (4 capacitor problem) and the resulting bandwidth and damping factor (c) Place a long cascade of such amplifiers in ADS, simulate Vout/Vin (AC small signal voltage gain) compare with your hand analysis.

The bottom image is a block-diagram representation of a single TASTIS amplifier.

Problem 3: The TASTIS amplifier above has two difficulties in interfacing to an external 50 Ohm (chip-chip) environment. First, it will be convenient for all stages to have an external DC interface bias level of either -150 mV or 0 mV, and a maximum signal swing of 300 mVpp. This will aid in ECL and CML compatibility. Second, the

IC must interface with 50 Ohm source impedances and 50 Ohm loading, both at DC and at AC. Input level-shifting and termination is provide by changing the input of the first TASTIS stage to that shown below. Output level-shifting and termination is provided by the interfacing network shown below.

The overall amplifier, with input level-shifted gm stage, transimpedance stage, and output driver then appears as below:



Please do the following:

a) design by hand the output pad driver. It is to drive an external 50 Ohm environment (50 Ohms internal load, 50 Ohms external), and should have a DC output voltage of -150 mV. Pick the emitter degeneration resistor so that the gain of this stage is 0 dB. The transistors are again biased at 1 mA/micron.

b) compute by hand (MOTC method) a1 and a2 of the output buffer, again.

c) Enter the IC design into ADS and simulate both for the AC voltage gain of each stage, for eye patterns, and for S-parameters

d) generate a mask layout in ADS

e) enter the wiring elements into ADS and re-simulate.

Hint: the trick to save much work in mask layout, and in IC simulations, is to use layout instances heavily.
In generating mask layouts, generate objects in the following order:

1) differential pair with emitter pull downs and nonzero emitter degeneration. Omit the actual emitter degeneration resistor from the layout instance. You may need several versions of these with different emitter lengths and different pull down resistances

2) You can now create differential pairs with zero or nonzero emitter degeneration by creating new layout instances consisting of a grouping of object (1) with a emitter degeneration resistor (of zero or nonzero value), and creating a new instance from each such combination.

3) add input and output 50 Ohm lines to (2) and output terminations to make output buffer.

4) Add emitter follower input buffers to different versions of (2) (zero degeneration resistors, different emitter size) with and without level shift diodes to make the two gm blocks of the 2 TASTIS stages.

5) Take (2) with zero emitter degeneration resistance and add emitter follower output buffers and feedback resistors to make transimpedance stages.

6) Past these all together, route DC wiring, add input and output and DC pads, and you have made the full IC.

Second Hint: IC simulation files can be created in a similar hierarchical fashion. This will again vastly reduce the amount of work required.