ECE 194J/594J Design Project

Optical Fiber Amplifier and 2:1 demultiplexer.

Due Dates----What and When
Due March 12, 5 PM by email. Design files to class upload site.

Items due: a) Report (b) ADS mask layout file (c) ADS simulation file. Both (b) and (c) must be clearly organized.

For (c) there must be a highest level in the hierarchy having the title: "receiver transient simulation" which must contain with in a block called "receiver". The block called "receiver" should contain sub-blocks containing (1) the front end , (2) the amplifier chain , and (3) the demultiplexer. There should also be files called "TIA frequency sweep", "TIA eye pattern simulation", "linear amplifier chain frequency sweep", "limiting amplifier chain eye pattern simulation", "receiver frequency sweep", "receiver chain eye pattern simulation" which are correctly set up for the relevant simulations. Hierarchy below that level is up to you. Receiver here refers to the (TIA + amplifier chain), limiting amplifier chain refers to the chain of the receivers alone.

You can shorten these names as file size limits dictate, but be sure to be clear, and document your terminology in the design report.

For (b), there should be a similar hierarchy, with the highest level having the title "receiver". Within this should be separate blocks "TIA", "limiting amplifier", "demultiplexer", and "latch". Hierarchy below that level is again up to you.

Report should be clearly written and well organized. It should contain =
-readable circuit diagrams with HBT junction sizes, R and C values, bias currents and voltages.
-a good set of screen shots (with sensibly chosen sets of zoom levels) of the IC layout.
-simulations of frequency response and eye patterns of TIA and limiting amplifier, each alone and in combination. Eye simulations should be at a low level corresponding to sensitivity and at a high level corresponding to the maximum for correct operation.
-hand analyses of relevant circuit performance to the level feasible. Bandwidth, gain, digital logic speed.
-discussion of key design decisions.

Joe Friday Style: no fluff or philosophy. Just the facts. All the facts. Any performance data simulation or analysis that is relevant.

Background

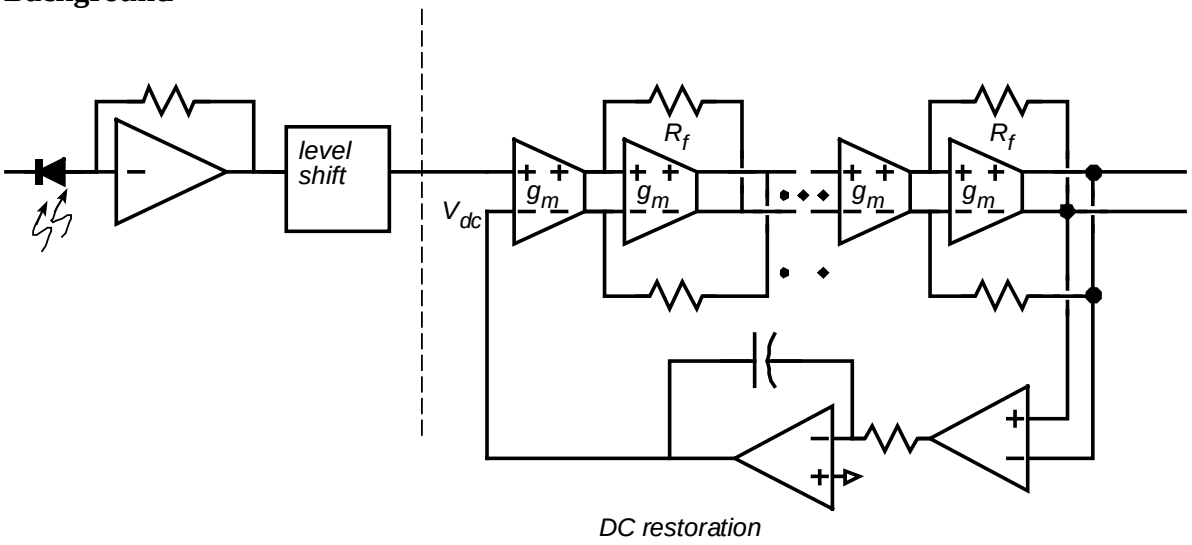


Figure 1: Optical Fiber Receiver Front-End .

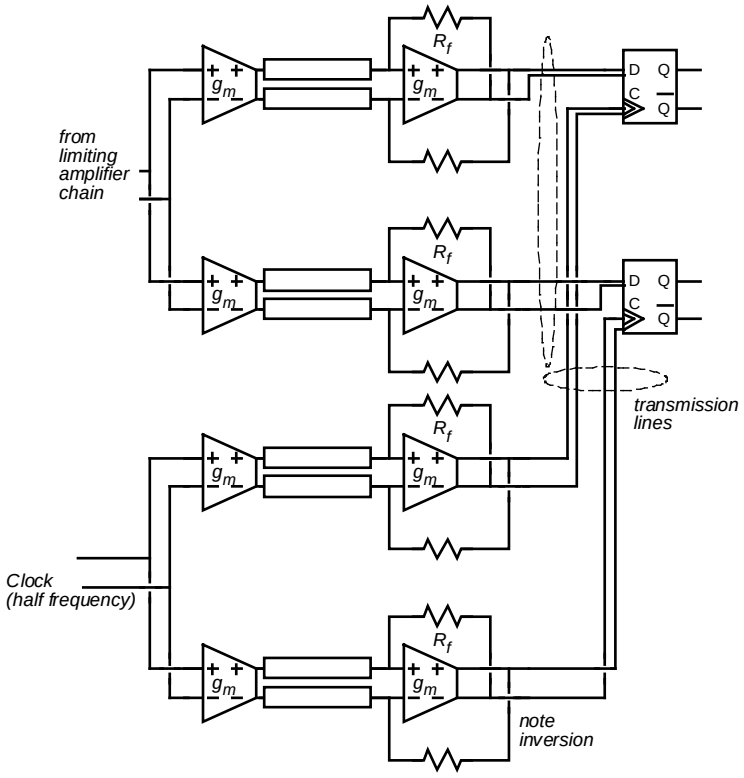


Figure 2: Optical fiber 2:1 demultiplexer, with PLL not shown.

The above two drawings show the optical receiver. It consists of a transimpedance amplifier, a limiting amplifier chain, and a 2:1 demultiplexer.

block diagram of an optical fiber receiver. The input from a photodiode is amplified by a transimpedance amplifier. A (usually) separate IC (shown above, right side of dotted line)

contains the clock and data recovery. The above figure shows the amplification and demultiplexing functions, but does not show how the relative phase of data and clock are measured.

In this diagram, short interconnects are indicated by simple lines, longer interconnects by transmission-line symbols. Clock and data are routed to a pair of master-slave latches, each operating at half the clock frequency. The 2 latches in combination sample alternating time slots of the data, recovering the data and demultiplexing the data to 1/2 the rate. Typical ICs use this structure in a 4:1 demultiplexing ratio.

You will be:

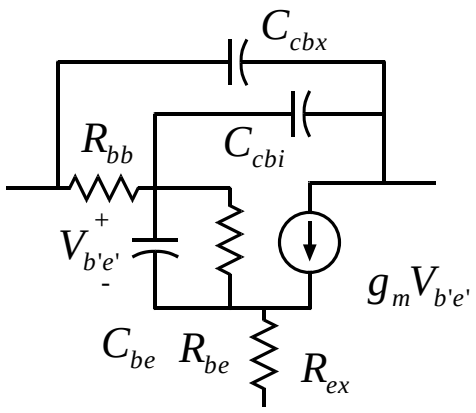
1) designing the latches and 2:1 demultiplexer ***INCLUDING*** performing mask layout and including layout parasitics.

2) designing the gm-Zt amplifier stages, including mask layout and layout inclusive of interconnects.

3) simulating the function of the full system, given the assumptions above.

Device Models

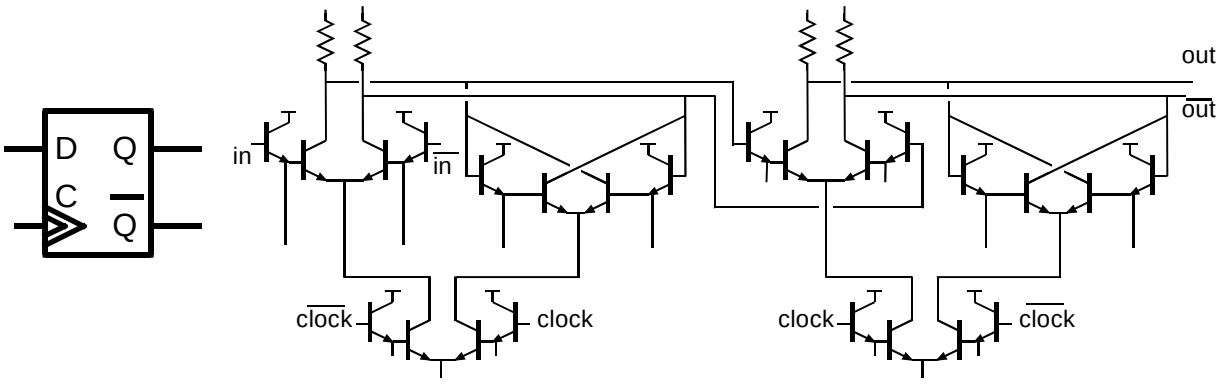
You will be using the large-signal (DC +AC) scalable HBT model covered in HW#2. A small signal equivalent of this is as below:



Recall that $C_{be} = C_{be,depl} + g_m \tau_f$. Cje=5.67 fF, beta=50, Ccbi=1.86 fF, Ccbx=1.34 fF, Rbb=14.7 Ohms, Rex=8 Ohms, and tau_f=0.244 ps. $g_m = qI / nKT$, where n=1.0. This is the model of a transistor having Ae=0.25 um x 4.0 um emitter area and biased at 1 mA/micron current density (4 mA total); the ft is 470 GHz ft and the fmax 825 GHz. It operates at a maximum of 2.5 mA/um at Vce=1.0 volts..

The SPICE model does not model the device Kirk effect, thermal failure, or breakdown. You must keep the current density below 10 mA/um^2, keep Vce below 2.5 V, and keep the dissipation below 20 mW/um^2 for all transistors.

DeMultiplexer Design



Above is shown the circuit diagram, missing bias sources, of a master slave latch. Designing the IC with 25 to 50 Ohm pull-up resistors, attempt to obtain the highest operational frequency feasible with the IC configured as a divide-by-two. Given that you are ignoring wiring parasitics, a well-designed latch in this technology should clock at about 200 GHz, perhaps a little higher.

Then, simulate and determine timing margins, as a function of clock rate. That is, put a random data stream into the D input. Clock C at the same rate. Vary the relative phases of

C and D to determine how long before/after the clock transitions the data must remain stable if correct operation is to be obtained.

Document these results clearly with circuit diagrams and simulation plots. Calculate by hand the delay time between a rising edge of clock (falling edge of clock bar) and the switching time at the collector node of the master latch. The inverse of twice this delay is the maximum clock frequency with the latch operating as a divider.

Simulate the pair of latches operating as a demultiplexer, e.g. with a 2-phase half-rate clock and data inputs. Determine the maximum rate of reliable operation. ***Warning: it is insufficient to verify that the output eye is clean. One must also check that the output data values are correct with a random data test.***

Be careful with the above circuit diagram and DC levels: First, the above circuit diagram is missing the diode level-shifter on the B-level emitter followers. You probably need to add these. Second, the output of a Cherry-Hooper, depending upon your design, may be at normal ECL levels or may be one diode drop more negative than this. If so, you may need to omit some of (but not all) the A-level emitter followers.

You must generate a mask layout of the master and slave latches. These will be used later in the full receiver mask layout. Once you have completed this mask layout, add the appropriate wire lengths to your schematic diagram.

Amplifier design .

Now, please design the amplifier system shown in the upper diagram. To keep the design task tractable, it is highly advisable to use nearly the same design and mask layout for all transimpedance blocks and all transimpedance blocks. You can use more or less stages than the diagram indicates. You do need the final 2:1 fan-out as illustrated.

The amplifier is to be designed for the highest feasible bit rate, with the stipulation that ***the eye must be >85% open in both voltage and in time*** under either small signal or large signal input. This rate is likely to be 140 Gb/s or larger, given the transistors available.

An SNR analysis at 160 Gb/s suggests optical receiver sensitivity around e.g. -10 dBm, e.g. 100 uA peak-peak photocurrent. Given this, and a TIA transimpedance of 50 Ohms, the minimum peak-peak input to the CDR IC is 5 mV. With a shorter optical link, the input signal will be stronger, and the CDR must also operate correctly with 300 mVpp input.

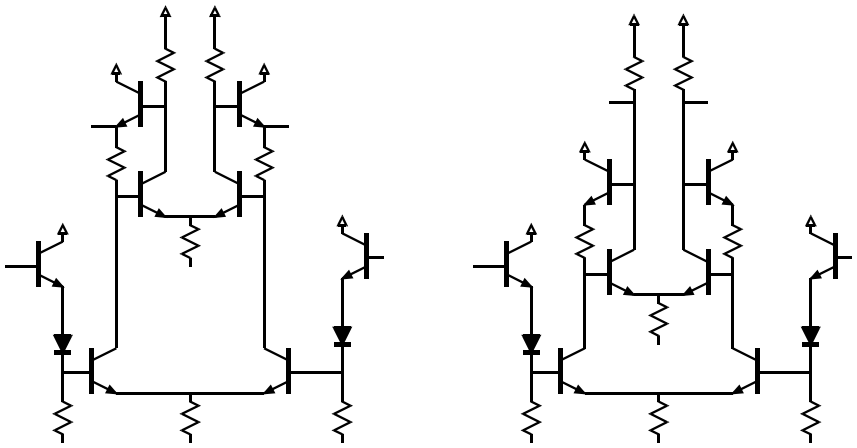
Your have earlier simulated the latch ICs. These will need 100 mVpp and perhaps 250 mVpp in order to function at full speed. Thus we have specified the required gain.

Initial Circuit Design

The amplifier is to be driven with a 50 Ohm impedance generator. The inputs are to be set at whatever DC level you prefer---it simplifies design to make this the same as the DC output level of subsequent stages. The undriven input is set at a similar DC bias.

In real systems, this DC level is adjusted by an operational amplifier so that the output differential DC level of the amplifier is zero. This is done by a slow feedback loop so as to not remove low frequency signal components. You will emulate this function in your circuit by emulating the operational amplifier with an ideal voltage-controlled voltage source (VCVS) in ADS.

. The load for the amplifiers is infinite. It would be best to load the amplifiers with an (unclocked) latch input to correctly simulate its bandwidth.



The figure above shows a couple of suggested designs. You need to think about the DC levels at the input and output of each stage (keeping them consistent), and the required input DC levels of the latches. For example, if you use outputs wired as on the left, the outputs are at least V_{be} below ground, and the latch should therefore not use emitter follower buffers on its input.

With this information, design the amplifier for the desired gain and DC levels. Simulate for bandwidth---you should run both transient and AC small signal voltage gain simulations--and design to obtain the highest feasible bit rate of operation, with the specification being >85% eye closure for either small signal or large-signal inputs.

Try to perform a first order (a1) time constant analysis of one stage and try to correlate this with your simulations.

Mask layout--and Resimulation

To keep this tractable, it is essential to keep the designs of all stages identical or nearly so, and to use a highly hierarchical layout.

You must generate a mask layout of the full receiver. From the physical layout, you must add the interconnect wire lengths back into the circuit schematic so that these are included in the simulation. Do this using the multilayer model available in ADS.

Once you add these wiring parasitics, you must resimulate all aspects of receiver performance.

Full simulation.
After adjusting the clock timing appropriately, simulate the full system and document clearly the highest feasible data rate of operation.