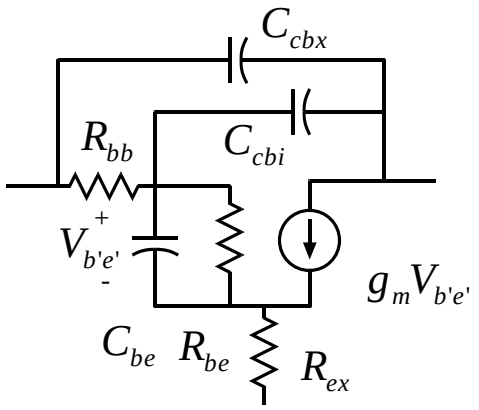
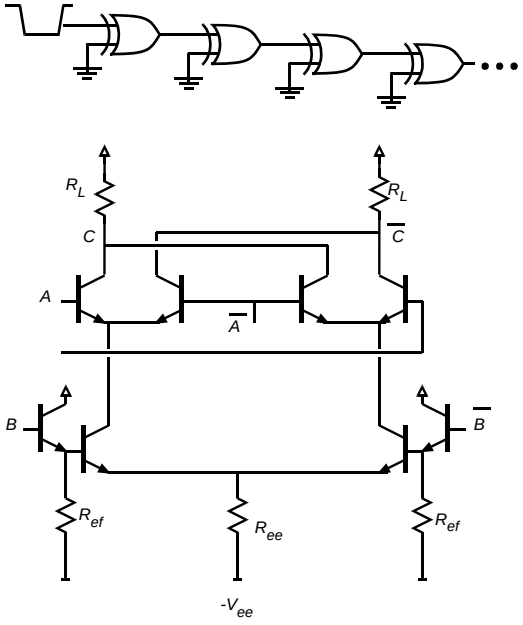


This is the hand analysis model; please use the HBT_scalable model in ADS for circuit simulations.

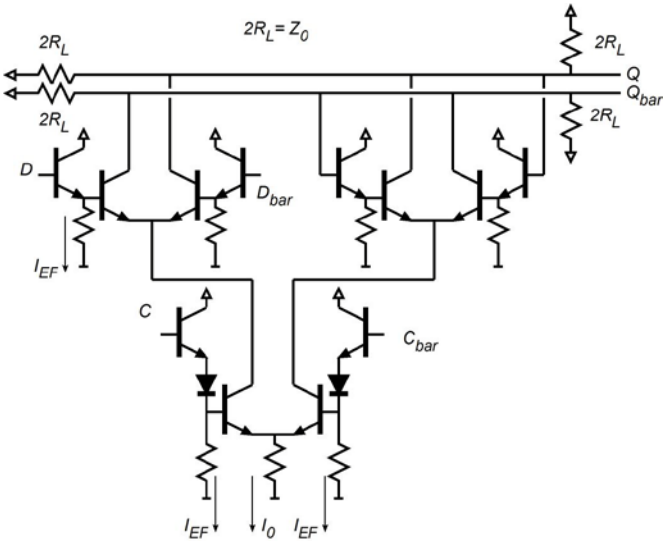


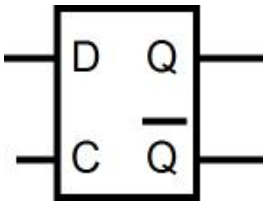
ECE194JC/594J PS4 Above is a device model . Recall that $C_{be} = C_{be,depl} + g_m \tau_f$. Let us take Cje=5.67 fF, beta=50, Ccbi=1.86 fF, Ccbx=1.34 fF, Rbb=14.7 Ohms, Rex=8 Ohms, and tau_f=0.244 ps. Lets use this device model in circuit calculations below. $g_m = qI / nKT$, where n=1.0. This is the model of a transistor having Ae=0.25 um x 4.0 um emitter area and biased at 1 mA/micron current density (4 mA total); the ft is 470 GHz ft and the fmax 825 GHz. It operates at a maximum of 2.5 mA/um at Vce=1.0 volts. Unlike previous problem sets, ***do not*** move all the collector-base capacitance inside Rbb.

Problem 1: Please find the A-level propagation delay of a CML XOR gate. The circuit diagram is the lower figure: the pull up resistors are 50 Ohm, while the resistors are to act as current sources carrying 6 mA each. Use the device model above, emitter length and device parameters scaled so that the transistors operate at 2 mA/um when turned on. The signal is propagated between successive gates on the A-Level input. a) Using MOTC analysis, compute the propagation delay per gate. Note that the expression will differ from those in class, due to the extra set of Ccb's connected to the output node. b) Simulate using ADS and compare with your hand analysis. You should see reasonable correlation.

Problem 2: Below is shown an ECL latch. Assume 2RL=Z0=50 Ohms. Choose the emitter bias resistors so that all $I_{EF} = I_0$=12 mA, choose differential pair transistor emitter junction lengths so that transistors operate at 2 mA/micron when on, and choose emitter follower transistor emitter junction lengths so that transistors operate at 2 mA/micron under DC bias.

figure (a)





A *master-slave latch* is produced by simply cascading a pair of such latches, but with inverted sign for the clock signal on the second stage:

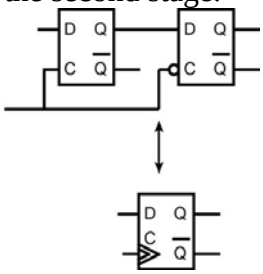
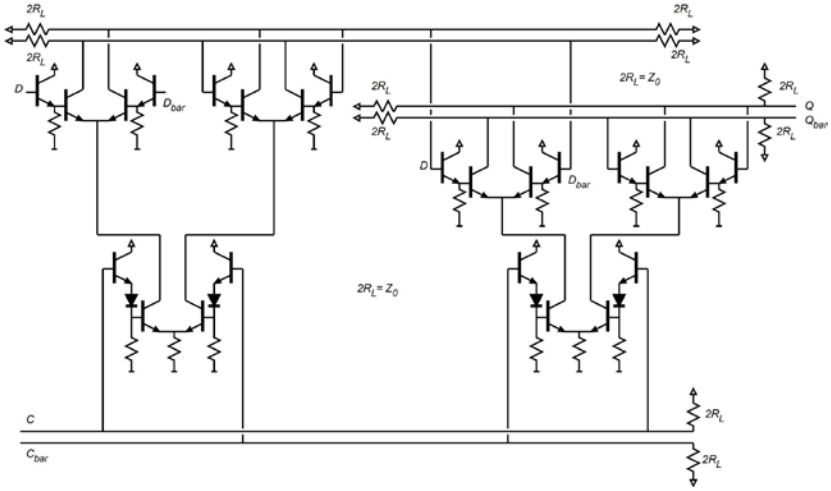


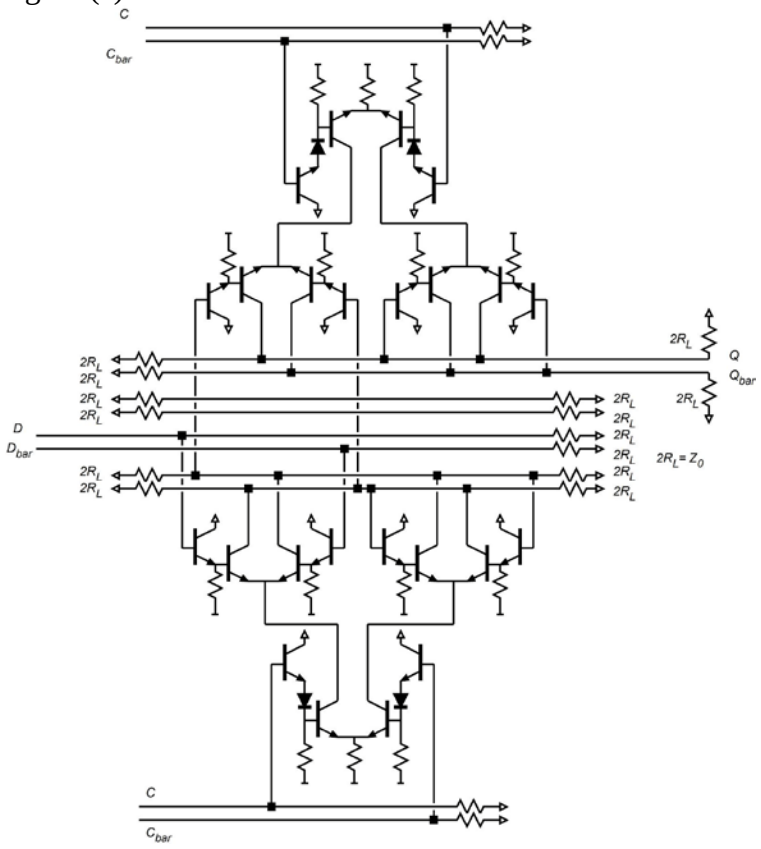
figure (b)



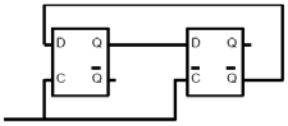
Another topology for layout for this would be as shown to the right. In this layout routing of signal lines at input and output can be made very tight for fast operation. Clock routing is more difficult, as separate drive is necessary for both the upper and lower circuit halves. This can be done using split drivers, or braching a 50 Ohm clock lines into two 25 Ohm clock lines each terminated in 25 Ohms.

Think carefully about the resistor values necessary for reflection-free termination of all lines.

figure (c)

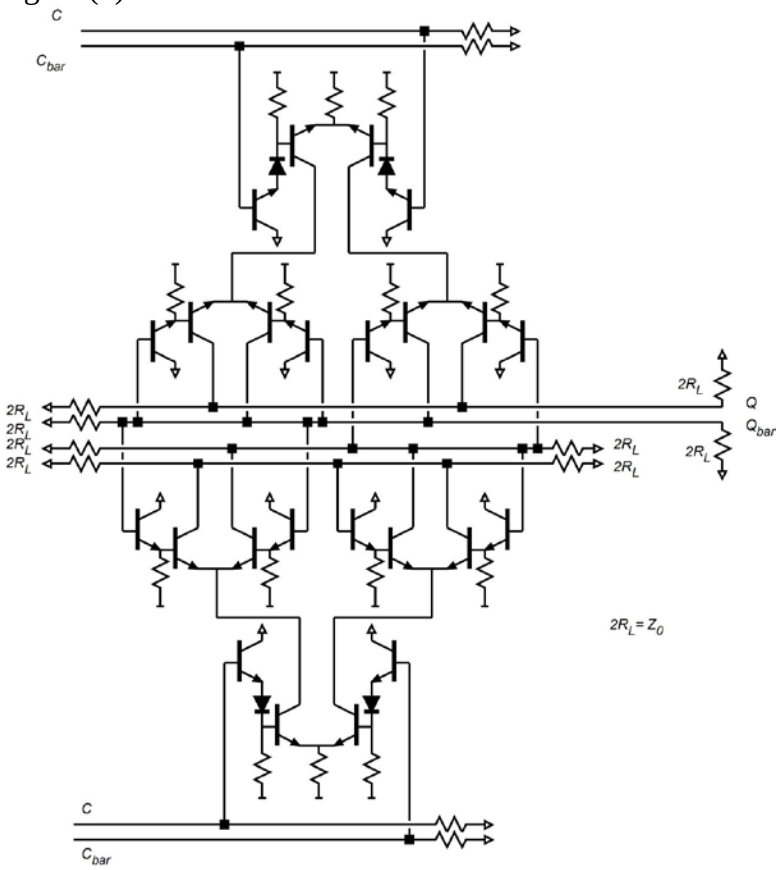


A 2:1 static frequency divider is made by connecting the inverting output of the master-slave latch back to its input.



Its mask layout is shown to the right

figure (d)



Please do the following:

(problem 2a) Taking the circuit of figure (a), calculate the delay between a rising edge of clock and a transition in the output state.

(problem 2b) simulate this in ADS and compare your hand result with computer simulation. In this simulation, use the (provided) random data sequence on the data and data bar inputs, and a square wave on clock. The clock rate in Hz should be equal to the data rate in bits/second.

(problem 2c) Generate an IC mask layout for the master-slave latch (figure c layout style). Generate a corresponding IC simulation file which includes layout parasitics. Again simulate with random data on the latch inputs and with square waves on the clock inputs. The clock rate in Hz should again be equal to the data rate in bits/second. Checking the latch outputs carefully for bit errors, determine the maximum clock frequency.

Hint: as with the previous problem set, heavy use of a design heirarchy is key to efficient use of your time in both laying out the mask design and in generating the circuit schematic for simulation. Figure (c) contains a four-fold symmetry.