ECE ECE145C (undergrad) and ECE218c (graduate)

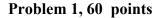
Final-Exam. Dec 13, 2002

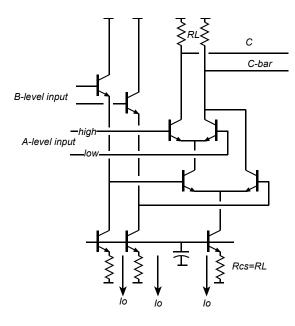
Do not open exam until instructed to.

Open book

Use any and all reasonable approximations (5% accuracy is fine.), *AFTER STATING THEM*.

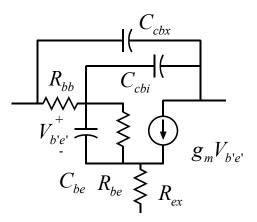
Name: _____





You will be working on the circuit below, a CML inverter

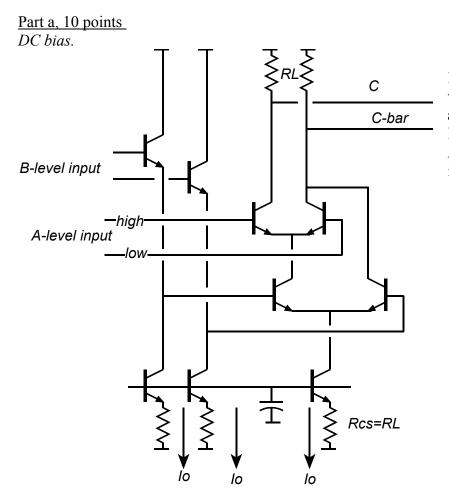
The circuits all use 3 um² transistors. Io is 3 mA in all cases. RL=Rcs=100 Ohms. The negative supply is -3.3 volts



To the left is a hbt small-signal device model . Recall that $C_{be} = C_{je} + g_m \tau_f$. Let us take Cje=Cbe,depl=20 fF, beta=infinity, Ccbi=3 fF, Ccbx=2 fF, Rbb=50 Ohms, Rex=5 Ohms, and tau_f=0.5 ps. The transistor, has 3 um^2 emitter area

For large-signal analysis, we will take Ccbx, Ccbi, and Cbe,depl as having no variation with bias voltage.

Vbe=0.7 volts at 1 mA/um² current density



Indicate the DC bias voltages on each node, assuming correct logical values on the A-level and B-level inputs. Part b, 20 points gate delay analysis.

For simplicity in analysis, *for the current-mirror transistors ONLY*, assume Rbb=0 Ohms.

Please calculate the *B-level* propagation delays, per gate, on an infinite string of gates. There is a slight difference in delay to the C and C_bar outputs; calculate the delay to C, not C_bar

Note that the current source capacitance has some effect.

Please show all your work, including

--the switching signal path circuit diagram will all relevant transistor parasitics indicated.

--calculation of A1...algebraic expression ...and numerical evaluation

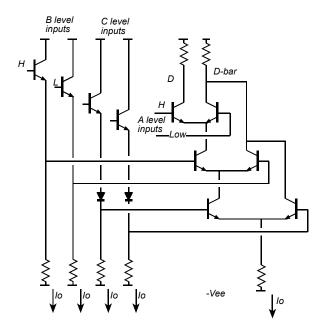
--calculation of B1...algebraic expression ...and numerical evaluation

--the resulting gate propagation delay.....numerical value only

Part c, 30 points gate delay analysis.

If we wanted to form the function $D = A \cdot B \cdot C$ we have 2 choices. One is to use a cascaded pair of gates, each of which as is shown in part b, with the first gate forming $E = A \cdot B$ and then driving the second gate, which forms $D = E \cdot C$. This could result, worst-case, in a total propagation delay of 2 B-level delays, such as is calculated in part b above.

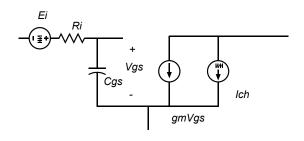
The alternative is to use a 3-level series gated circuit. The supply voltage is now -4 volts. Ignore the loading of the pull-down resistors. Calculate the delay from the C-level inputs to the D output, using all the steps as outlined in part b. *Note very carefully, the H/L (high-low) assignments on the B-level and A-level inputs.* How does the delay compare to twice the delay of the gate of part B ?

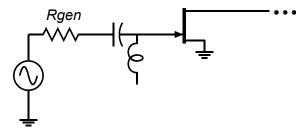


Problem 2, 40 points

noise analysis

Part a, 20 points



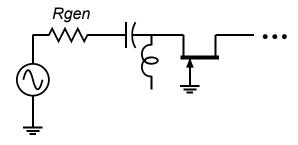


A FET has noise model as shown here. Ri=20 Ohms, gm=100 mS. The transistor ft is 200 GHz. Ich is the drain noise spectral density...the channel noise parameter Gamma is 1.5

The inductor and capacitor are both infinite (a bias T, to simplify the problem). Rgen is 50 Ohms.

Calculate (1) the total input-referred noise voltage, in V^2/Hz and (2) the noise figure

Part b, 20 points



Again we use a bias T. The inductor and capacitor are both infinite (a bias T, to simplify the problem). Rgen is again 50 Ohms.

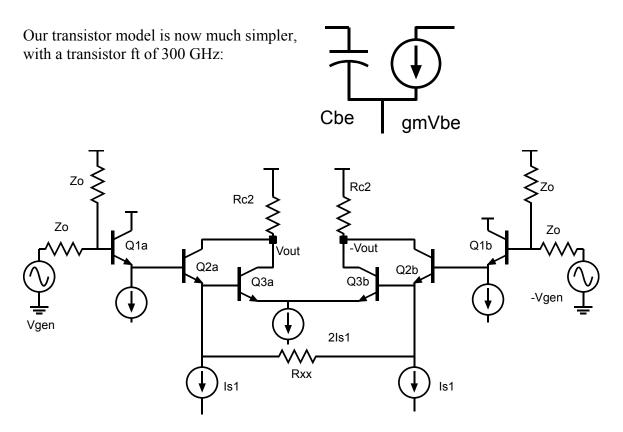
Again calculate (1) the total input-referred noise voltage, in V^2/Hz and (2) the noise figure

Part e, xx points

Please make a *quantitative* bode plot of the transfer function (label both axes, draw pole frequencies in the right places, and slopes correctly)

		_	_					_	П				-		П		_	_				_		_		П	
					Ħ				IT															1		Π	
			+		╫			+					-					+						+		H	
		\rightarrow	_	\square	11			_					_	11	11			_		_				_		\square	
					Ħ																					Ħ	
			+	\parallel	╫			+	+		 -		+		+			+	+			+		+	+	+	++
		_	-	\square	╢			+			 <u> </u>	_	+					_	_	_		_		-			
			+		Ħ			+	Ħ									+						+		Ħ	
		-	-		+			+					+					+						+		+	
					Ш			_	\square						\parallel			_						_		\square	
					Ħ																					Π	
		+	+	\square	$^{++}$		+	+	\square				+		+			+		\vdash		-		+	-	\parallel	
				\square	11				\square					\square				\downarrow						\downarrow		\parallel	\square
				Ħ	T			T	Ħ					Π					Τ							Π	
 I			_		11	I				Ц	I				11						LI		_				\square

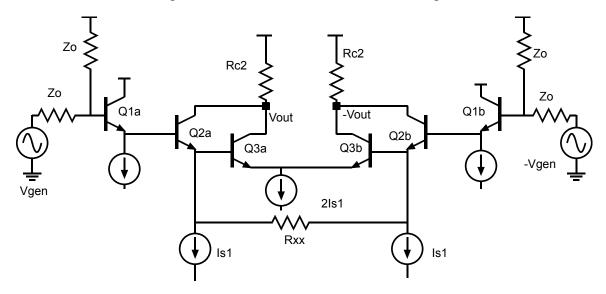
Problem 2, xx points



The circuit has all transistors biased at 1 mA each. Rxx is 52 Ohms. Rc2 has a 300 mV DC drop across it.

Part a, xx points DC bias

Draw all DC node voltages and branch currents on the circuit diagram below



Part b, xx points AC midband analysis

Find the differential voltage gain of the circuit, which we will here define as *** $2 \cdot (V_{out} / V_{gen})$, where Vout is the AC voltage at the collector of Q3a.

Part c, xx points *High frequency analysis*

Using the method of your choice, find the first 2 poles of the transfer function (if complex, find the natural resonance frequency and the damping factor).