Mixed-Signal IC Design Notes set 1:

Quick Summary of Device Models

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Background / Review

This material was covered in ECE145A

Quickly review key information.

Transistor models

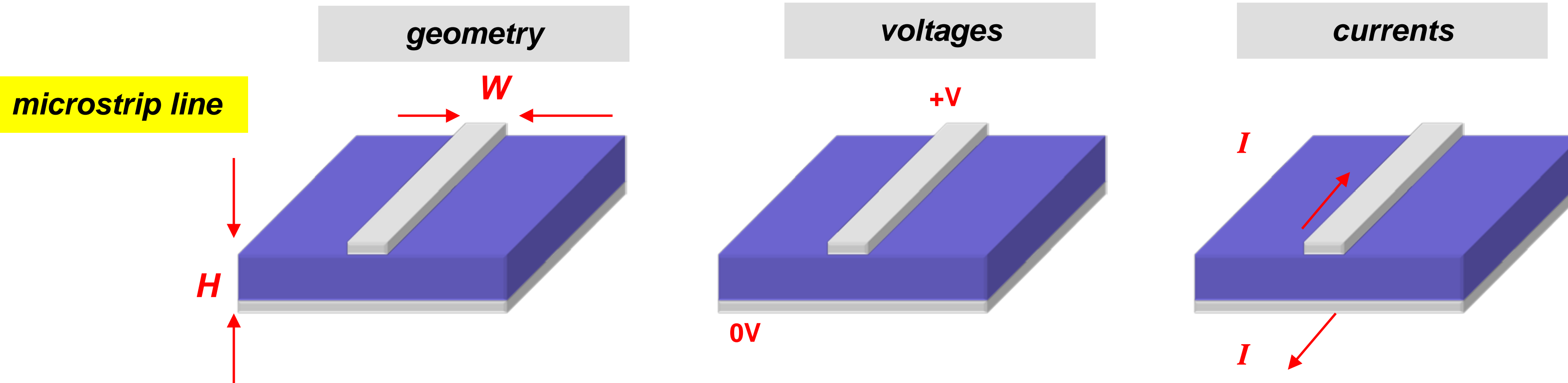
Interconnect models

2 - port parameters

If greater detail is required, please refer to the ECE145a online notes.

Transmission Lines

Transmission Lines for On-Wafer Wiring



characteristic impedance : $Z_o \cong \frac{\eta_0}{\sqrt{\varepsilon_r}} \frac{H}{H+W}$

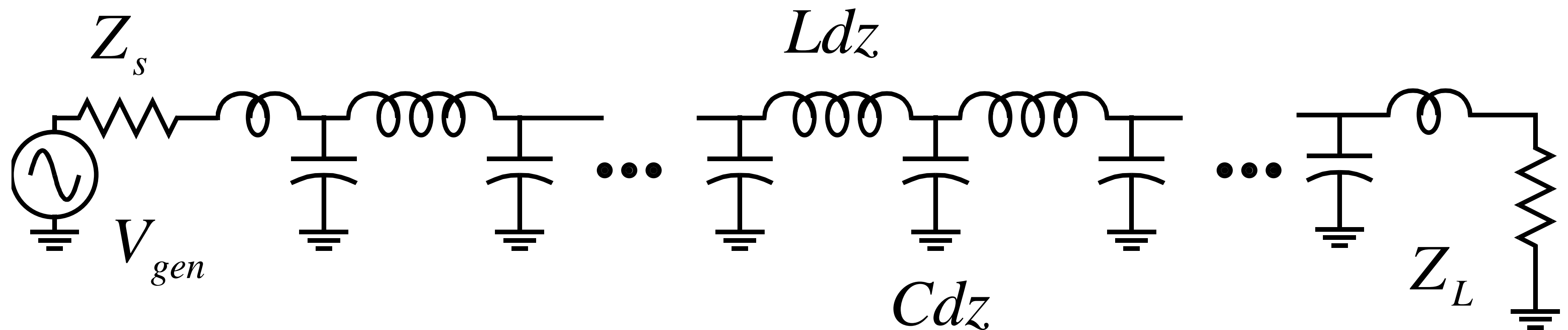
where $\eta_0 \approx 377\Omega$ and

propagation velocity : $v = \frac{c}{\sqrt{\varepsilon_r}}$

where c is the speed of light.

These are approximate relationships : learn how to use ADS

Transmission Lines: Waves, Voltage, Current



$V(z,t) = V^+(t - z/v) + V^-(t + z/v)$ forward and reverse wave voltages

$I(z,t) = \dfrac{V^+(t - z/v)}{Z_o} - \dfrac{V^-(t + z/v)}{Z_o}$ forward and reverse wave currents

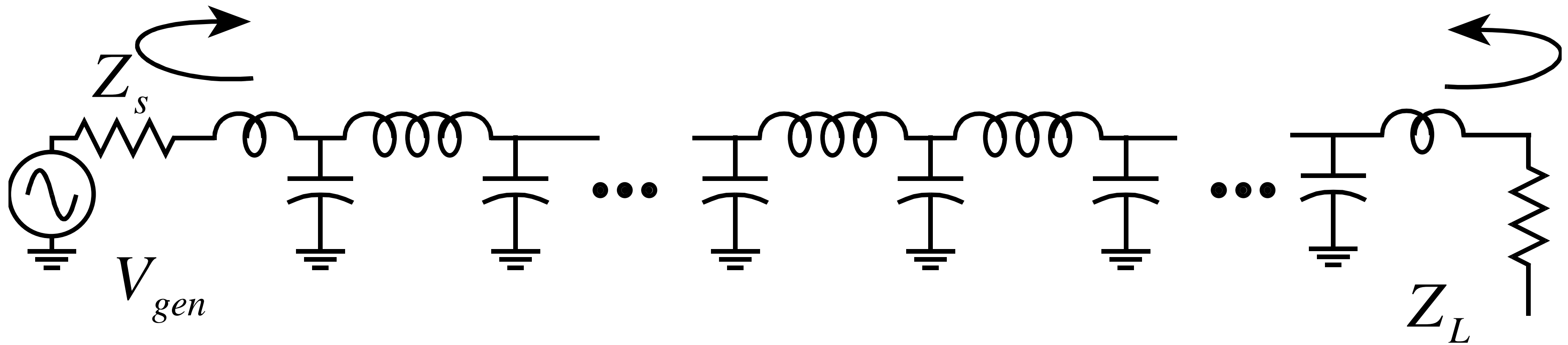
where

$Z_o = \sqrt{L/C}$ characteristic impedance

and

$v = 1/\sqrt{LC}$ propagation velocity

Reflections



At end of line:

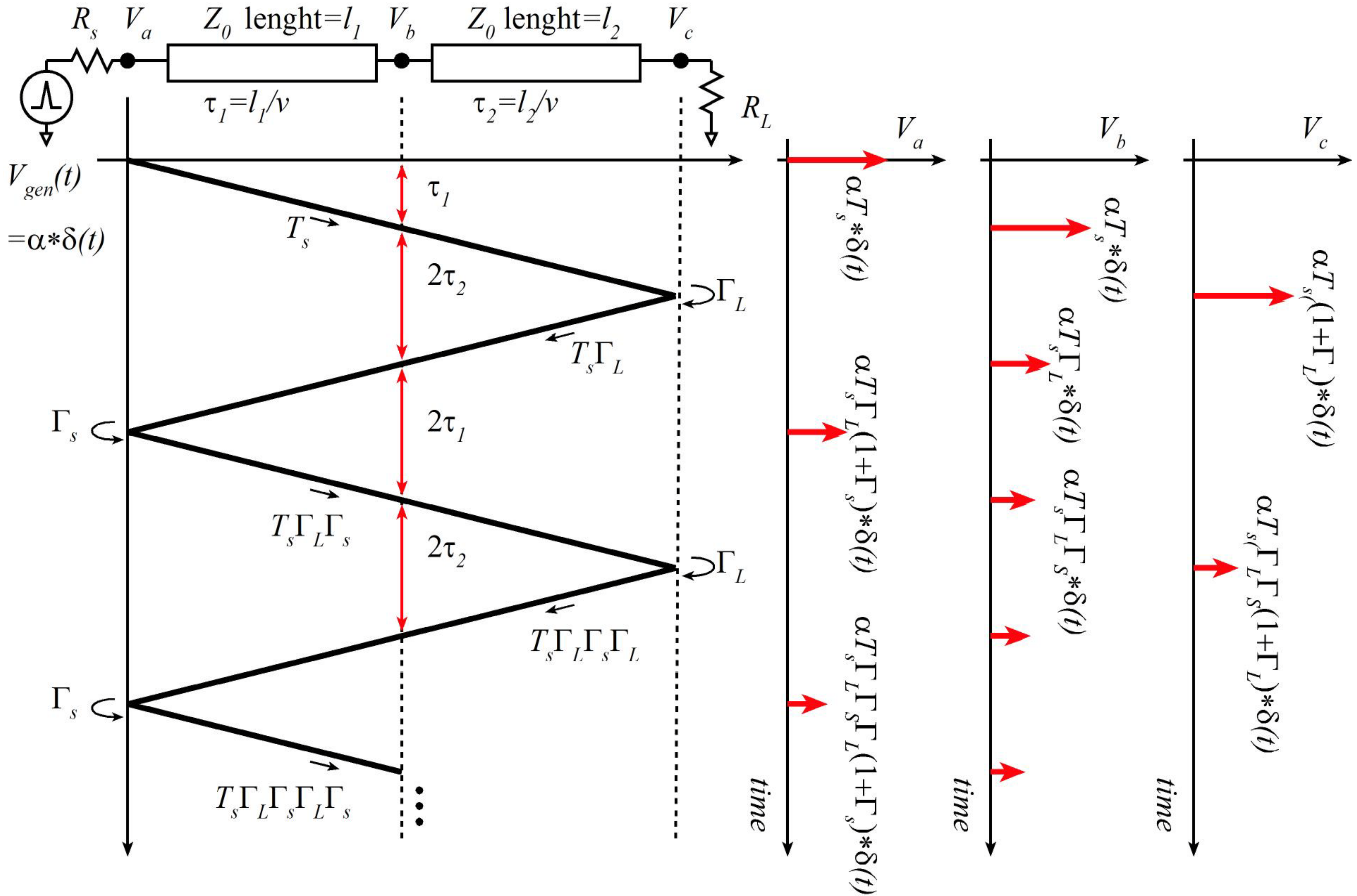
$$V^- = \Gamma_l V^+ \quad \text{where } \Gamma_l = \frac{(Z_l/Z_o)-1}{(Z_l/Z_o)+1} \text{ load reflection coefficient}$$

At beginning of line:

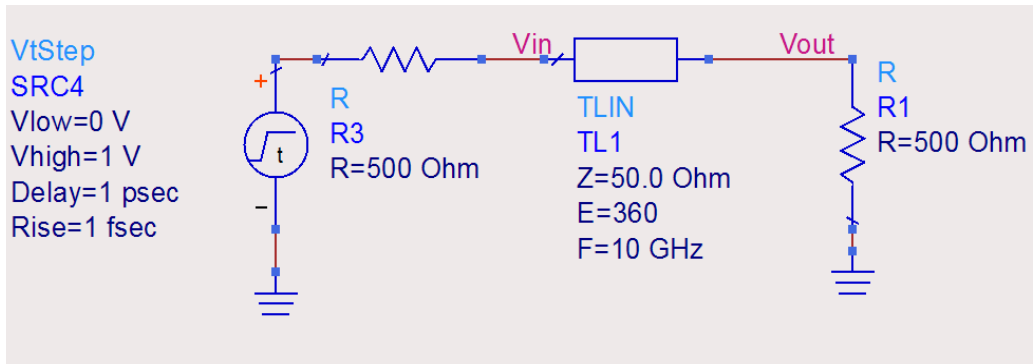
$$V^+ = \Gamma_s V^- + T_s V_{gen} \quad \text{where } \Gamma_s = \frac{(Z_s/Z_o)-1}{(Z_s/Z_o)+1} \text{ source reflection coefficient}$$

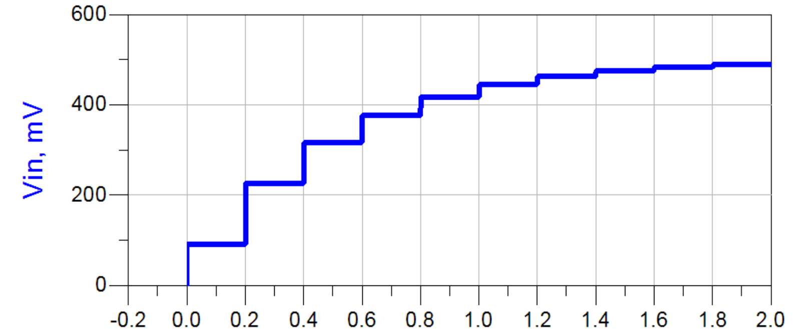
$$\text{and } T_s = \frac{Z_o}{Z_o + Z_s} \text{ source transmission coefficient}$$

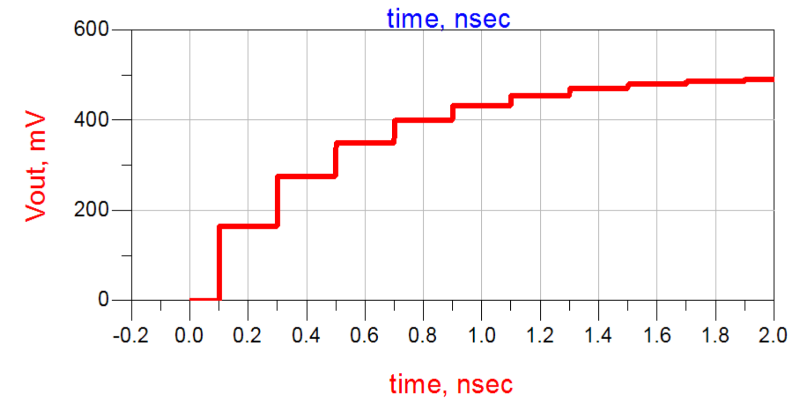
Pulse Reflections on Transmission Lines



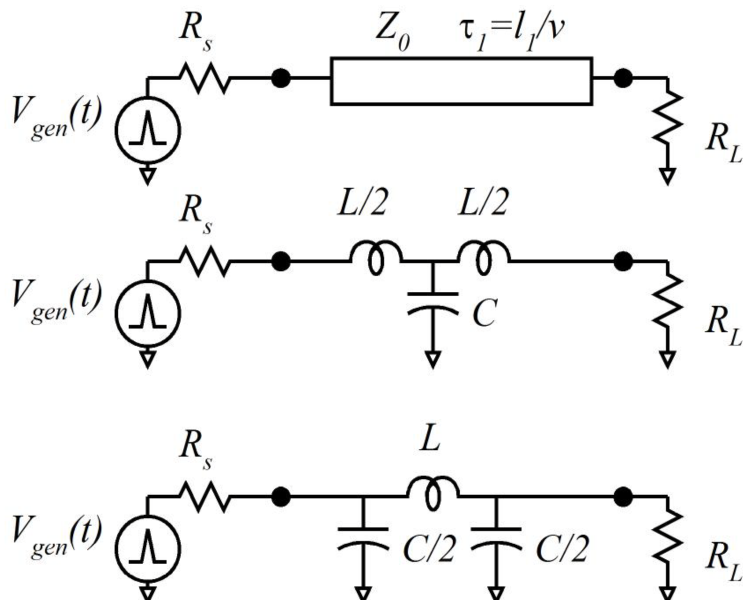
Relating Lumped and Distributed Circuits



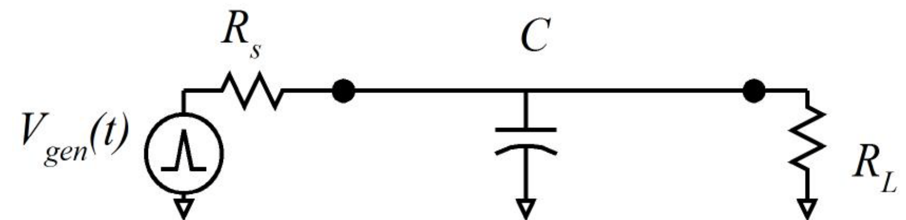




$$L = Z_0\tau \, , C = \tau / Z_0$$



Approximate model



$$L/(R_L + R_s) << (R_L \,||\, R_s)C$$

$\rightarrow$ neglect inductor

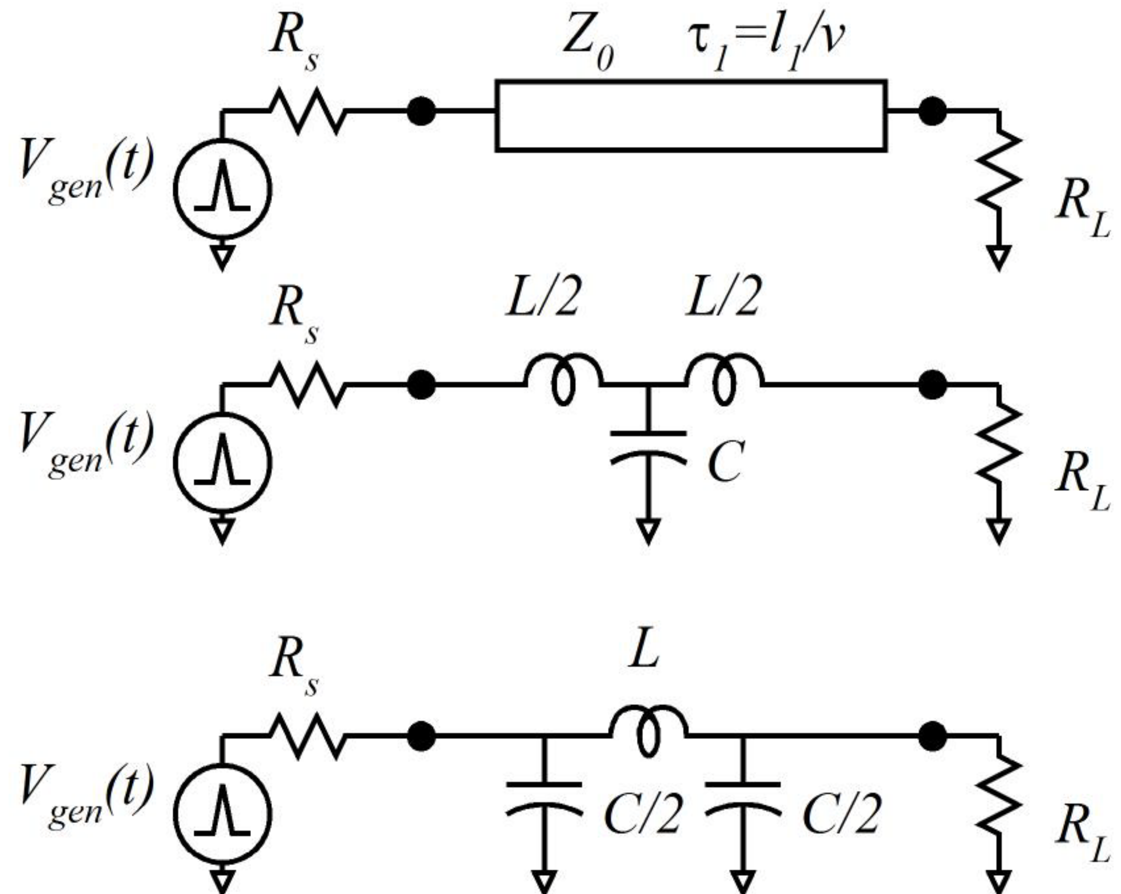
RC circuit $\rightarrow$ charging.

Short Tramission Lines Can Be Modeled as L's and C's

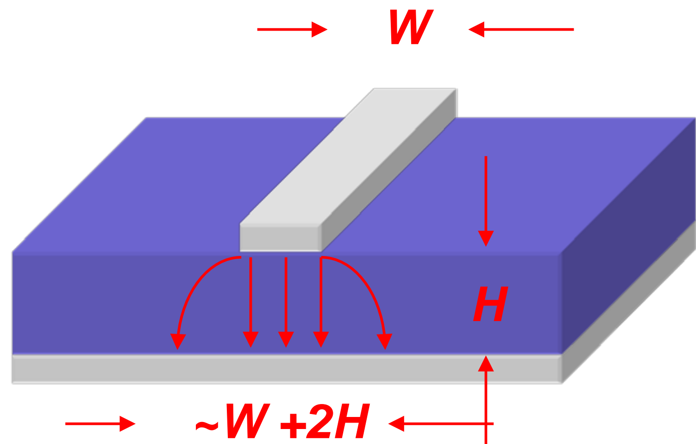
$L = Z_0 \tau \; , C = \tau / Z_0$

High - Z_0 line :
large L, small C.
$\rightarrow$ approximately
an inductor

Low - Z_0 line :
large C, small L.
$\rightarrow$ approximately
a capacitor.



Skin effect loss



Current penetrates the conductor by one skin depth

$$\delta = \sqrt{\omega\mu\sigma/2}$$

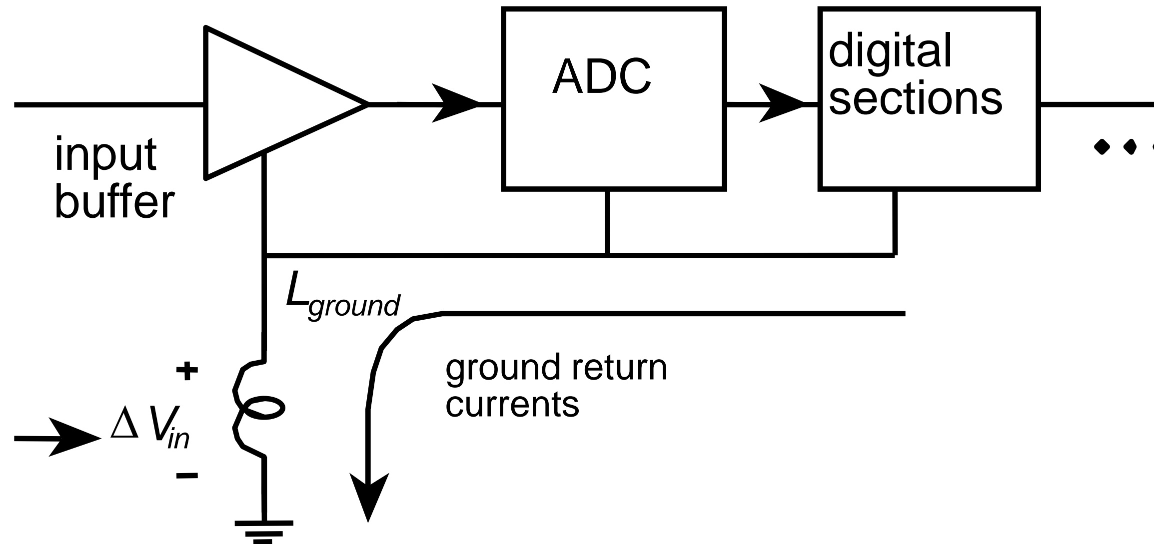
where σ is the conductivity.

Line has added series resistance per unit length

$$Z_{surface} = \frac{1}{P}\frac{(1+j)}{\delta\sigma}, \text{ where P is the effective current - carrying periphery.}$$

package resonance and grounding

What is Ground Bounce ?



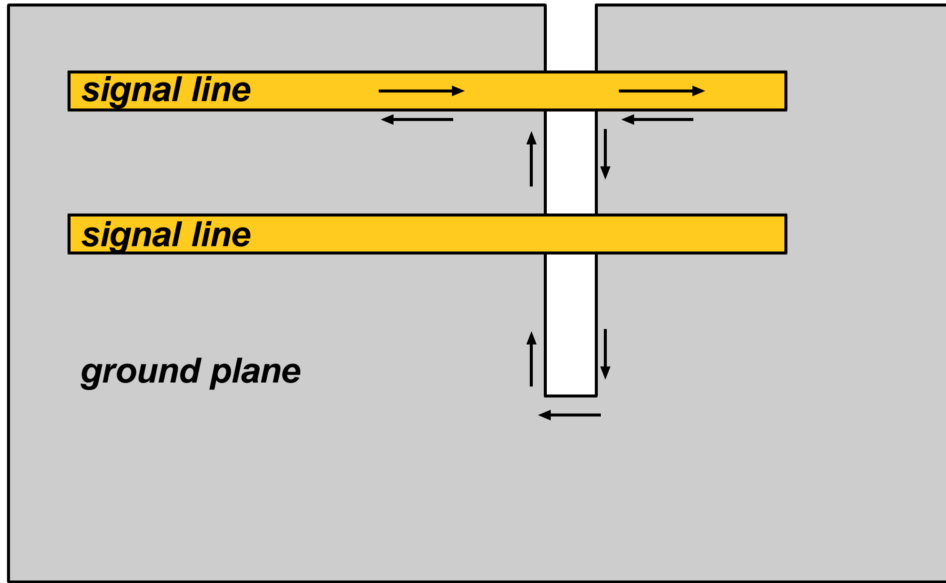
ground bounce noise

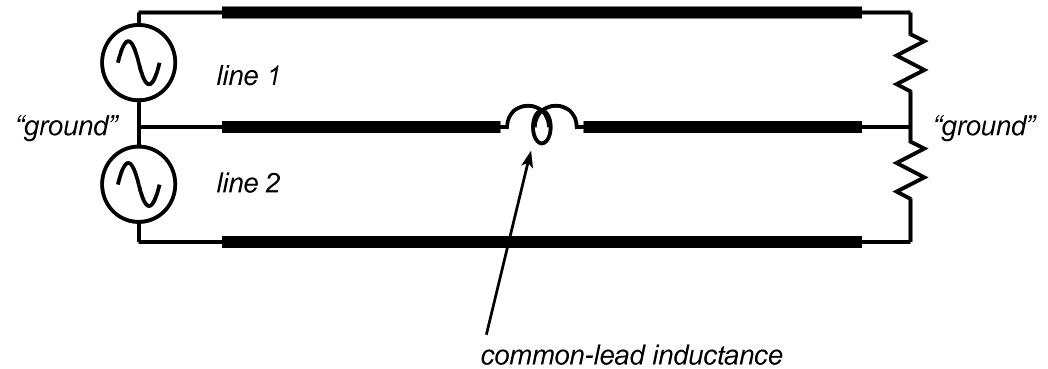
"Ground" simply means a reference potential shared between many circuit paths.

To the extent that it has nonzero impedance, circuits will couple in unexpected ways

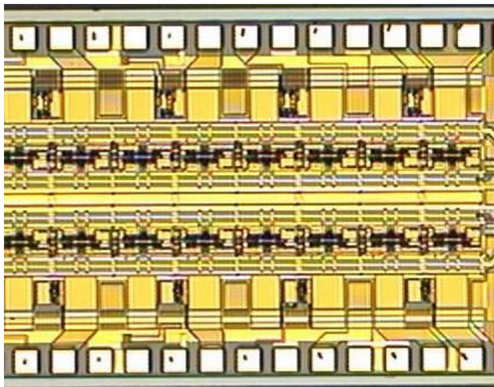
RFI, resonance, oscillation, frequently result from poor ground systems

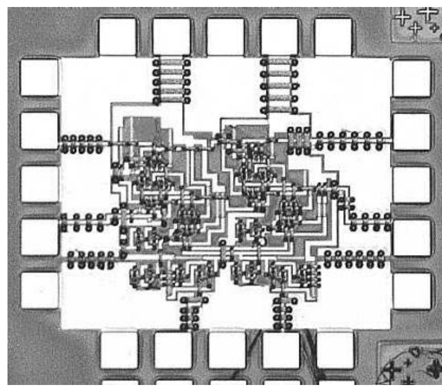
Ground Bounce on an IC: break in a ground plane

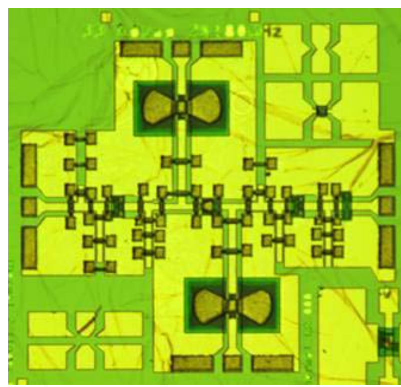




coupling / EMI due to poor ground system integrity is common in high-frequency systems
whether on PC boards
...or on ICs.



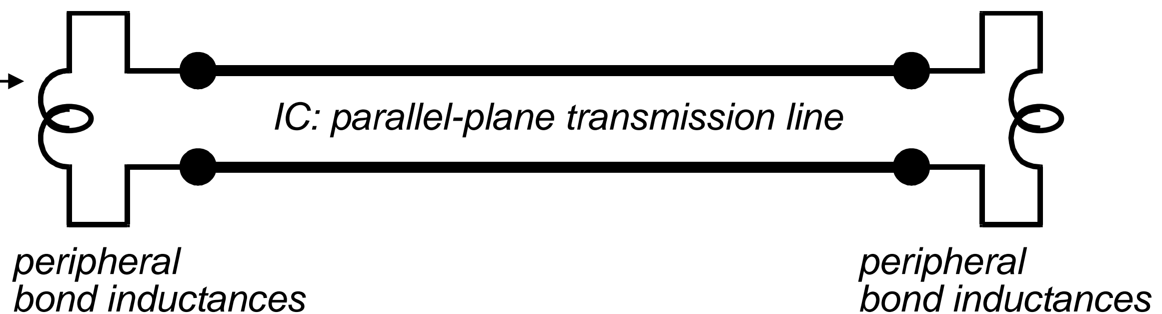




Ground Bounce: IC Packaging with Top-Surface-Only Ground

Peripheral grounding allows parallel plate mode resonance
die dimensions must be <0.4mm at 100GHz

Bond wire inductance aggravates the effect: resonates with through-wafer capacitance at 5-20 GHz

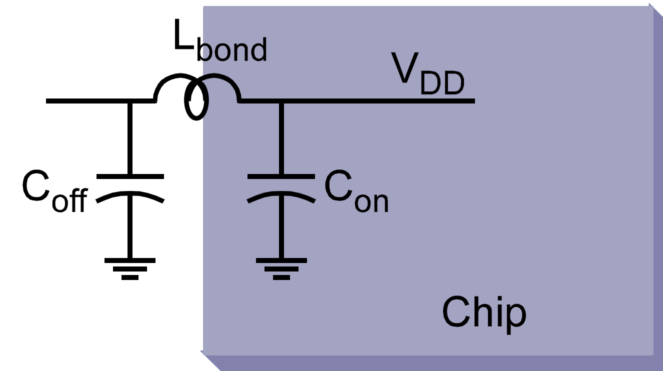


power-supply resonance

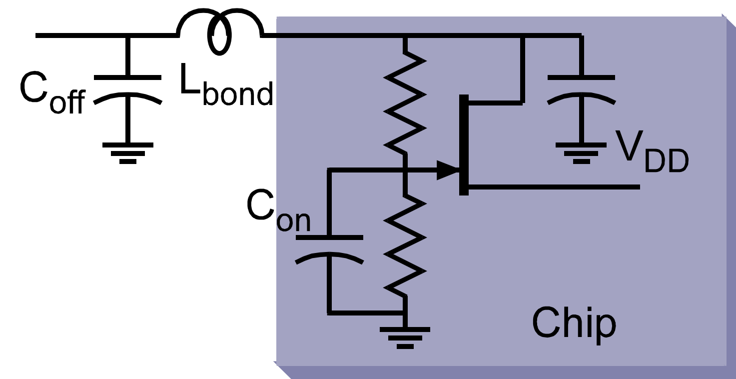
Power Supply Resonance

Resonates at $f = 1/2\pi\sqrt{L_{bond}C_{on}}$

gain peak / suckout, oscillation, etc.



Active (AC) supply regulation

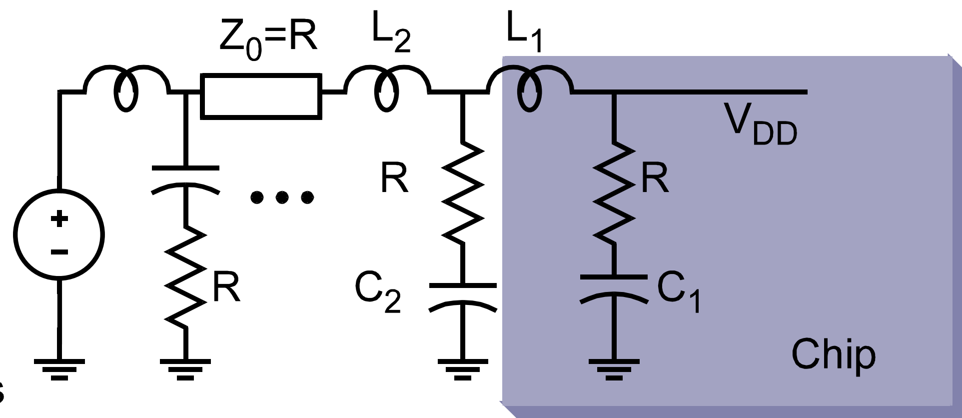


Passive filter synthesis

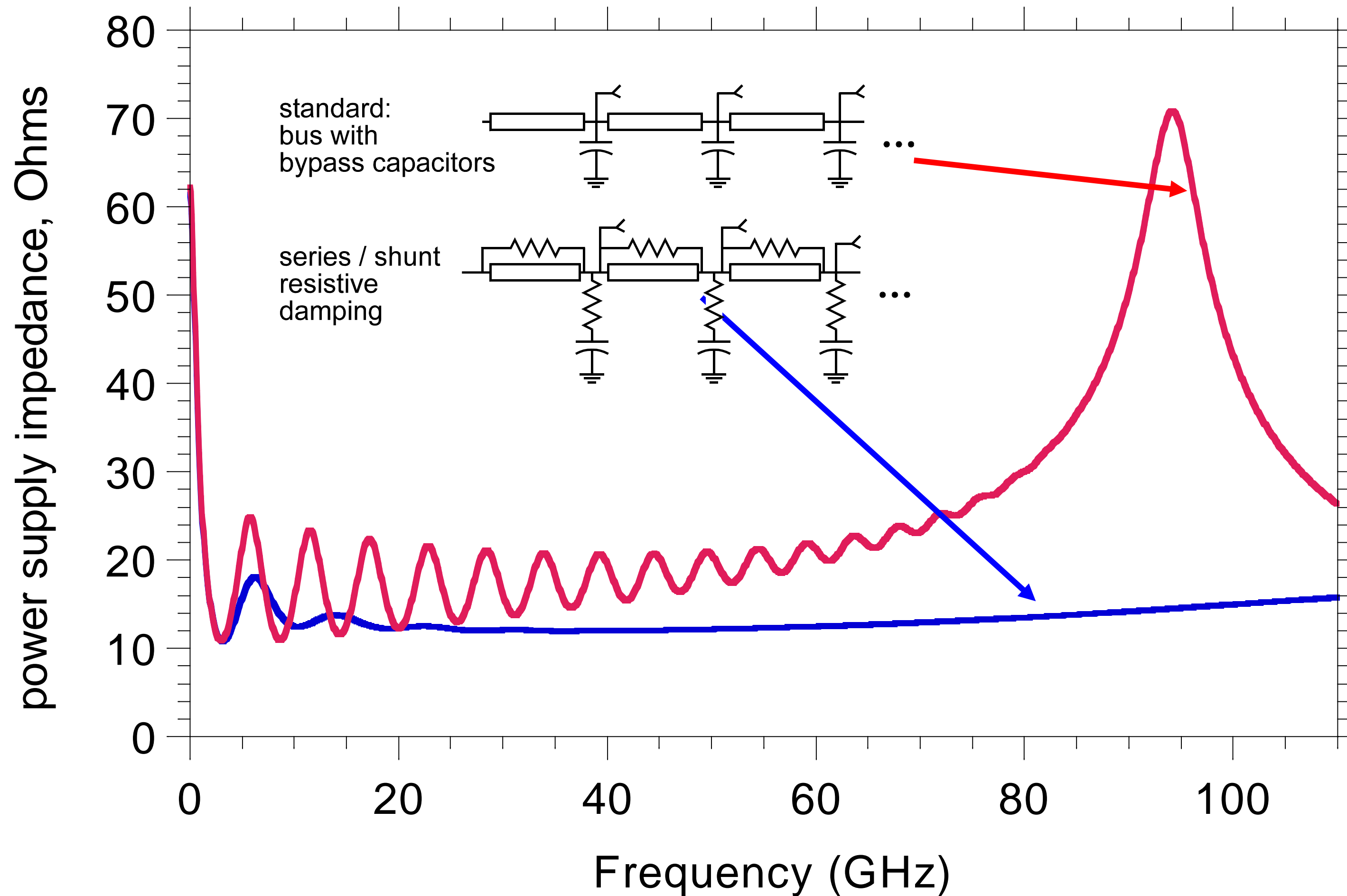
$$R = \sqrt{L_1/C_1}$$

$$\sqrt{L_1/C_1} = \sqrt{L_2/C_2} = \bullet\bullet\bullet$$

supply impedance is R at all frequencies



Power Supply Resonances; Power Supply Damping

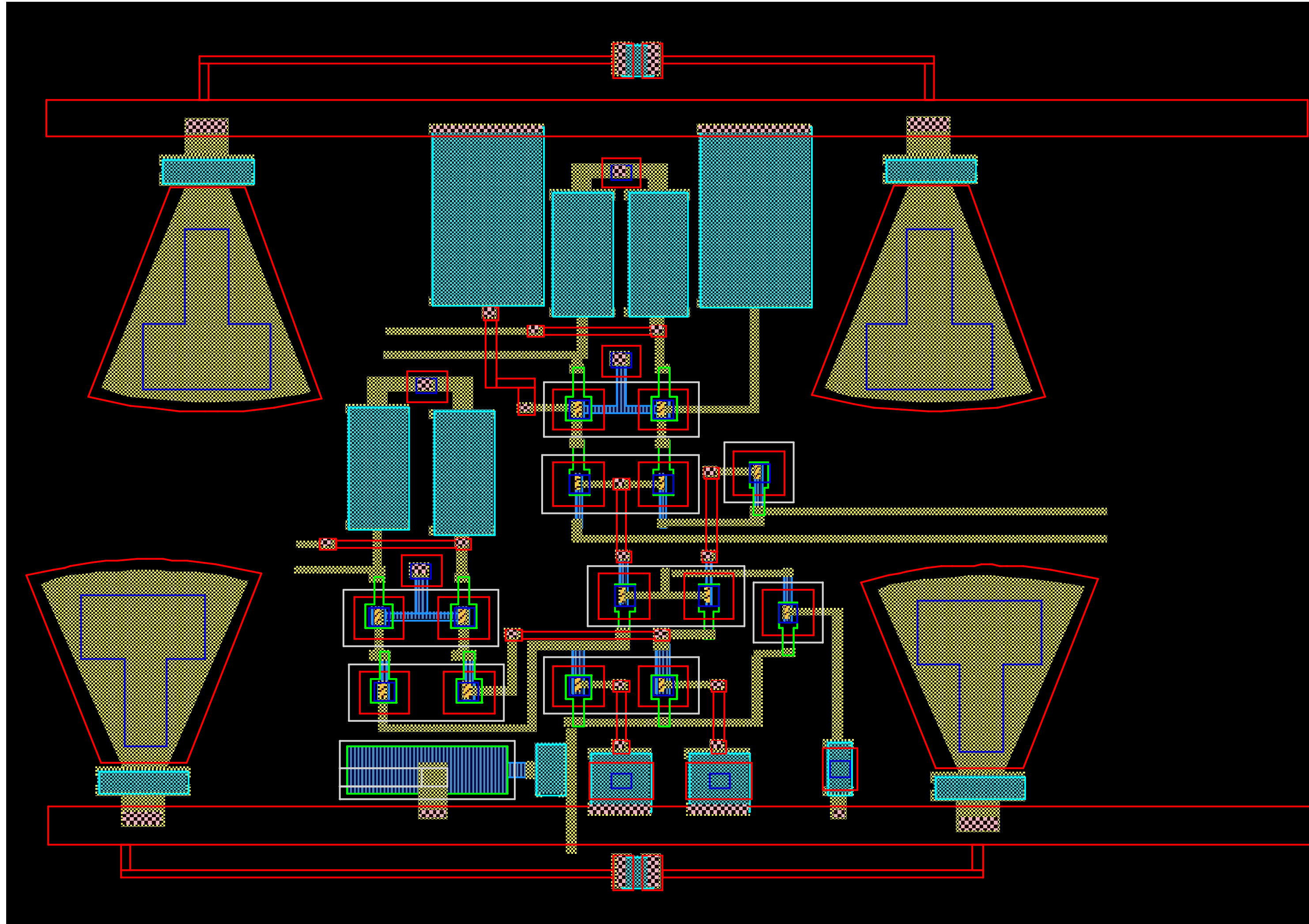


90 GHz--local resonance between power supply capacitance and supply lead inductance

*~N*5GHz resonances--global standing wave on power supply bus*

Power supply is certain to resonate: we must model, simulate, and add dampling during design.

Standard cell showing power buses



Interconnects: Summary, Design Strategy

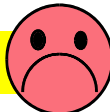
IC Interconnects -- Thin-Film Microstrip

narrow line spacing → IC density

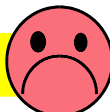
no substrate radiation, no substrate losses

fewer breaks in ground plane than CPW

... but ground breaks at device placements

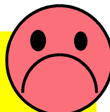


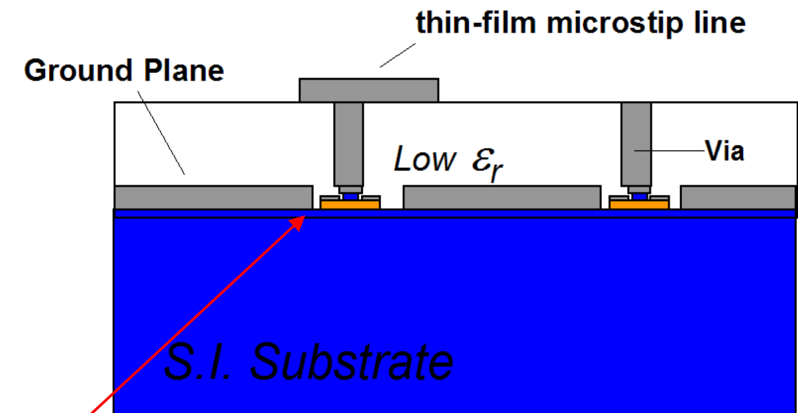
still have problem with package grounding

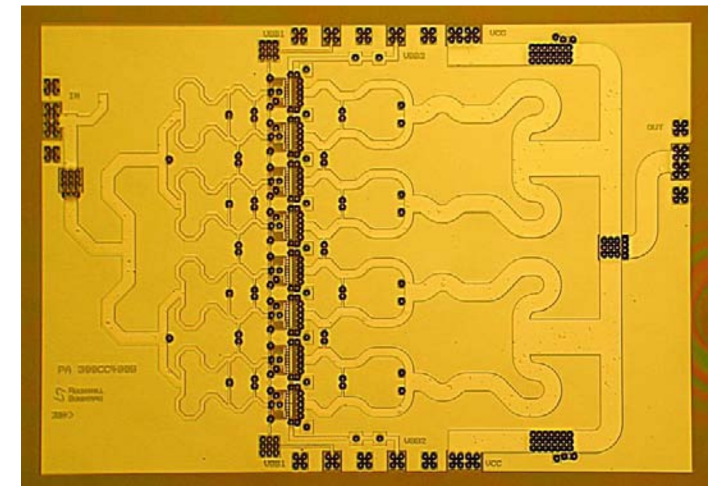


...need to flip-chip bond

thin dielectrics → narrow lines
→ high line losses
→ low current capability
→ no high-Z_o lines

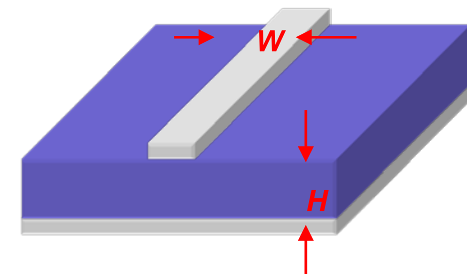






InP mm-wave PA (Rockwell)

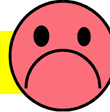
$$Z_o \sim \frac{\eta_o}{\varepsilon_r^{1/2}}\left(\frac{H}{W+H}\right)$$



IC Interconnects -- Inverted Thin-Film Microstrip

narrow line spacing → IC density

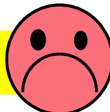
Some substrate radiation / substrate losses



No breaks in ground plane

... no ground breaks at device placements

still have problem with package grounding



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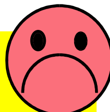
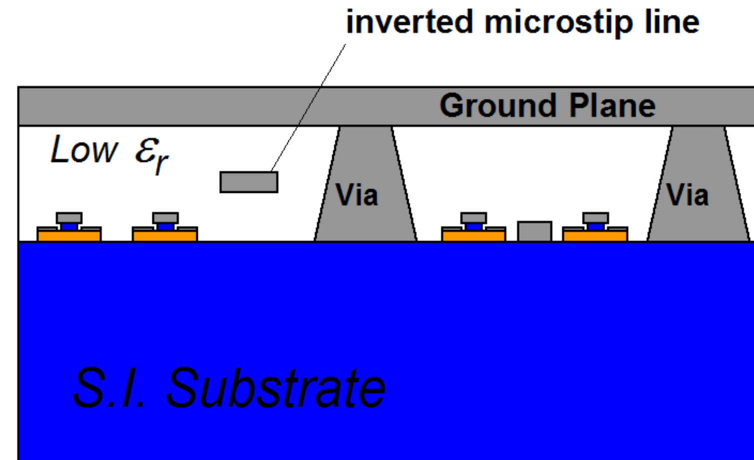
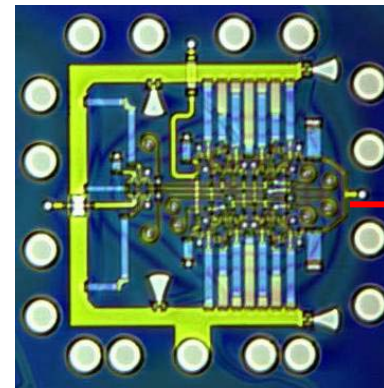
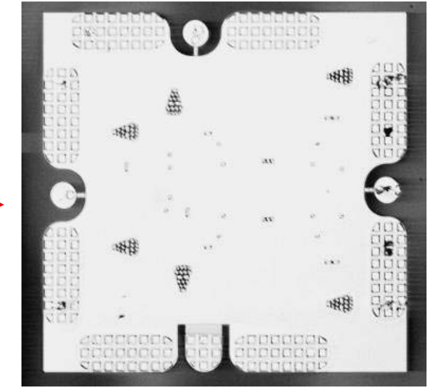
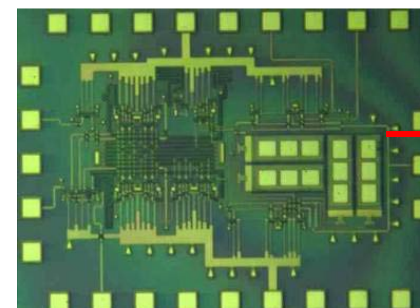


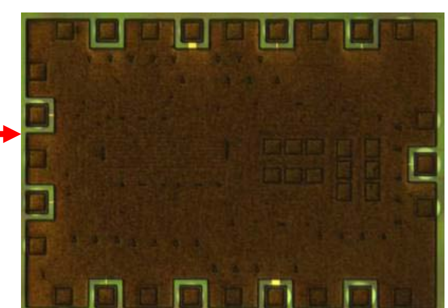






InP 150 GHz master-slave latch





InP 8 GHz clock rate delta-sigma ADC

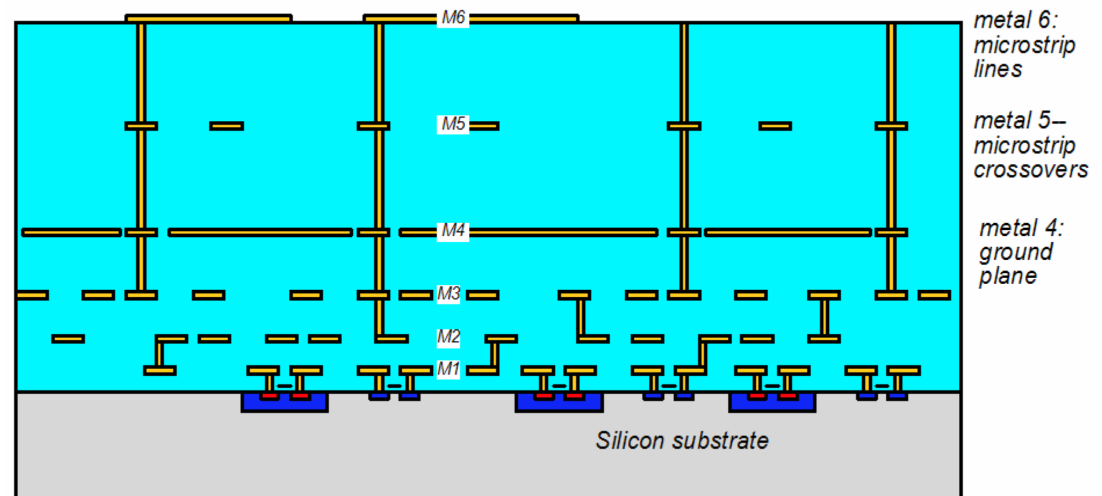
VLSI Interconnects with Ground Integrity & Controlled Z_o

narrow line spacing → IC density

no substrate radiation, no substrate losses

negligible breaks in ground plane

negligible ground breaks @ device placement

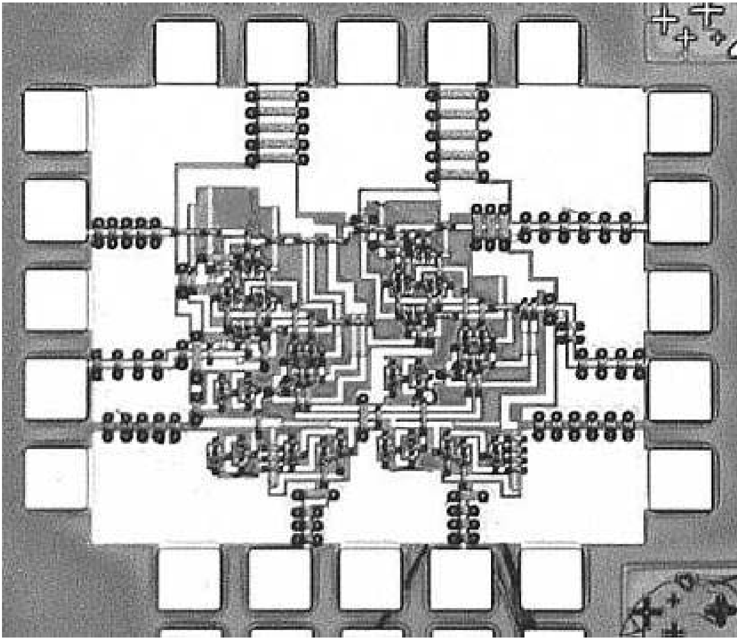


still have problem with package grounding

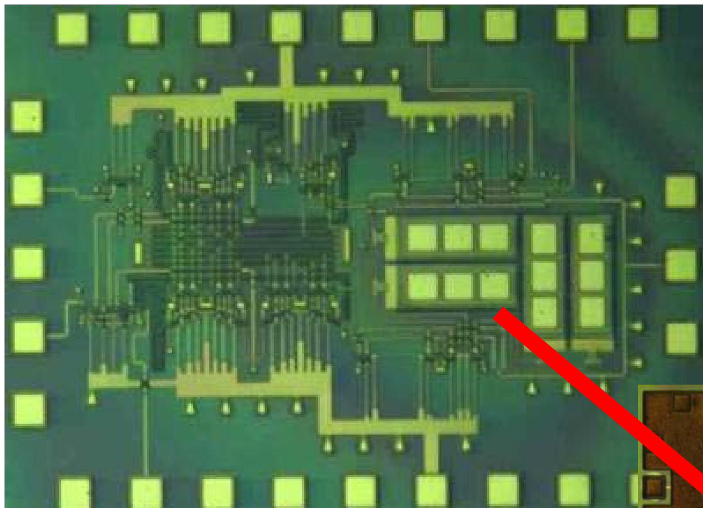
...need to flip-chip bond

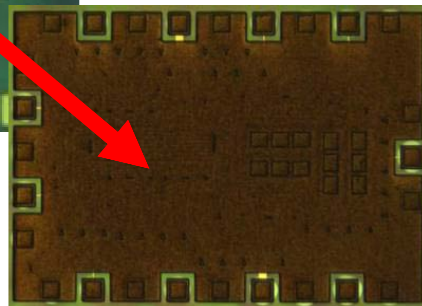
thin dielectrics → narrow lines
→ high line losses
→ low current capability
→ no high-Z_o lines

No clean ground return ? → interconnects can't be modeled !



35 GHz static divider
interconnects have no clear local ground return
interconnect inductance is non-local
interconnect inductance has no compact model



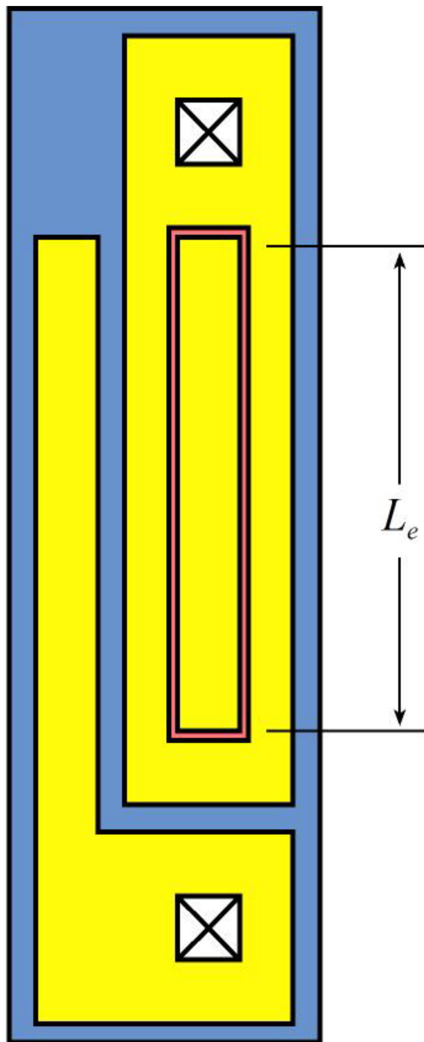


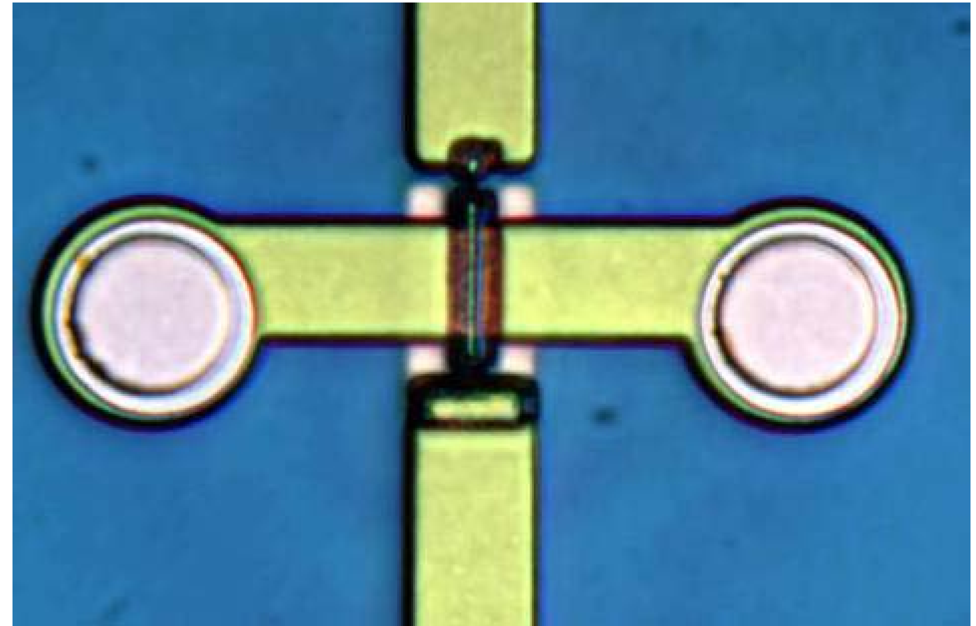
8 GHz clock-rate delta-sigma ADC
thin-film microstrip wiring
every interconnect can be modeled as microstrip
some interconnects are terminated in their Zo
some interconnects are not terminated
...but ALL are precisely modeled

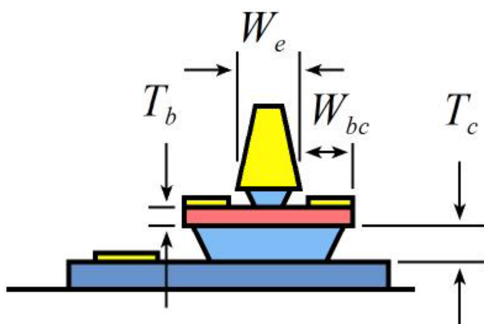
InP 8 GHz clock rate delta-sigma ADC

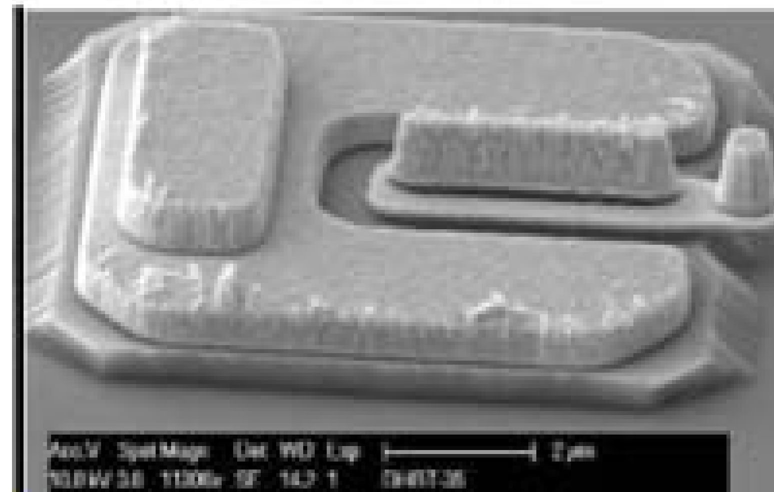
Active Devices: Bipolar Transistors

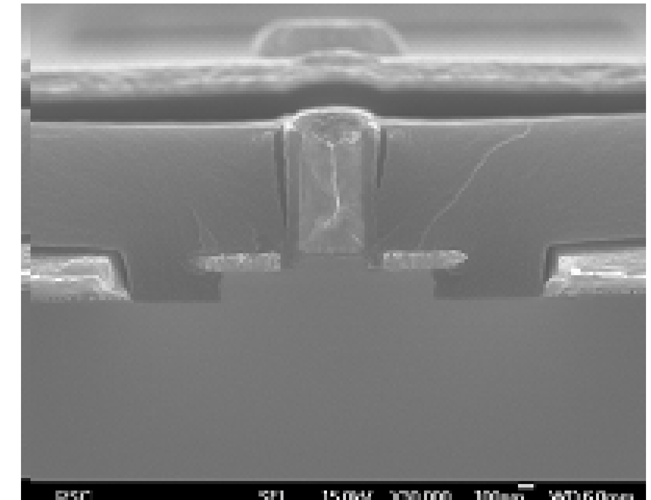
HBT Physical Structure





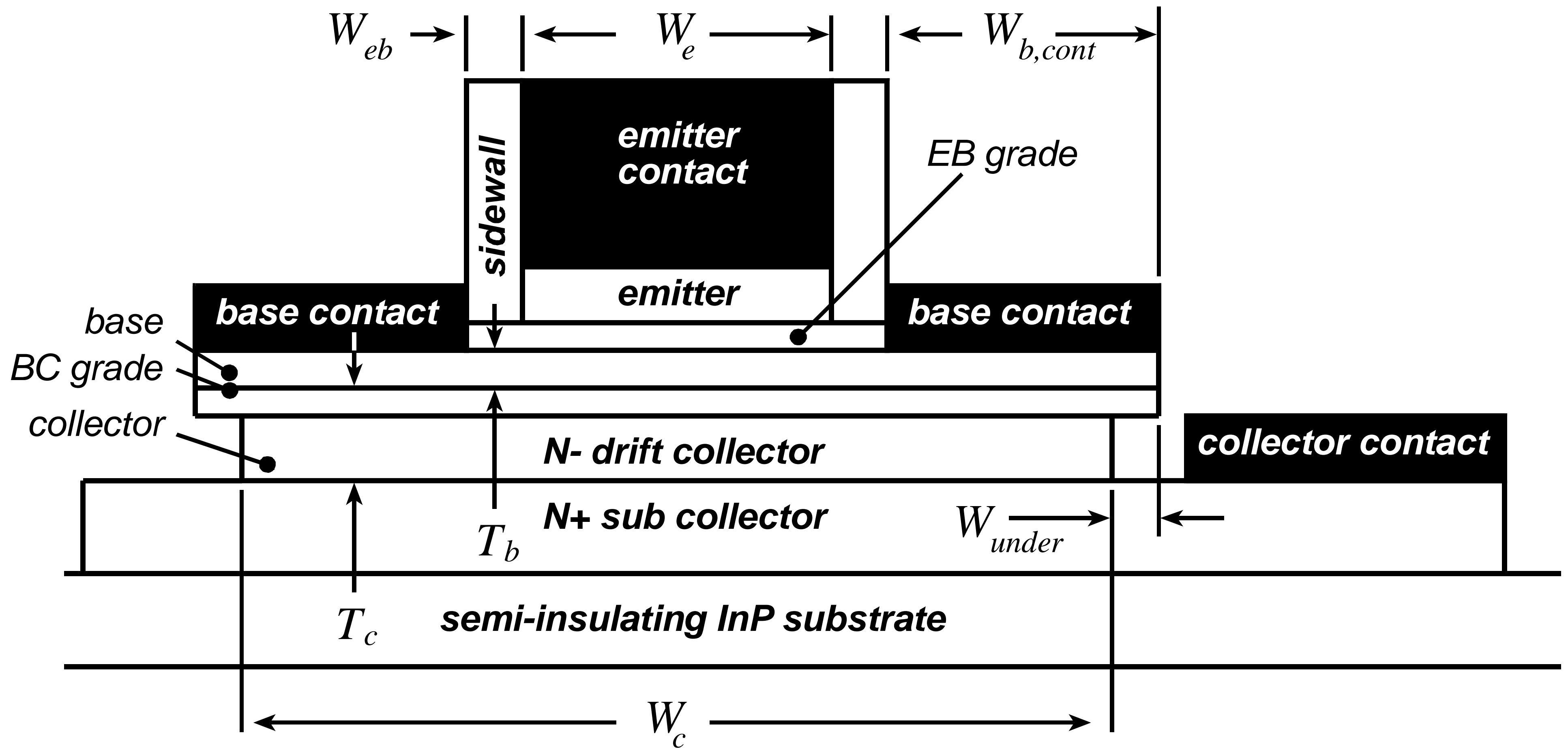




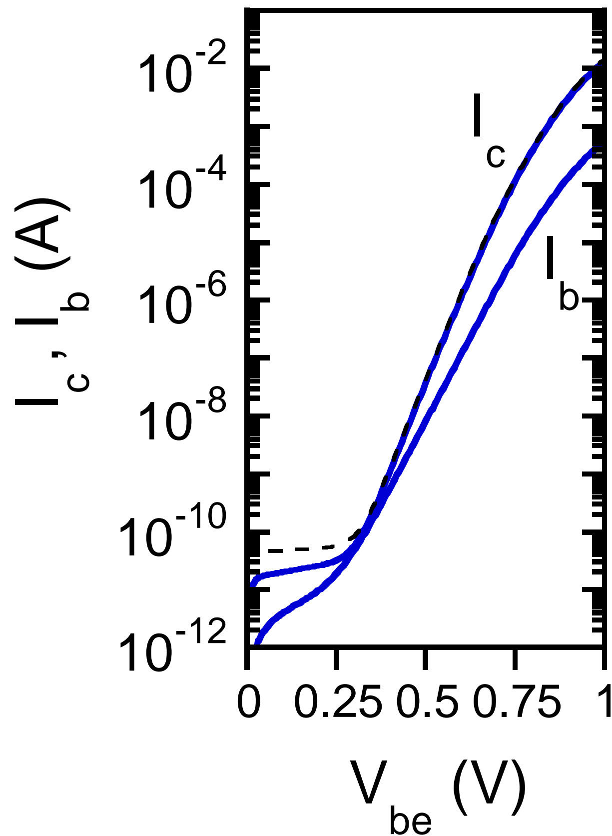


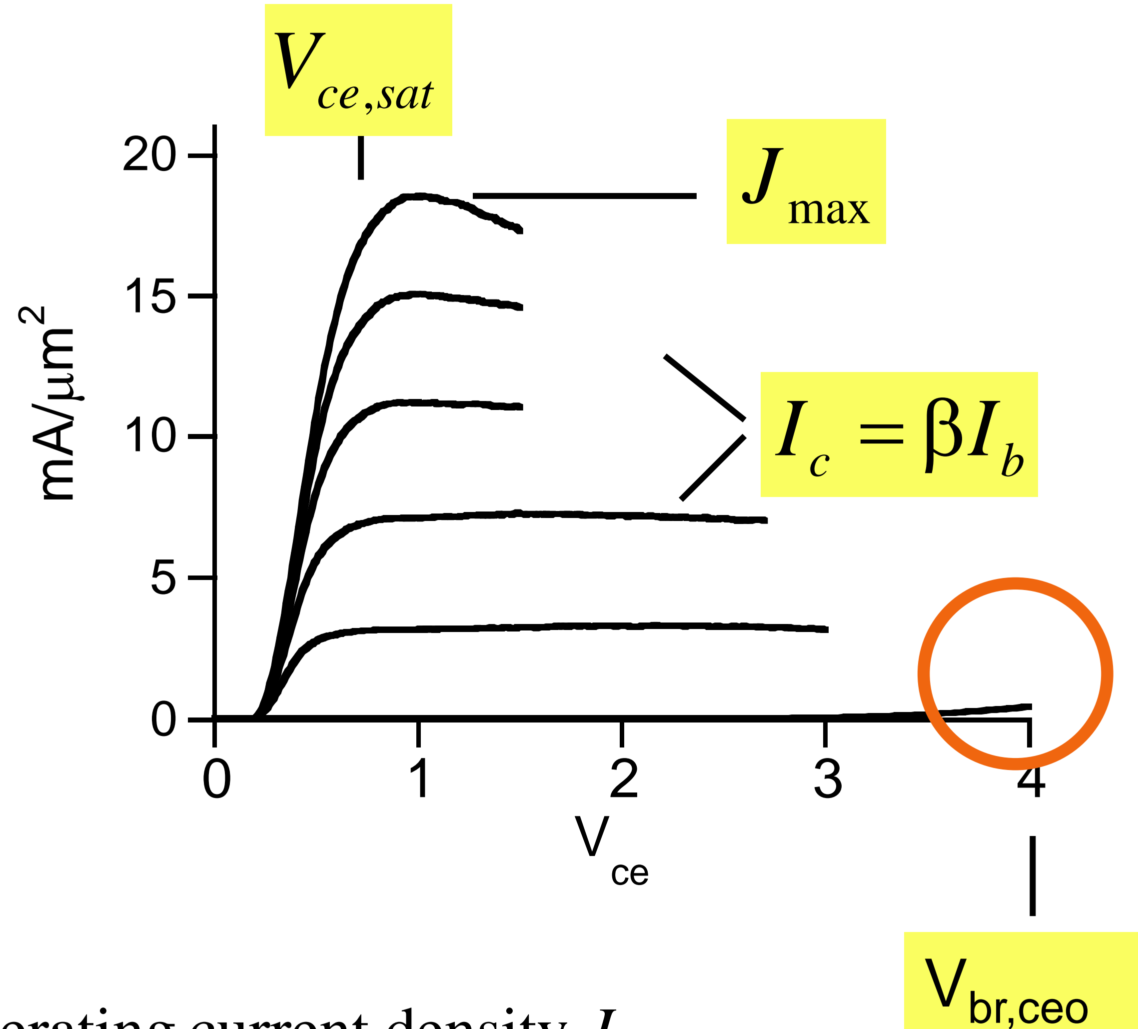
Physical structure, symbolic

Device Stripe Length = L_E
perpendicular to drawing



Bipolar Transistor: DC characteristics: common-emitter





HBTs have a maximum operating current density J_{max}.

This is set by : Kirk effect, Maximum power density.

More information in design project documentation.

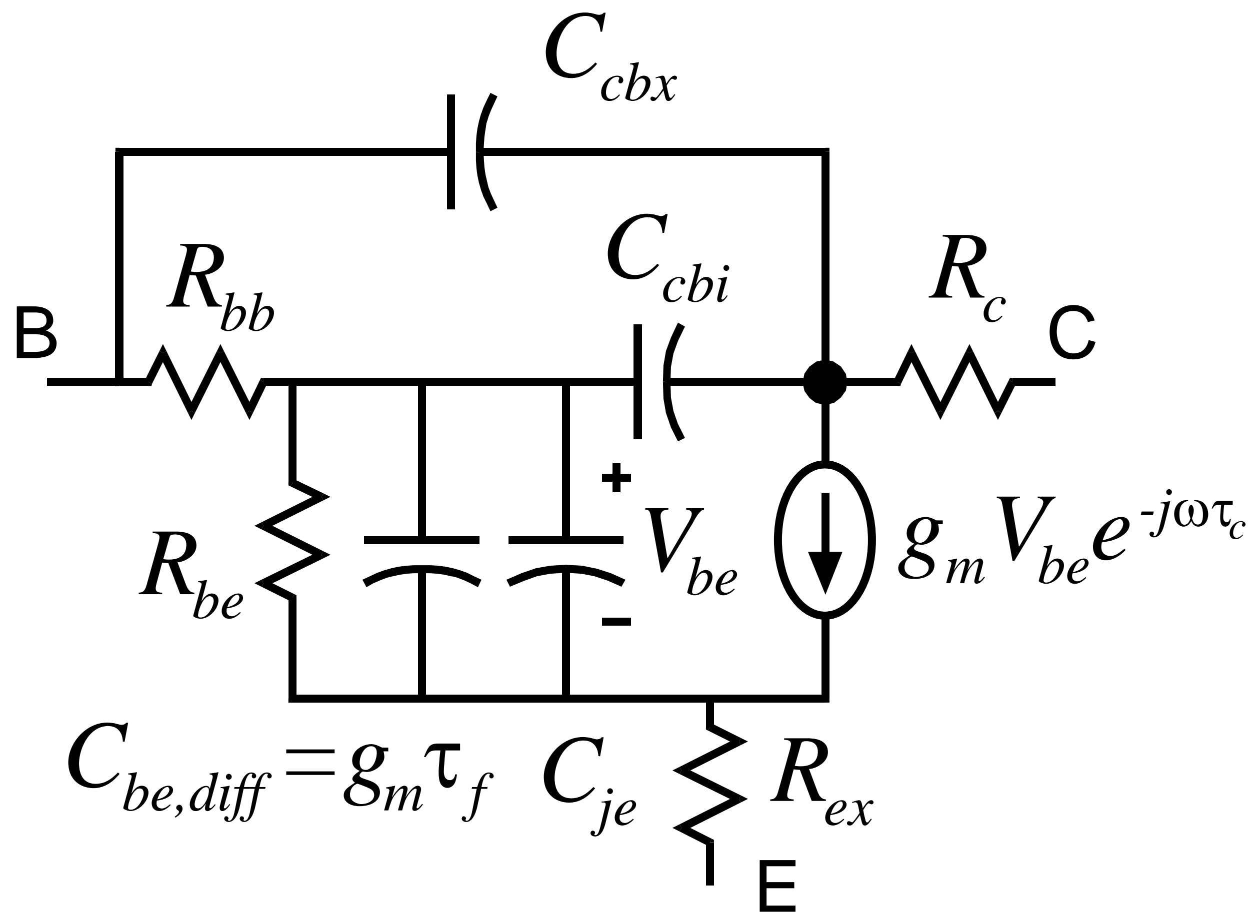
HBT hybrid-Pi equivalent-circuit model

$$g_m = g_{mo}\exp(-j\omega\tau_c)$$

$$g_{mo} = qI_c / nkT$$

$$R_{be} = \beta / g_{mo}$$

$$\tau_f = \tau_b + \tau_c$$



Given N_{finger} HBT fingers of emitter length L_E :

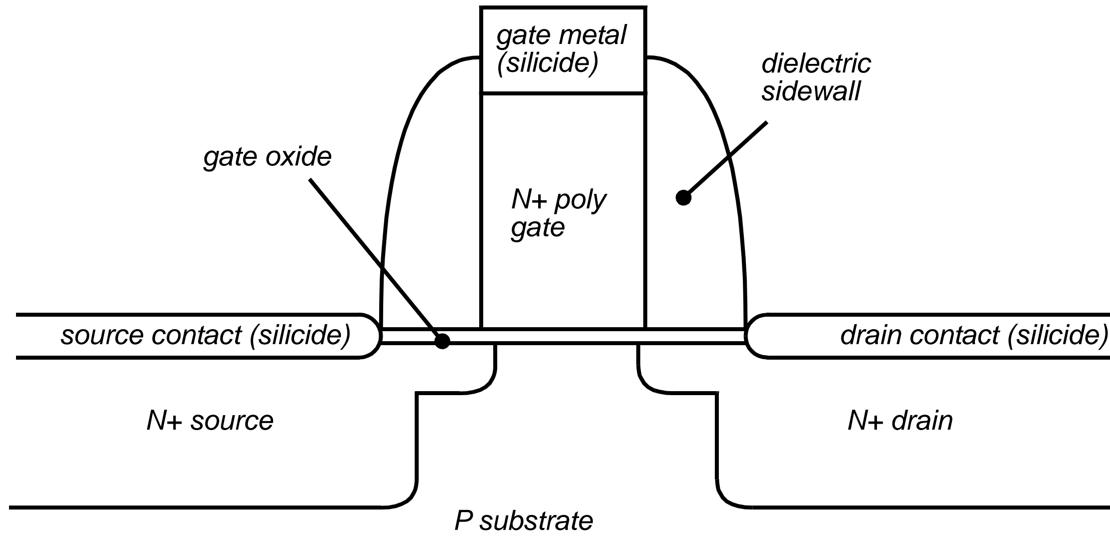
$(C_{je}, C_{cbi}, C_{cbx})$ vary in proportion to $N_{finger}L_E$,

$(R_{bb}, R_{ex}, R_c, I_{c,\max})$ vary in proportion to $1/N_{finger}L_E$.

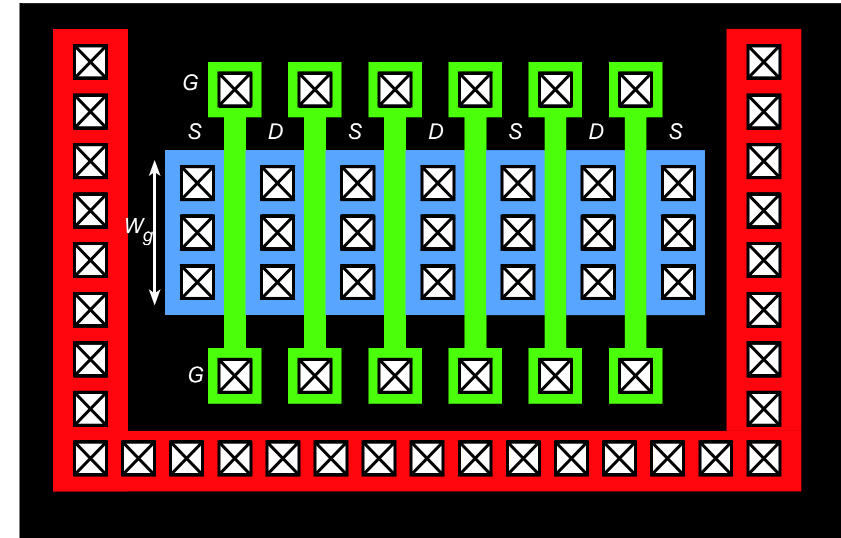
Active Devices: MOSFETs

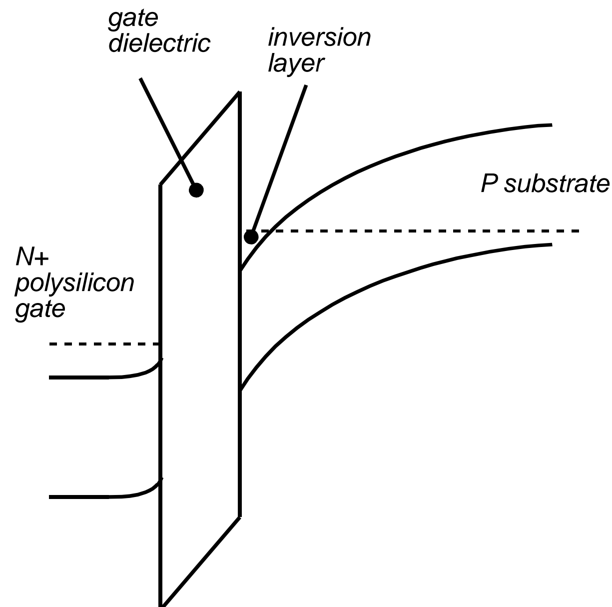
MOSFETS

Cross-Section

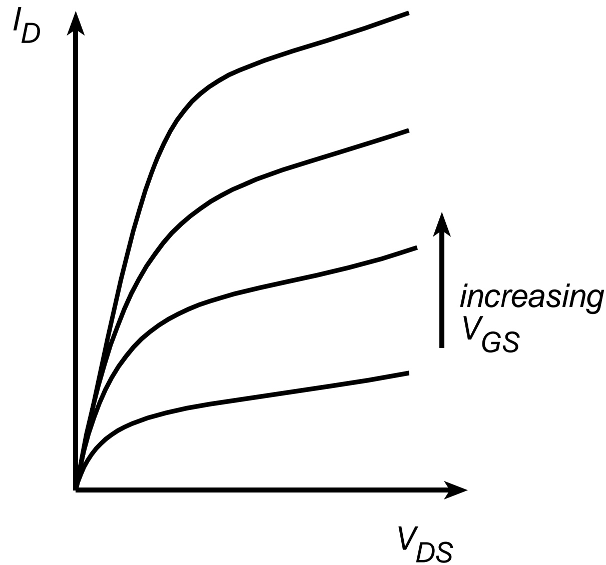


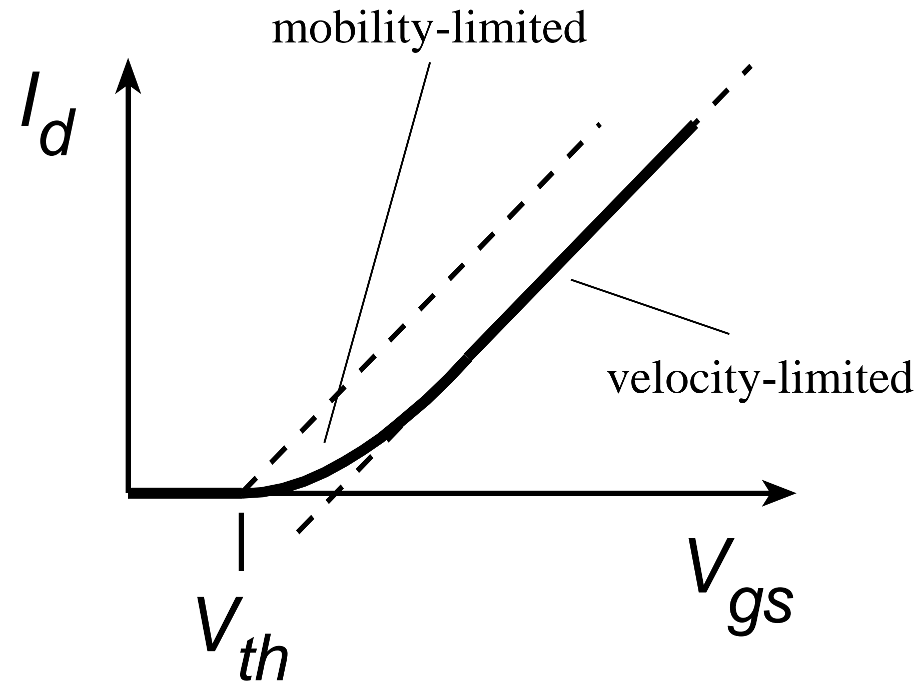
Layout (multi-finger)





MOSFET DC Characteristics





For drain voltages larger than the knee voltage :

mobility – limited current

$$I_{D,\mu} = \mu c_{ox} W_g (V_{gs} - V_{th})^2 / 2L_g$$

velocity – limited current

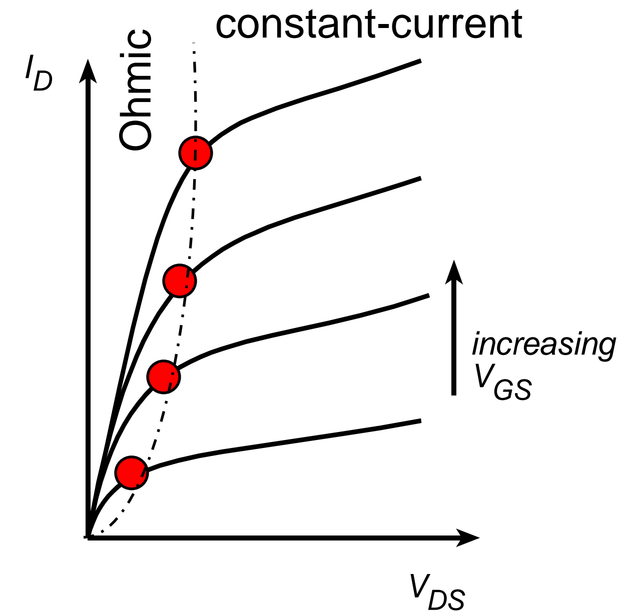
$$I_{D,v} = c_{ox} W_g v_{sat} (V_{gs} - V_{th})$$

Generalized Expression

$$\left(\frac{I_D}{I_{D,v}}\right)^2 + \left(\frac{I_D}{I_{D,\mu}}\right) = 1$$

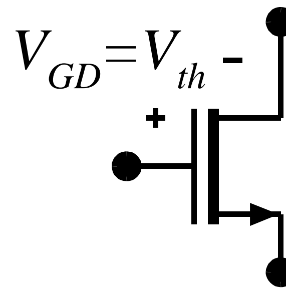
Knee Voltage: Mobility-Limited Case

The knee voltage defines the boundary between the Ohmic and constant - current regions

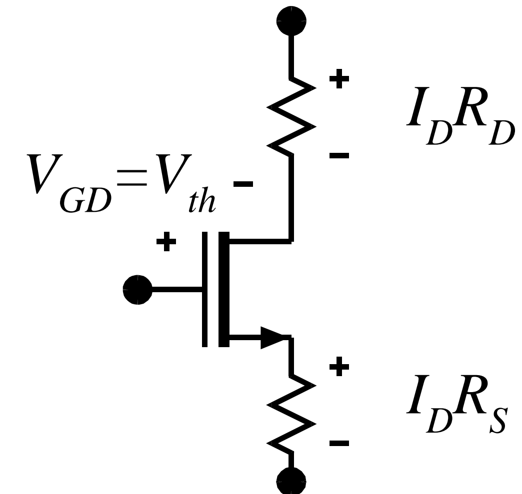


In the mobility - limited regime, the knee in curve occurs when

$$V_{dg} = V_{ds} - V_{gs} = -V_{th}$$

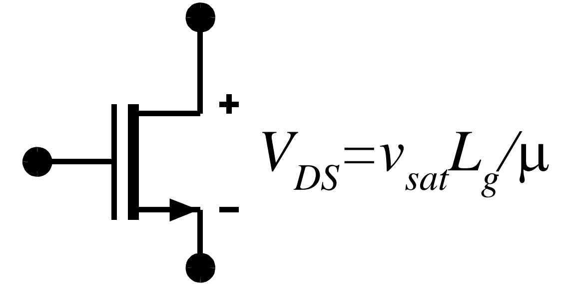


The Knee Voltage is further increased by voltage drops across the parasitic source & drain resistances.

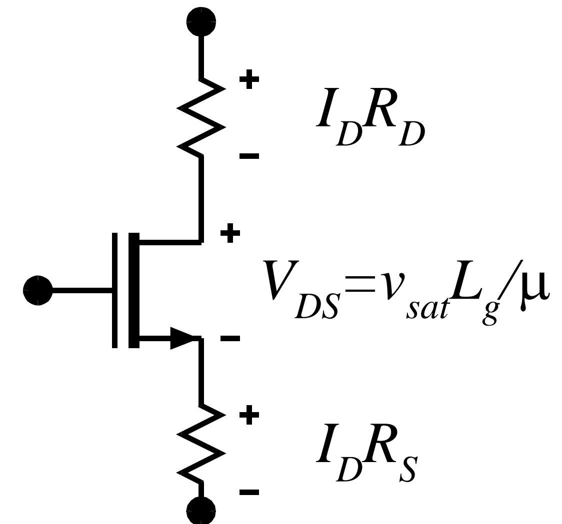


Knee Voltage: Velocity-Limited Case

In the velocity - limited regime, the knee in curve occurs when $V_{ds} = v_{sat} L_g / \mu$



Again, the Knee Voltage is further increased by voltage drops across the parasitic source & drain resistances.

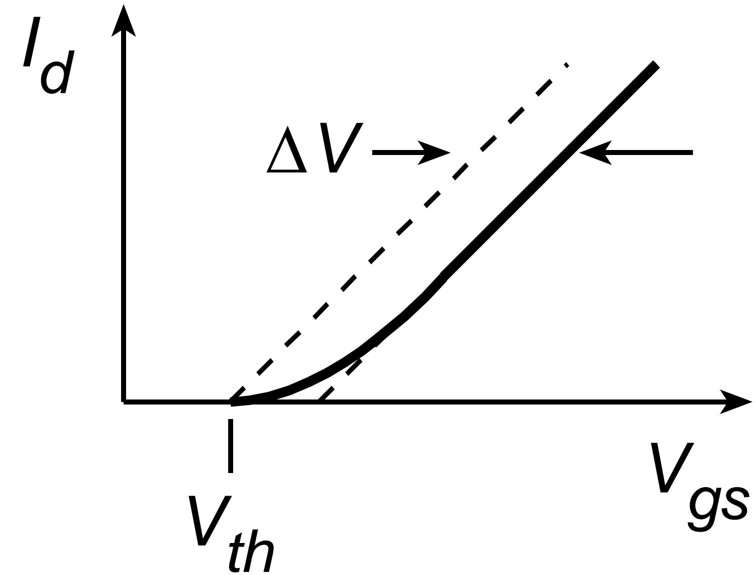


MOSFET Transconductance

mobility – limited

$$I_{D,\mu} = \mu c_{ox} W_g (V_{gs} - V_{th})^2 / 2L_g$$

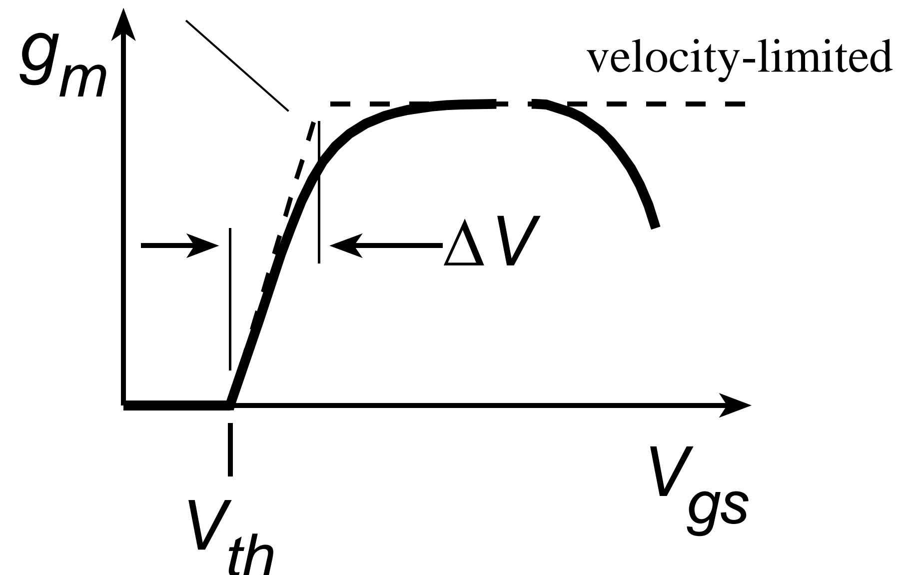
$$\rightarrow g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu c_{ox} W_g (V_{gs} - V_{th}) / L_g$$



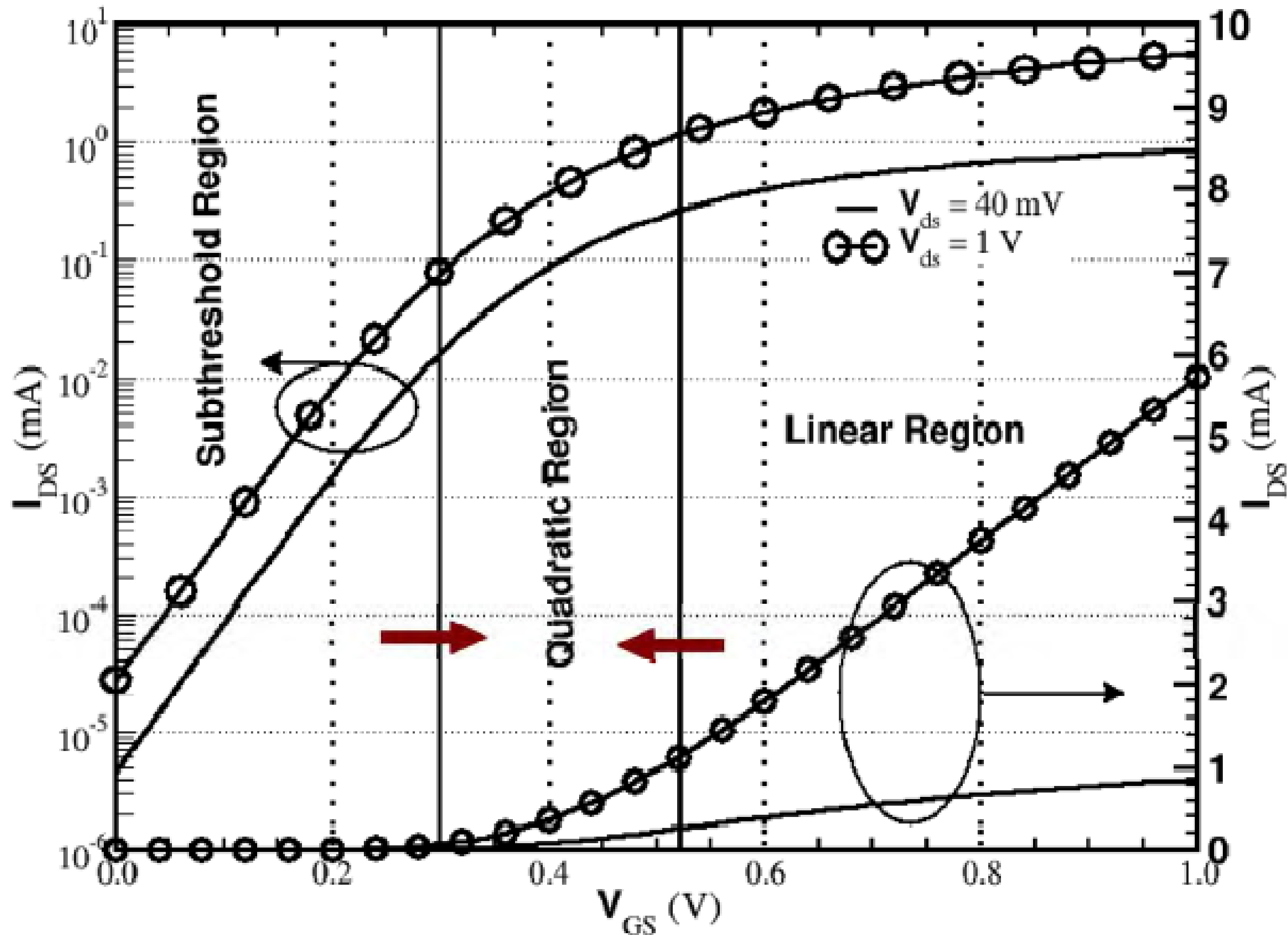
velocity – limited

$$I_{D,v} = c_{ox} W_g v_{sat} (V_{gs} - V_{th})$$

$$\rightarrow g_m = \frac{\partial I_D}{\partial V_{GS}} = c_{ox} W_g v_{sat}$$

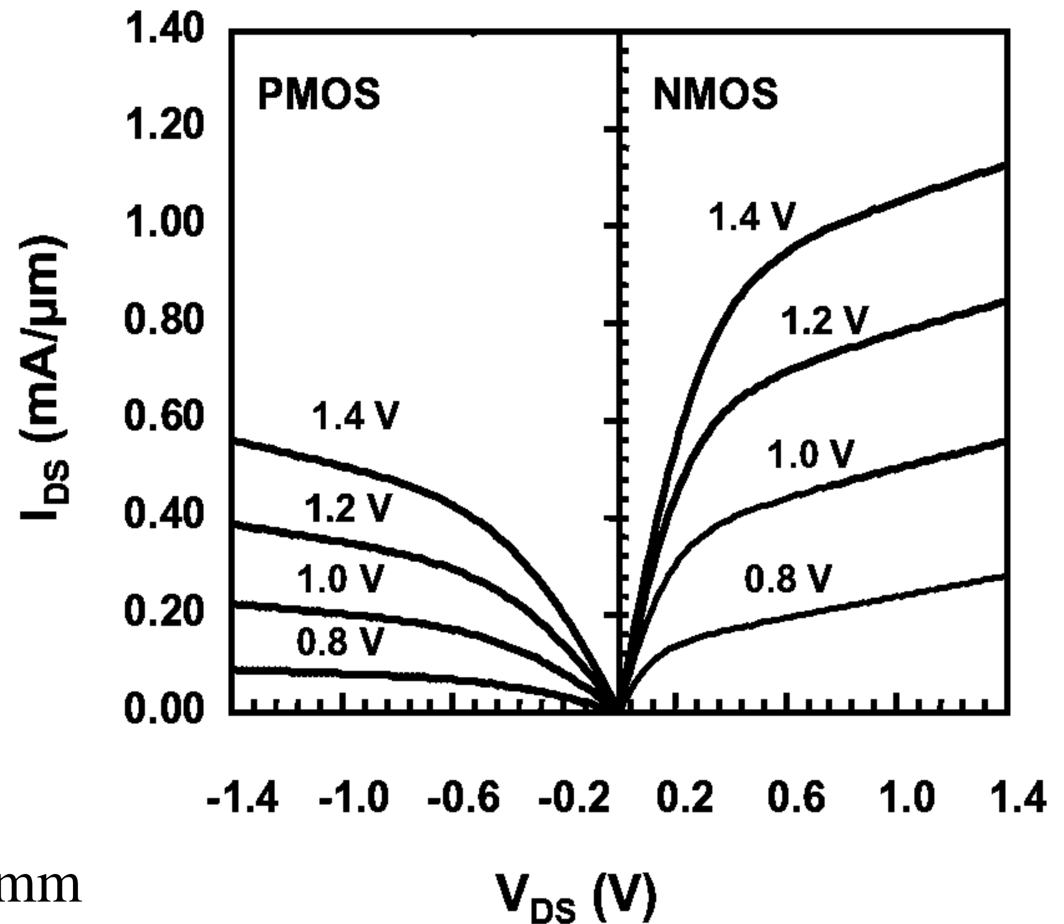


Linear vs. Square-Law Characteristics: 90 nm



Sorin Voinigescu, CSICS RF & High Speed CMOS, Nov. 12, 2006

90 nm MOSFET DC Characteristics



N - channel

$$g_m / W_g = c_{ox} v_{sat} = 1.4 \text{ mS} / \mu\text{m} = 1.4 \, \text{S} / \text{mm}$$

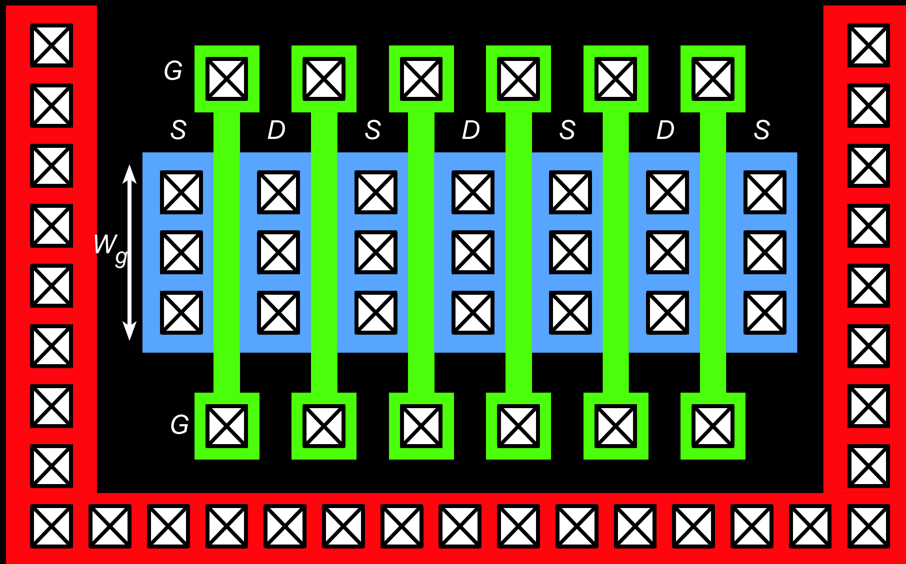
$$V_{th} = 0.6 \text{ V} \quad 1/\lambda \sim 3\text{V}$$

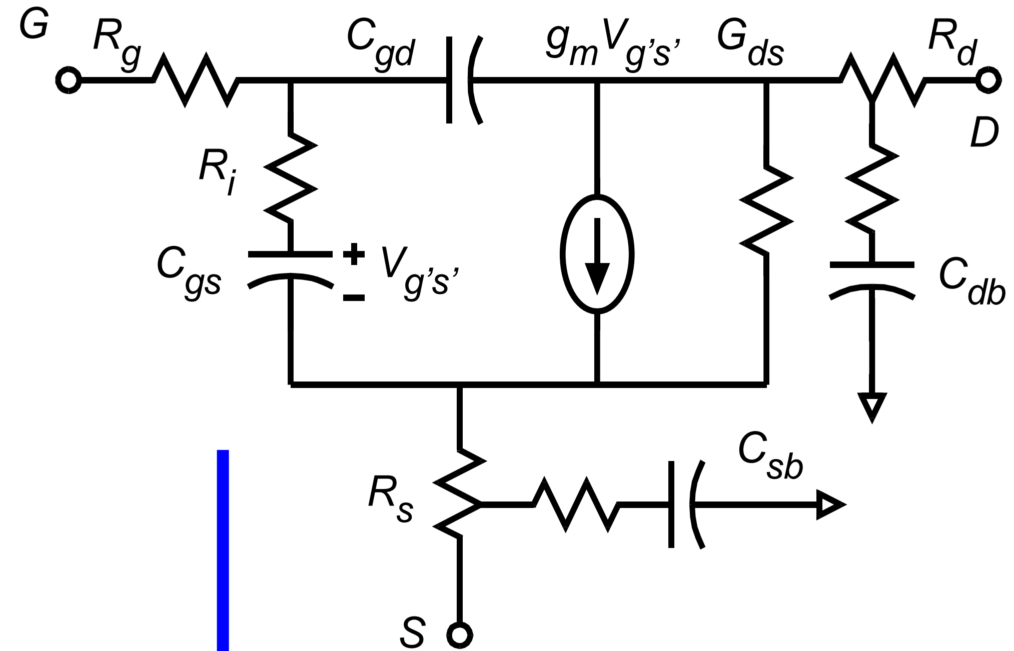
P - channel

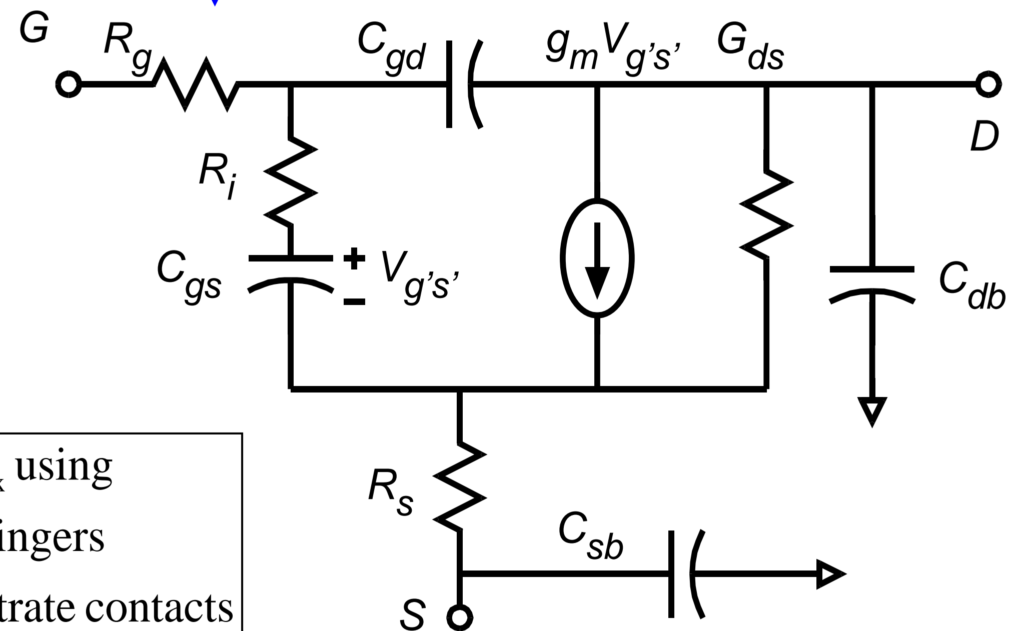
$$g_m / W_g = c_{ox} v_{sat} = 0.7 \text{ mS} / \mu\text{m} = 0.7 \, \text{S} / \text{mm}$$

$$|V_{th}| = 0.6 \text{ V} \quad 1/\lambda \sim 3\text{V}$$

Device Structure and Model







$N =$# gate fingers, $W_g =$ gate width

$$g_m \sim \frac{\varepsilon}{T_{eq}} v_{eff}(NW_g) \text{ or } \frac{\varepsilon}{T_{eq}} \mu (NW_g)(V_{gs} - V_{th})$$

$$C_{gs} \sim \frac{\varepsilon}{T_{eq}} L_g (NW_g) \qquad R_g \sim \frac{\rho_s}{12 L_g}\left(\frac{W_g}{N}\right) + \frac{R_{end}}{2N}$$

$$C_{gd} \propto NW_g \qquad R_d \propto 1/NW_g$$

$$G_{ds} \propto NW_g \qquad R_s \propto 1/NW_g$$

$$R_i \sim 1/g_m \qquad C_{sb} \propto NW_g$$

$$C_{db} \propto NW_g$$

Increase $f_{\max}$ using
- short gate fingers
- ample substrate contacts

Oversimplified Model

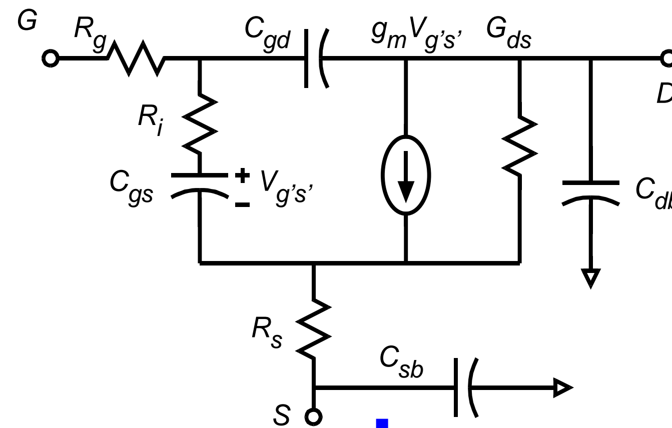
For rough hand analysis, etc

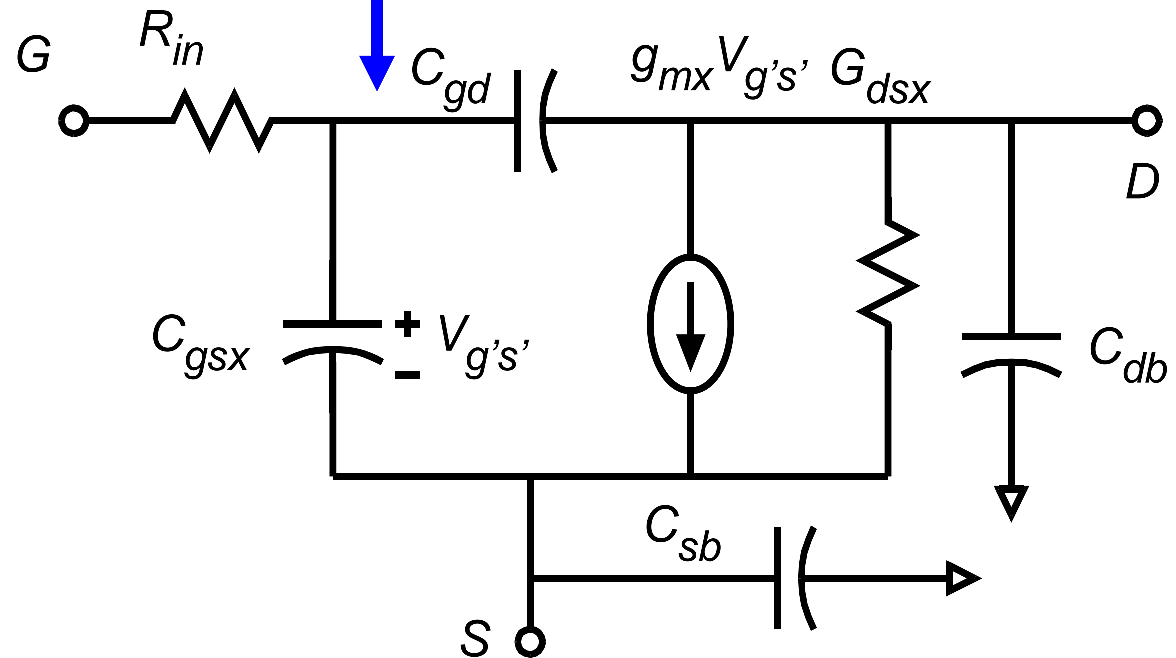
$$g_{mx} \sim \frac{g_m}{1+g_m R_s}$$

$$C_{gsx} \sim \frac{C_{gs}}{1+g_m R_s}$$

$$G_{dsx} \sim \frac{G_{ds}}{1+g_m R_s}$$

$$R_{in} \sim R_s + R_g + R_i$$





Approximate cutoff frequencies

$$1/2\pi f_\tau \sim C_{gs}/g_m + C_{gd}/g_m + (R_s + R_d)C_{gd}$$

$$f_{\max} \sim \frac{f_\tau}{2\sqrt{(R_s + R_g + R_i)G_{ds} + 2\pi R_g C_{gd}}}$$

End