Mixed-Signal IC Design Notes set 2:

Fundamentals of Analog IC Design

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Transistor Circuit Design

This note set

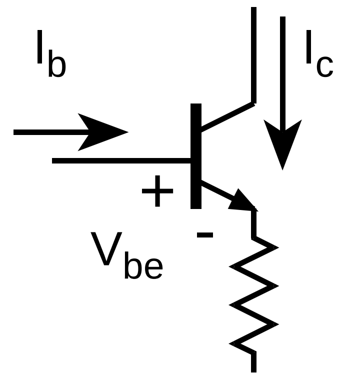
-reviews the basics
-starts at the level of a first IC design course
-moves very quickly

This will

-establish a common terminology
-accommodate capable students having minimal background in ICs.

DC models
DC bias analysis

Large-Signal Model For Bias Analysis



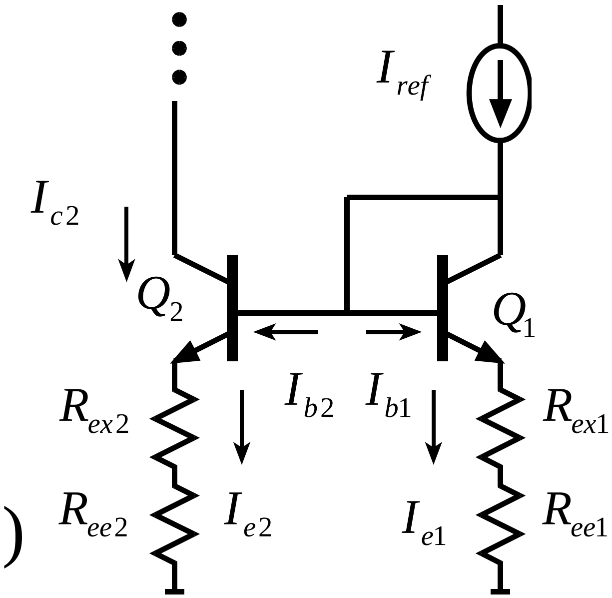
Provided that $V_{ce} > 0$,

$I_c = I_s \exp(V_{be} / V_T)$ and $I_b = I_c / \beta$, where $V_T = kT / q$

...note that V_{be} is specified internal to the emitter resistance R_{ex}

The $I_e R_{ex}$ drop is significant for HBTs operating at current densities near that required for peak transistor bandwidth.

DC Bias Example: Current Mirror

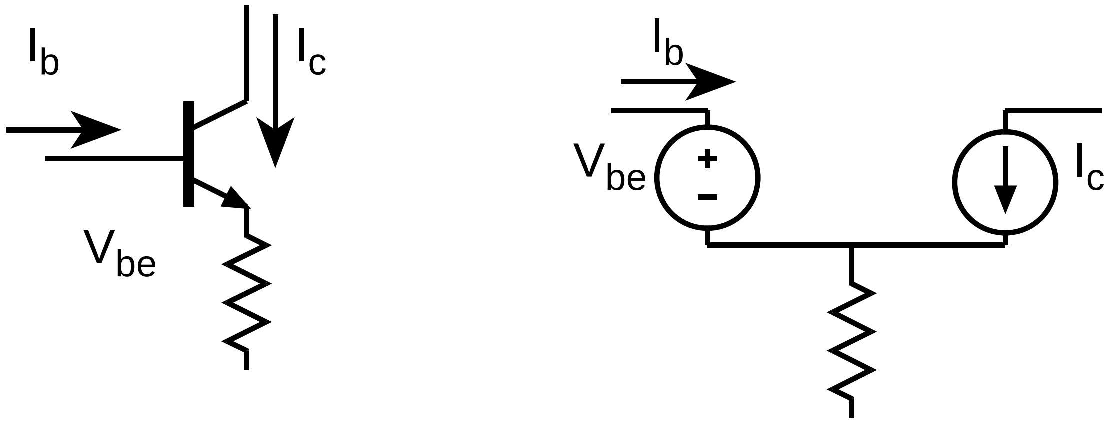


We have $V_{be1} + I_{e1}(R_{ex1} + R_{ee1}) = V_{be2} + I_{e2}(R_{ex2} + R_{ee2})$
and $V_{be1} = V_t \ln(I_{c1} / I_{s1}), V_{be2} = V_t \ln(I_{c2} / I_{s2})$

Assume that $\beta >> 1,\ \ R_{ee2} = 2R_{ee1}$
& assume that $A_{E1} = A_{E2}$ (A_E is the emitter area).

This implies $R_{ex1} = R_{ex2} / 2$, and $I_{s1} = 2I_{s2}$,
from which we find $I_{c2} = I_{c1} / 2$

Simpler DC Model for Bias Analysis



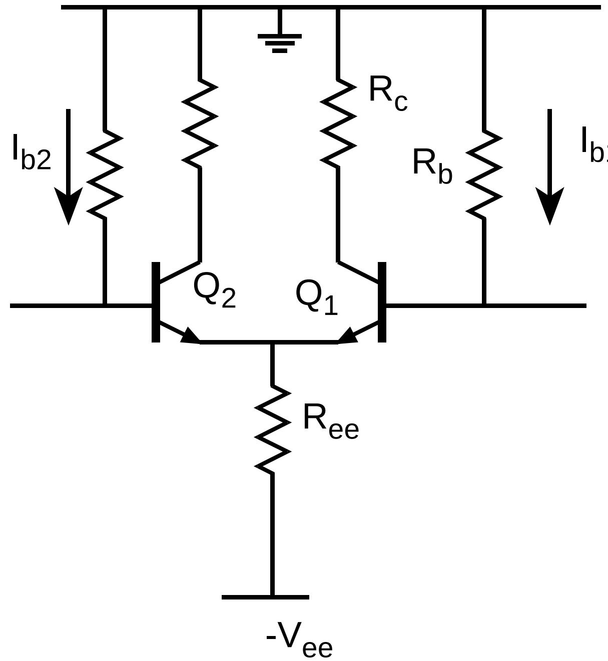
It is often sufficient in bias analysis to ignore the variation of V_{be} with I_c and instead take $V_{be} = V_{be,on} = \phi$.

$V_{be,on}$ depends upon current density and technology.

Biased at current densities within ~10% of peak bandwidth bias,

$$V_{be,on} = \phi \sim \begin{cases} 0.9\text{ V Modern Si/SiGe HBTs} \\ 0.7\text{ or }0.9\text{ V InGaAs/InP HBTs} \\ 1.4\text{ V GaAs/GaInP HBTs} \end{cases}$$

Simple DC Bias Example



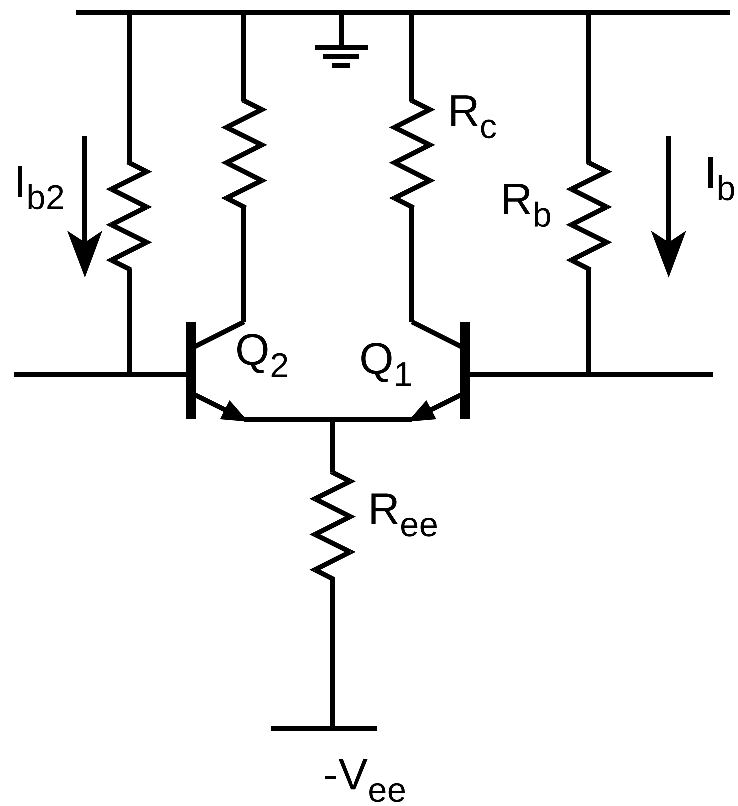
If we neglect the $I_b R_b$ drops, then $V_{b1} = V_{b2} = 0$ Volts.

Approximate $V_{e1} = V_{e2} = -\phi \cong -0.9$ V (SiGe).

$$I_{c1} + I_{c2} = 2I_{c1} = (-V_{ee} - 0.9V)/R_{ee}$$

$$I_{c1} = I_{c2} = (-V_{ee} - 0.9V)/2R_{ee}$$

Efficiently Handling Base Currents In Bias Analysis



If $I_b R_b$ drop is singificant,

one can solve simultaneous equations :

$$I_{c1} + I_{c2} = 2I_{c1} = (-V_{ee} - \phi - I_{b1}R_b) / R_{ee}$$

where $I_{b1} = I_{c1} / \beta$,

Quicker : find by iteration :

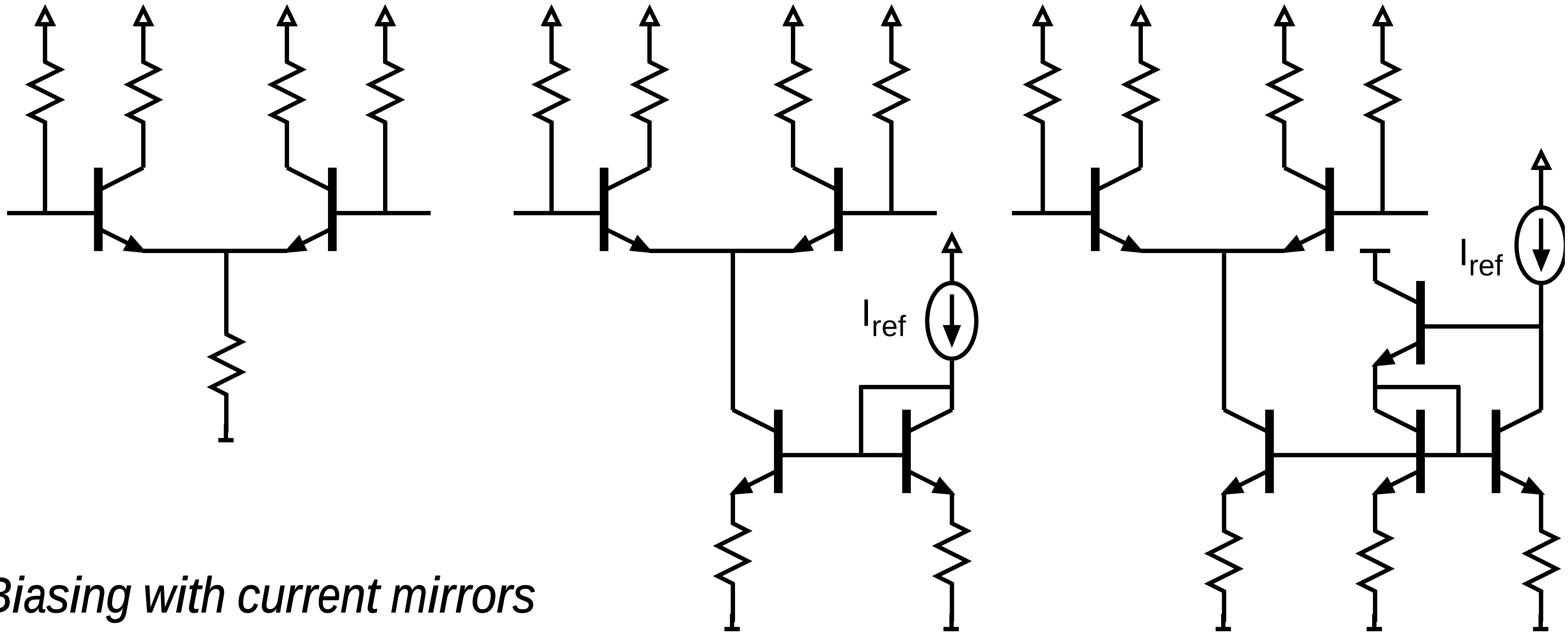
1) solve $I_{c1} = (-V_{ee} - \phi) / 2R_{ee}$

2) solve $I_{b1} \cong I_{c1} / \beta$

3) use this value of I_b to solve $I_{c1} = (-V_{ee} - \phi - I_{b1}R_b) / 2R_{ee}$

Works because any well - designed circuit has DC bias only weakly dependent upon β.

Typical Circuit Biasing in Mixed-Signal ICs



Biasing with current mirrors

more precise---

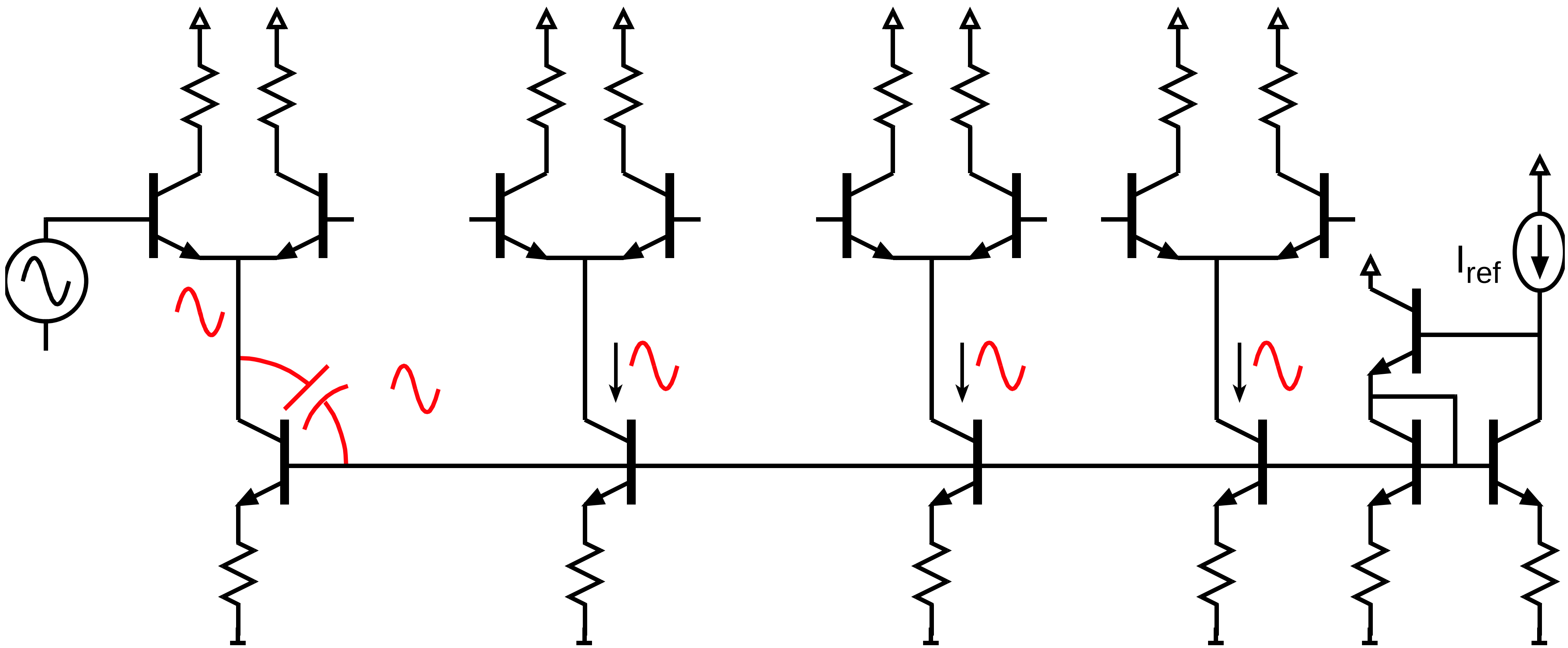
often more compact

but loads emitter node with C_{cb} ---or worse

and provides path for stage-stage coupling

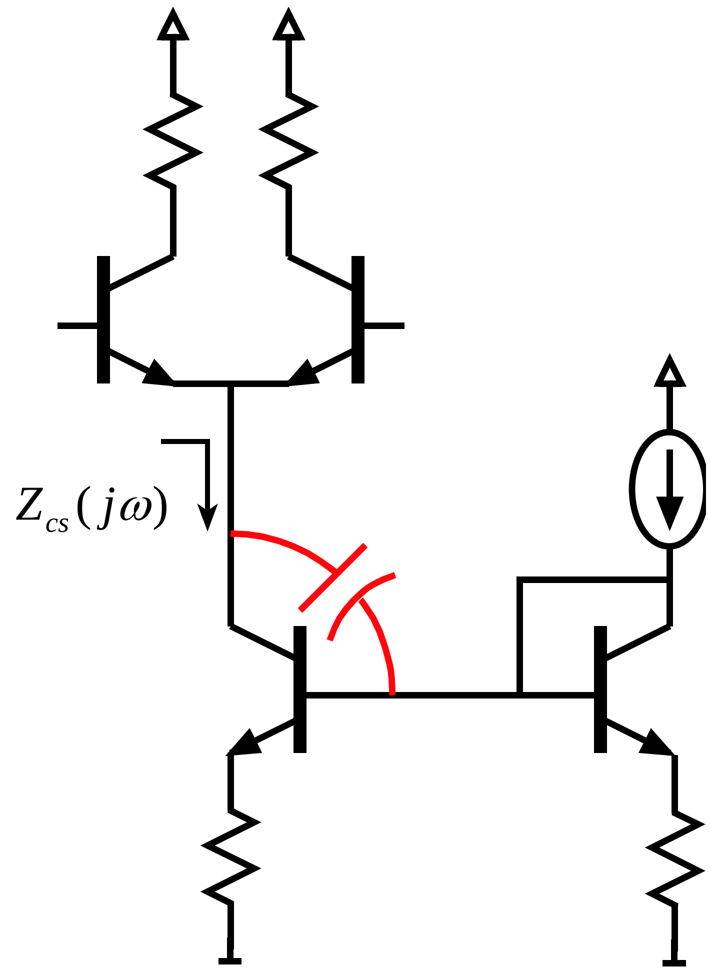
Resistive biasing--- resistively loads emitter node---lower DC precision

Problems with Current Mirror Biasing



stage-stage coupling through C_{cb} and the shared current mirror reference...

Problems with Current Mirror Biasing



Because of C_{cb} and C_{be}, the current source output impedance $Z_{cs}(j\omega)$ varies with frequency.

We will derive this in later lectures.

Implications:

increased common-mode gain at high frequencies

common-mode instability

Avoiding Thermal Instability

Given that $V_{be} = V_t \ln(I_{c2} / I_{s2}) = (kT / q)\ln(I_{c2} / I_{s2})$

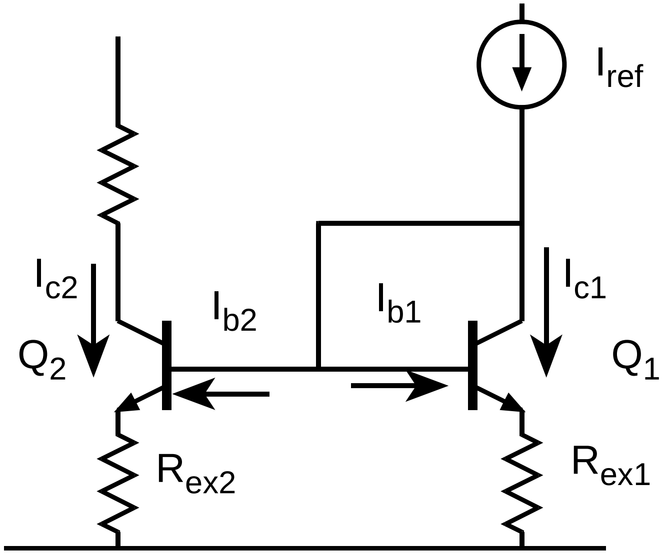
....note that $I_s \propto T^{3/2}$, so at constant I_c,

$dV_{be} / dT = (k / q)\ln(I_{c2} / I_{s2}) - (kT / q)(dI_{s2} / dT)^{-1}$

The device has some thermal resistance $dT / dP = \theta$ (Kelvin/Watt). Current mirror is thermally unstable if

$$1 < \frac{dI_c}{dV_{be}} \bullet \frac{dV_{be}}{dT} \bullet \frac{dT}{dP} \bullet \frac{dP}{dI_c}$$

$$1 < \frac{1}{R_{ex} + kT / qI_e + R_{ee}} \bullet \frac{dV_{be}}{dT} \bullet \theta \bullet V_{ce}$$



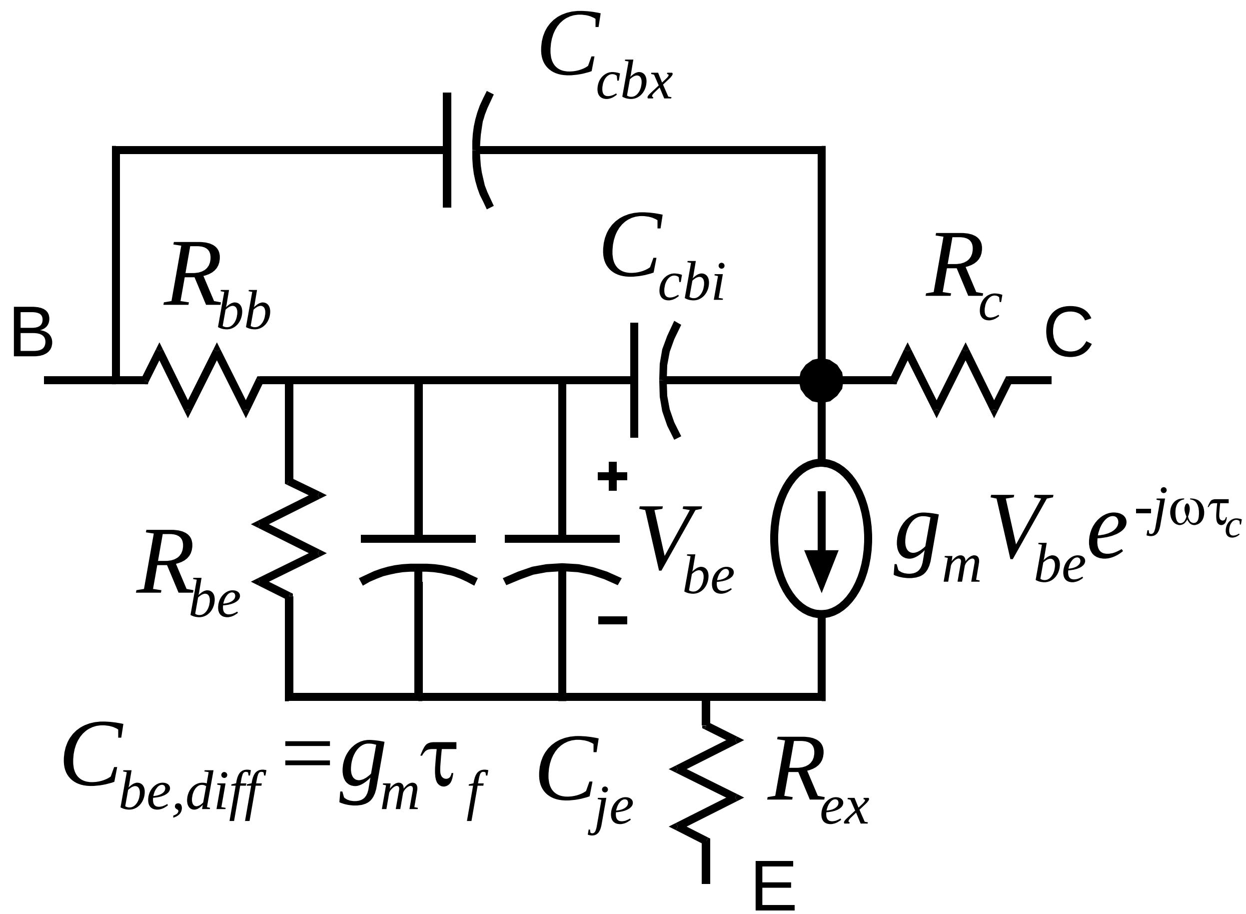
Fast Bipolar ICs normally use $I_e * R_{ee} \sim 300mV$ to avoid thermal runaway. Thermal runaway can also result from internal device temperature gradients. Large area devices must therefore be avoided...use array of smaller devices with ballasting. (process dependent)...UCSB HBT process puts safe maximum device area ~ 10 square microns at $10^5\ A/cm^2$ biasing

small-signal baseband analysis

Hybrid-π Bipolar Transistor Model

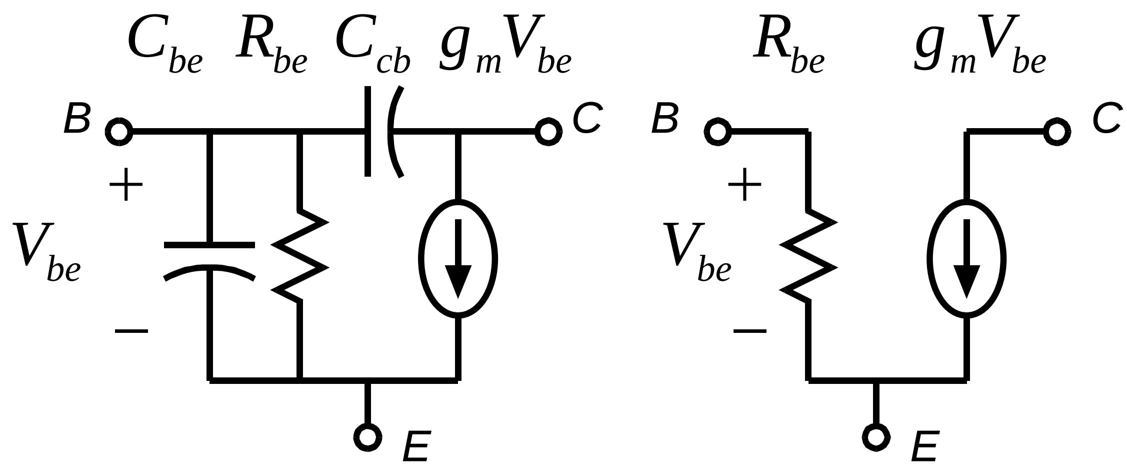
$$R_{be} = \beta / g_m$$

$$\tau_f = \tau_b + \tau_c$$



Accurate model, but too detailed for quick hand analysis

Oversimplified Model for Quick Hand Analysis

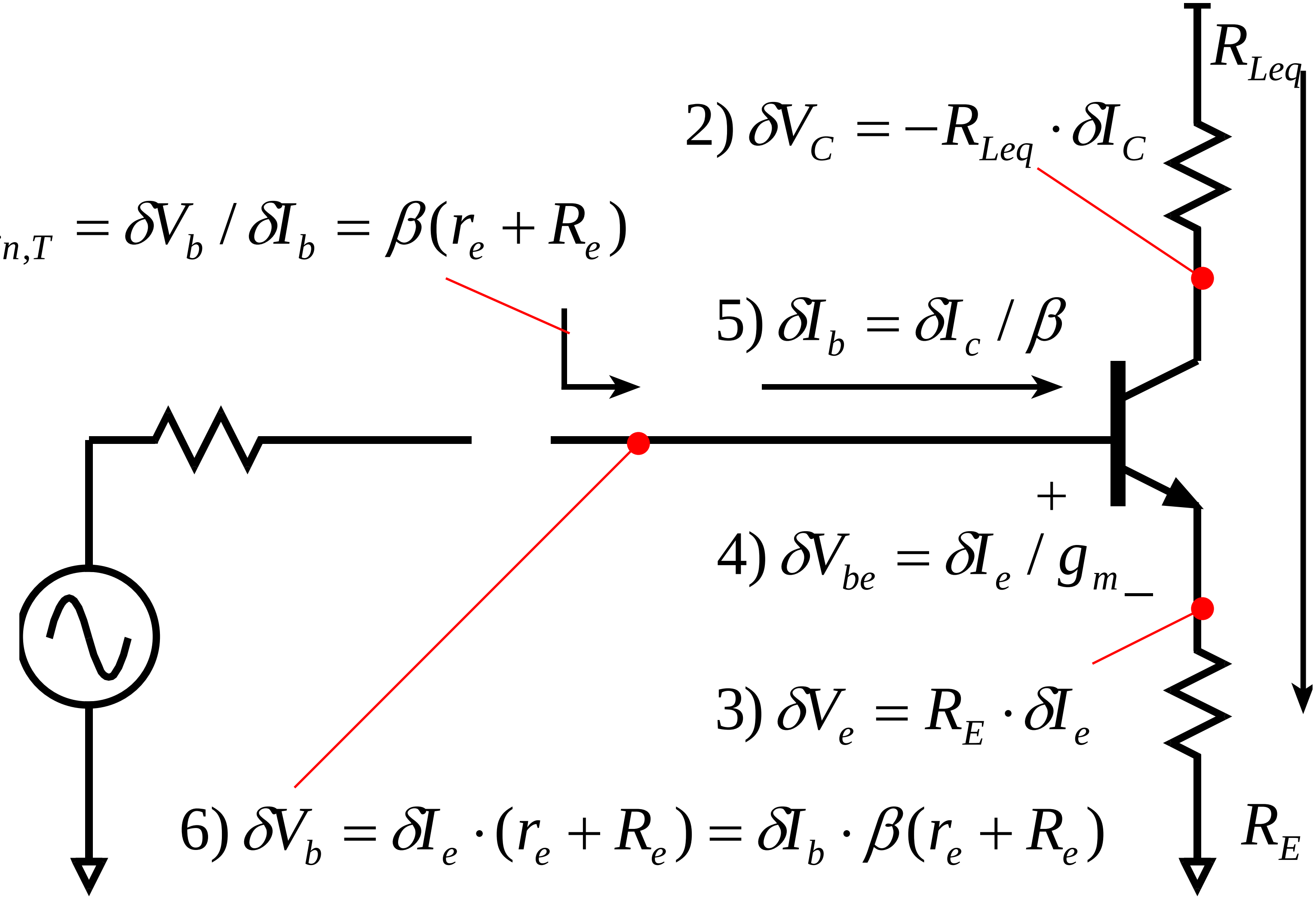


In most high-frequency circuits, the node impedance is low and R_{ce} is therefore negligible.

Neglecting R_{bb} in high-frequency analysis is a poor approximation but is nevertheless common in introductory treatments.

The "textbook" analyses which follow use this oversimplified model. These introductory treatments will later be refined.

Common Emitter Stage: Basics



1) $\delta I_e \cong \delta I_c$

2) $\delta V_C = -R_{Leq} \cdot \delta I_C$

3) $\delta V_e = R_E \cdot \delta I_e$

4) $\delta V_{be} = \delta I_e / g_m$

5) $\delta I_b = \delta I_c / \beta$

6) $\delta V_b = \delta I_e \cdot (r_e + R_e) = \delta I_b \cdot \beta (r_e + R_e)$

7) $R_{in,T} = \delta V_b / \delta I_b = \beta (r_e + R_e)$

8) $\delta V_{out} / \delta V_{in} = \delta V_{out} / \delta V_B = -R_{Leq} /(r_e + R_e) = -R_{Leq} /(R_e + 1/ g_m)$

Gain is - $R_{Leq} /(R_e + 1/ g_m)$; Transistor R_{in} is $\beta (r_e + R_E)$

Emitter Follower Stage: Basics

6) $R_{in,T} = \delta V_b / \delta I_b = \beta(r_e + R_{Leq})$

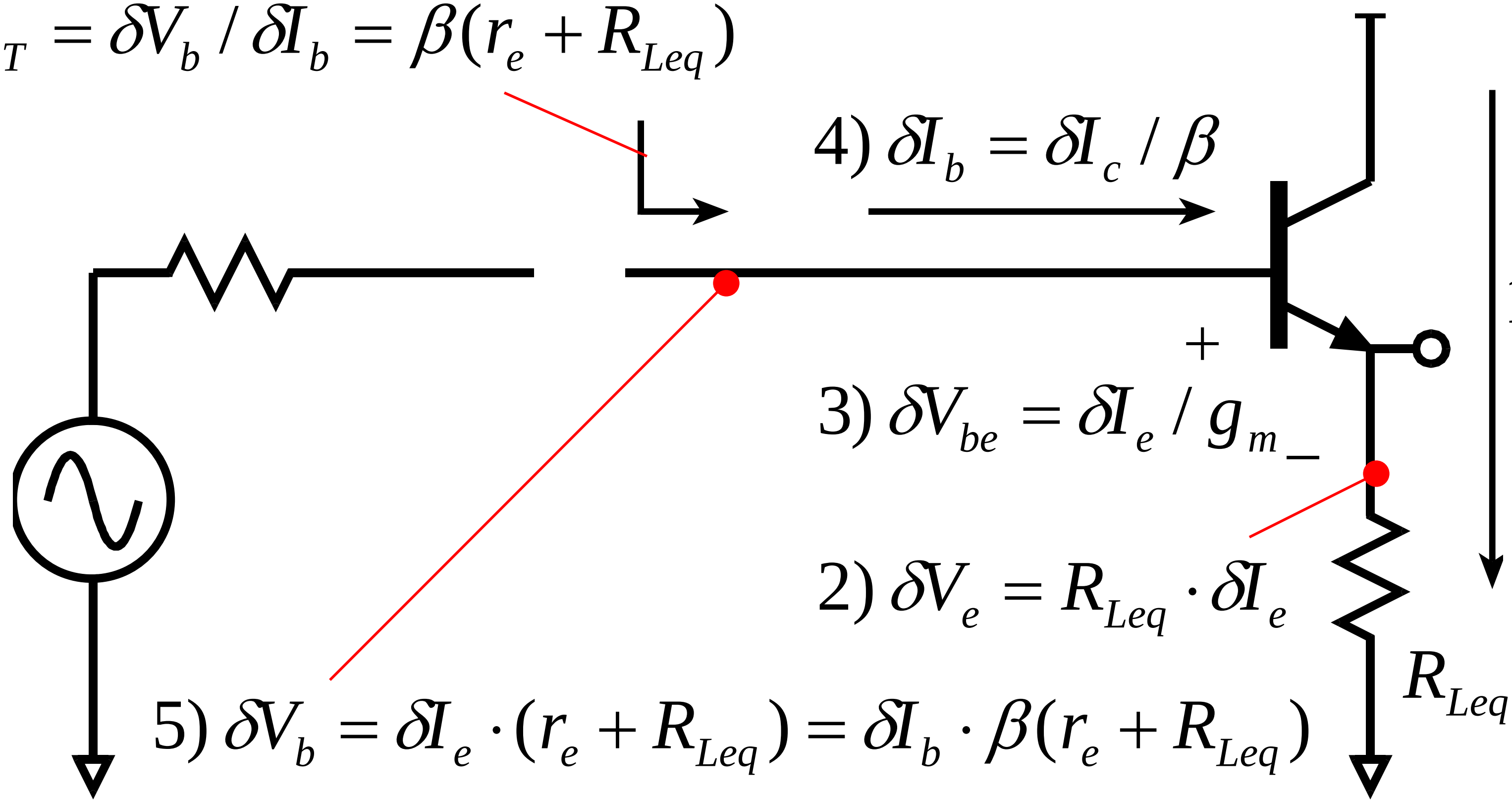
4) $\delta I_b = \delta I_c / \beta$

1) $\delta I_e \cong \delta I_c$

3) $\delta V_{be} = \delta I_e / g_m$

2) $\delta V_e = R_{Leq} \cdot \delta I_e$

5) $\delta V_b = \delta I_e \cdot (r_e + R_{Leq}) = \delta I_b \cdot \beta(r_e + R_{Leq})$



7) $\delta V_{out} / \delta V_{in} = \delta V_{out} / \delta V_E = R_{Leq} /(r_e + R_{Leq}) = R_{Leq} /(R_{Leq} + 1/ g_m)$

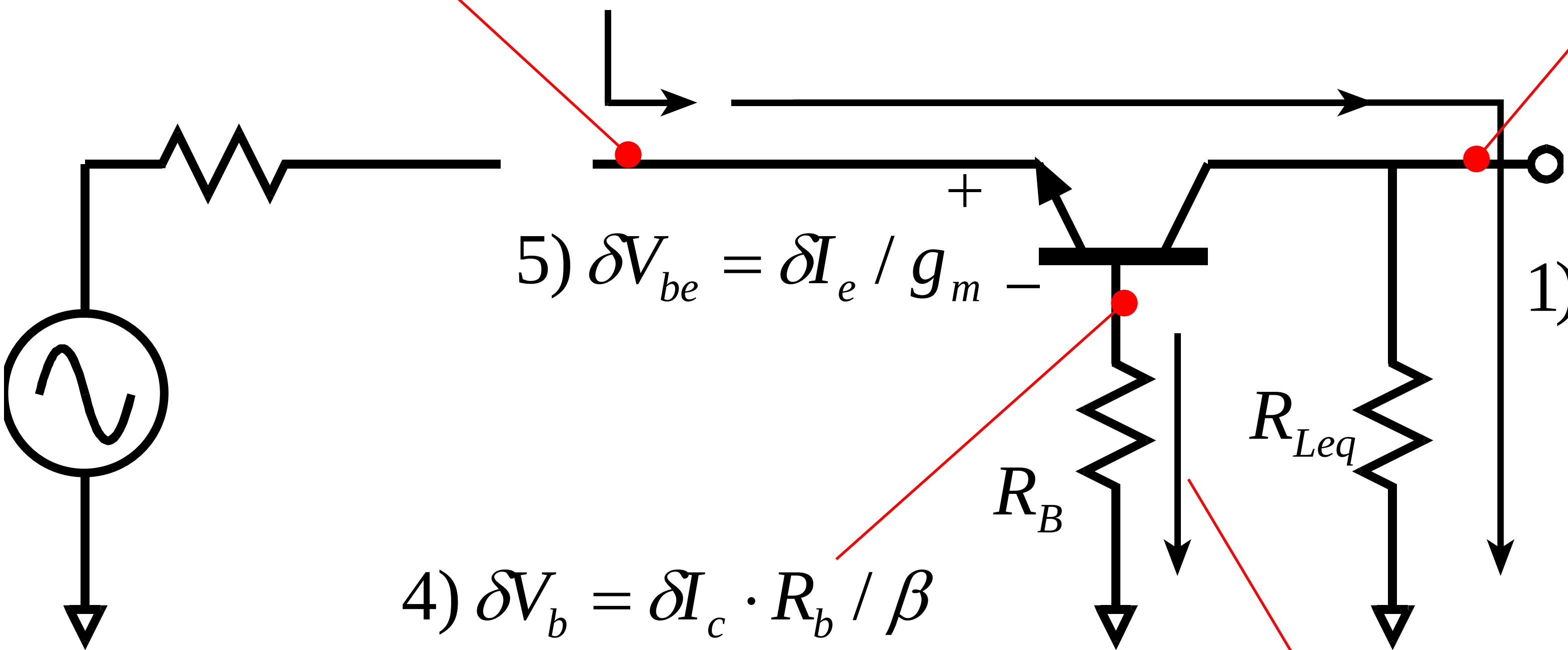
Gain is $R_{Leq} /(R_{Leq} + 1/ g_m)$; Transistor R_{in} is $\beta(r_e + R_E)$

Common-Base Stage: Basics

$$6)\ \delta V_{in} = \delta I_e \cdot (r_e + R_b/\beta)$$

$$2)\ \delta V_{out} = R_{Leq} \cdot \delta I_C$$

$$7)\ R_{in,T} = \delta V_e/\delta I_e = r_e + R_B/\beta$$



$$5)\ \delta V_{be} = \delta I_e / g_m$$

$$1)\ \delta I_e \cong \delta I_c$$

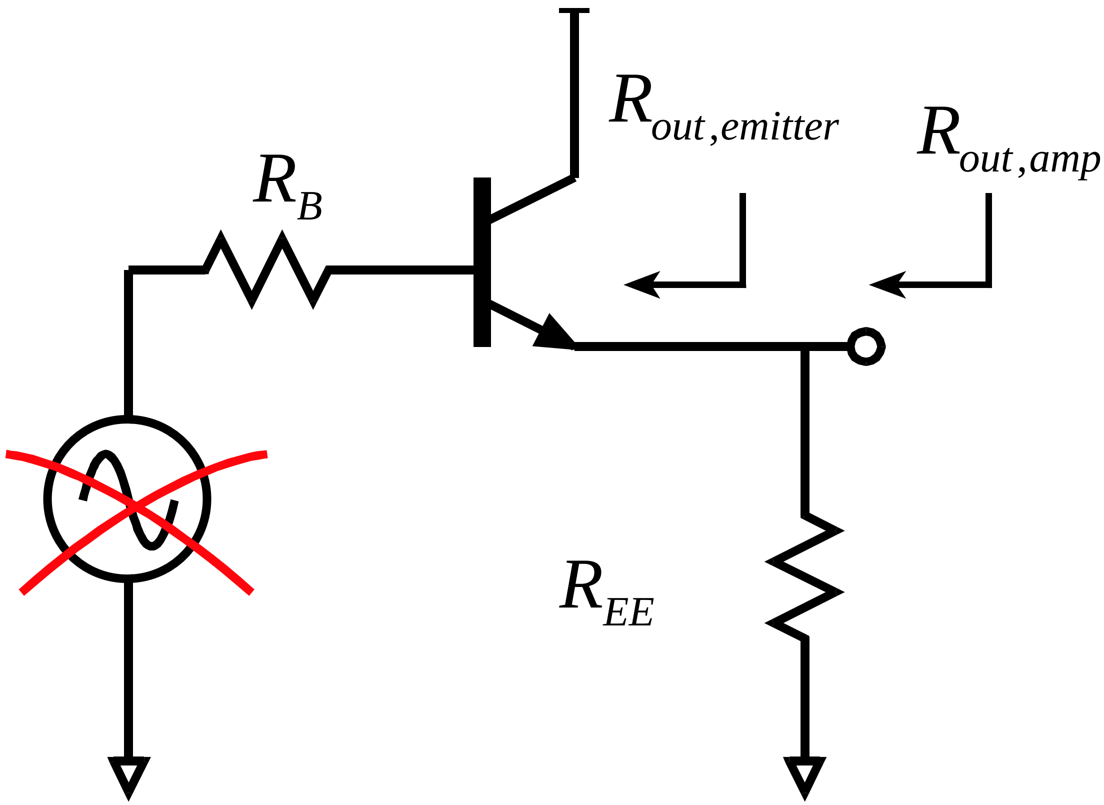
$$4)\ \delta V_b = \delta I_c \cdot R_b/\beta$$

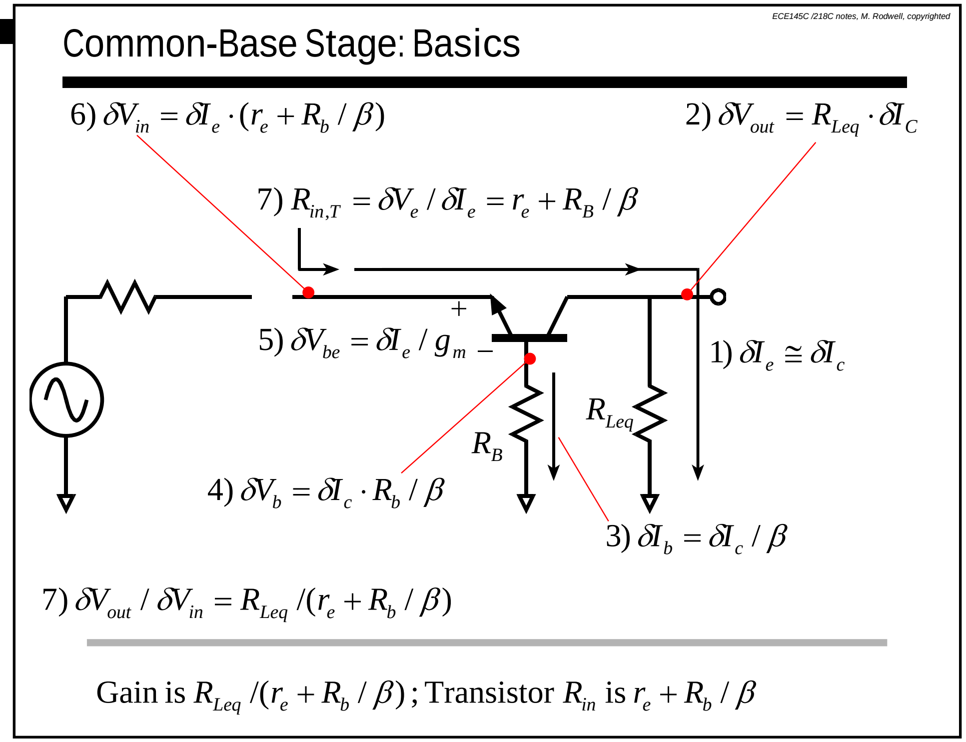
$$3)\ \delta I_b = \delta I_c/\beta$$

$$7)\ \delta V_{out}/\delta V_{in} = R_{Leq}/(r_e + R_b/\beta)$$

Gain is $R_{Leq}/(r_e + R_b/\beta)$; Transistor R_{in} is $r_e + R_b/\beta$

Emitter Follower Output Impedance



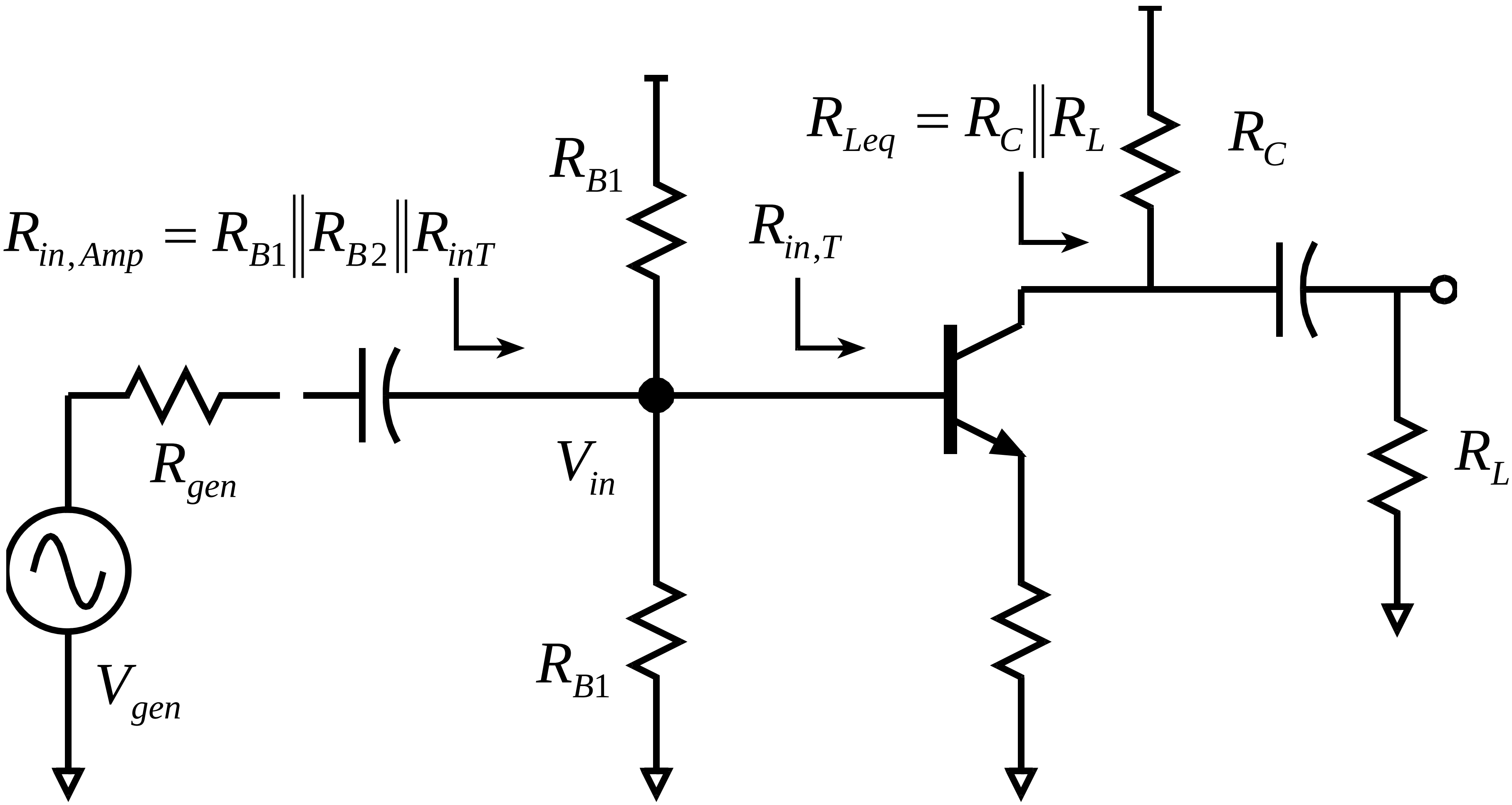


E.F. output impedance is same problem as C.B. input impedance

$$R_{out,emitter} = r_e + R_B / \beta = 1/ g_m + R_B / \beta$$

$$R_{out,amp} = R_{out,emitter} \| R_{EE}$$

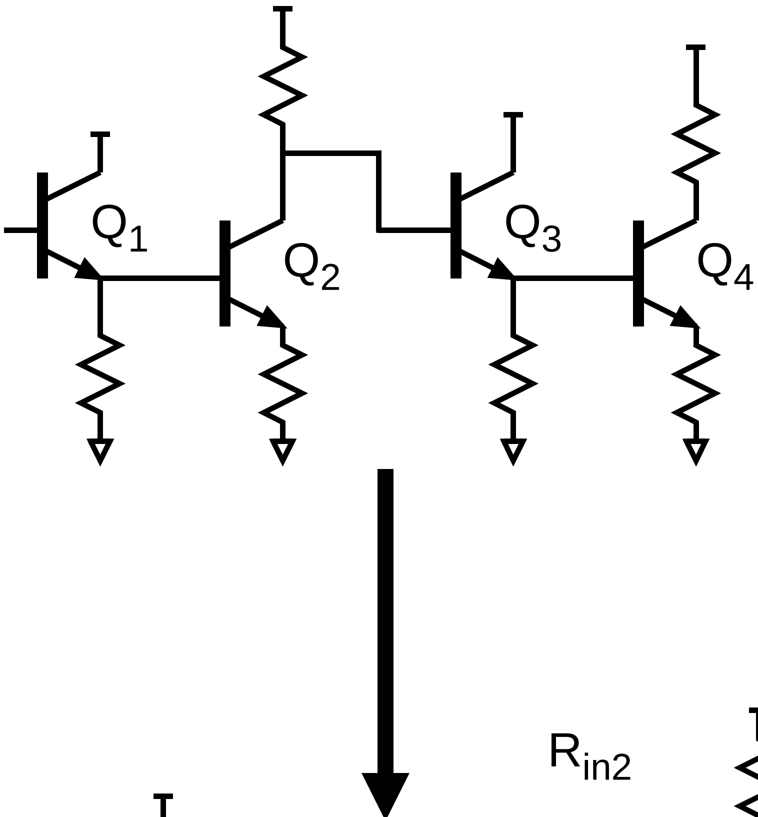
Including Bias Circuit Resistances



These are (trivially) added in parallel with the transistor terminal impedances to determine the net circuit impedances.

From which, $V_{in} / V_{gen} = R_{in,amp} / (R_{in,amp} + R_{gen})$, etc.

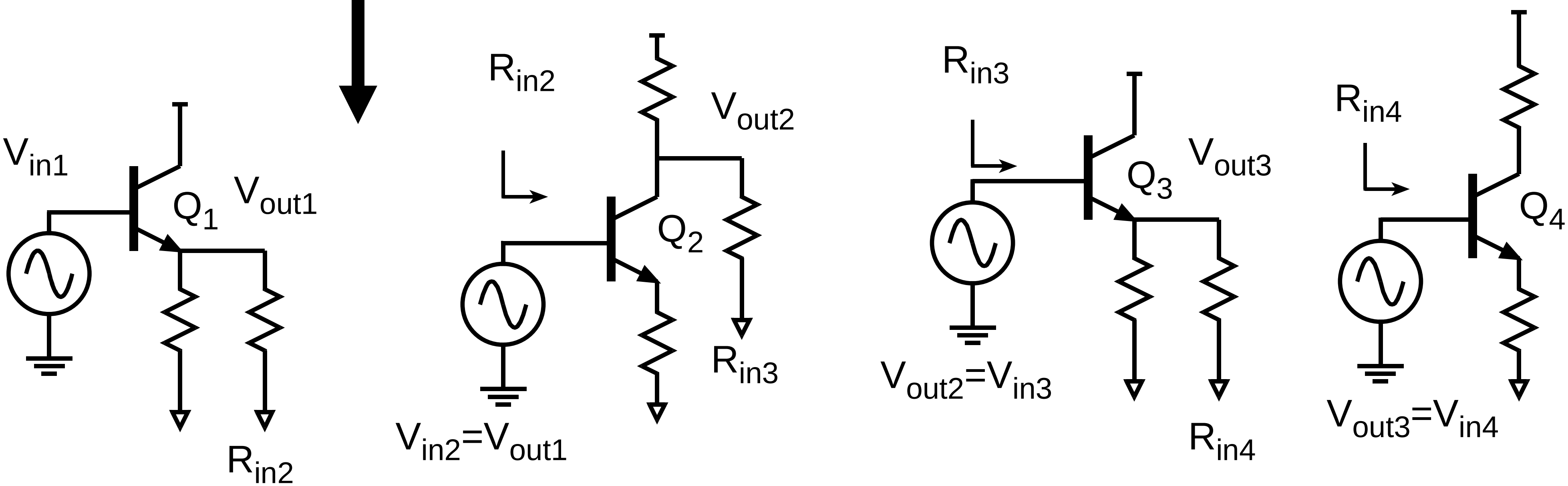
Baseband Analysis Of Multistage Circuits



For baseband analysis of multi-stage circuits, simply break into individual stages.

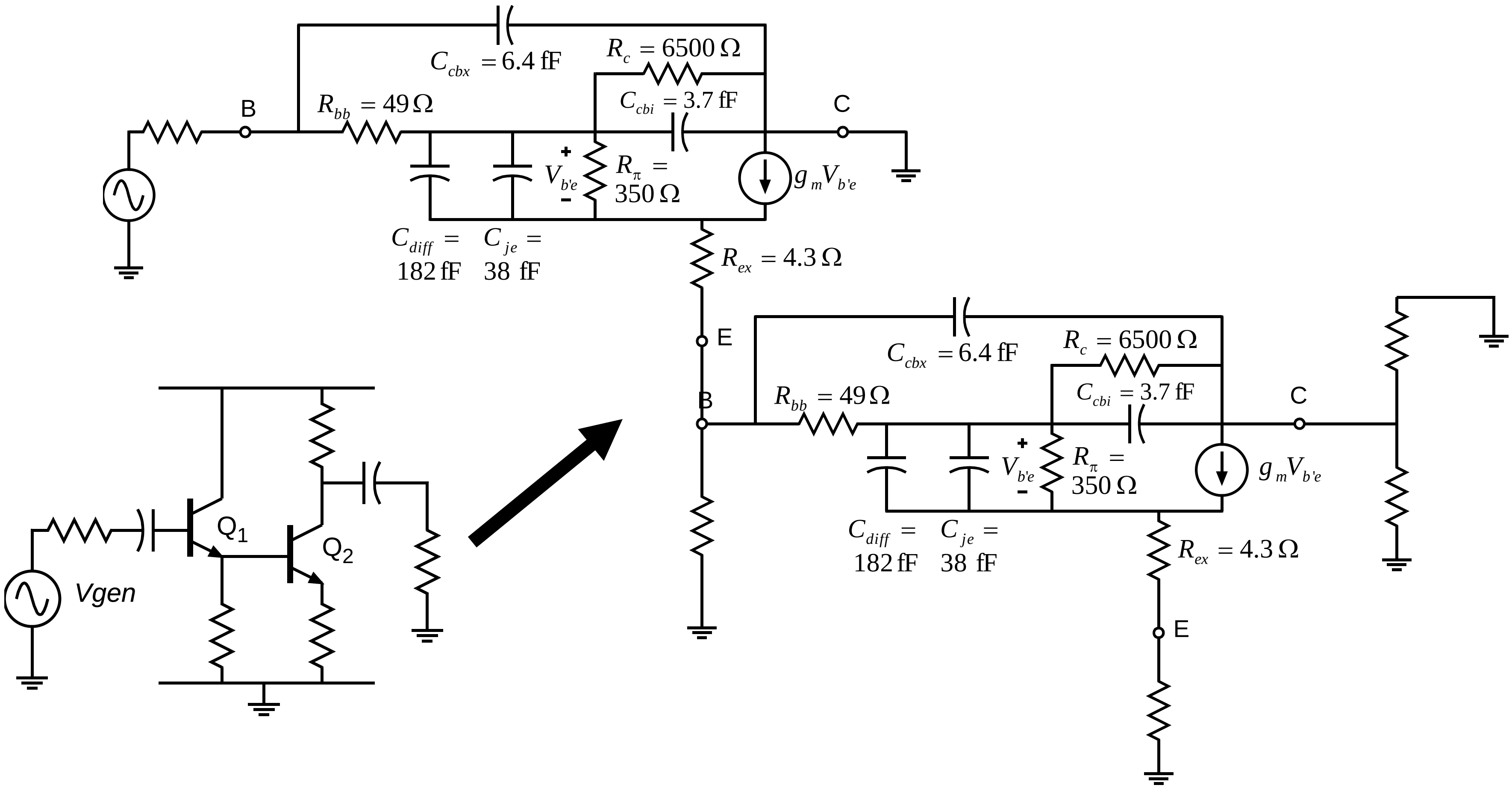
Load impedance of the Nth stage includes the input impedance of the (N+1)th stage

Analysis is then trivial...



small-signal baseband analysis

High-Frequency Analysis: The General Problem



Analyzing frequency response is difficult: cannot separate stage-by-stage

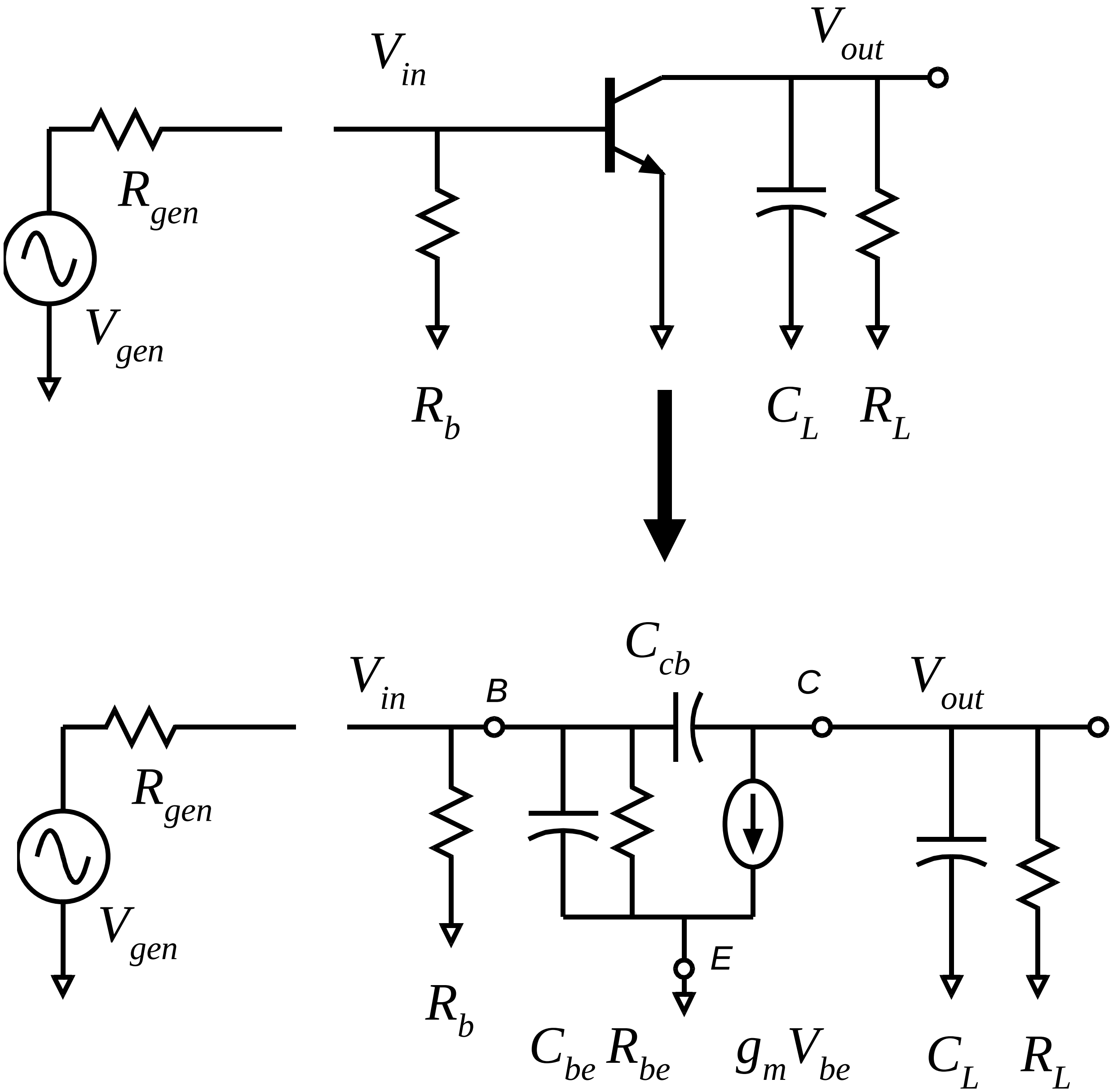
Method #1: nodal analysis: accurate, general, tedious.

Method #2: method of time constants: accurate, limited applicabilty, quick & intuitive

Nodal Analysis

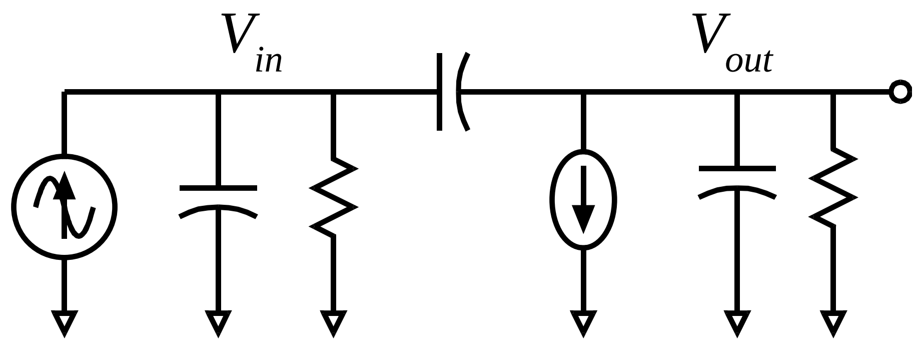
Tutorial: Transfer Function Analysis: Nodal Analysis I

Simple & very familiar example : common - emitter amplifier.



Tutorial: Transfer Function Analysis: Nodal Analysis II

Reduced circuit :



$$(R_i = R_{gen} \,||\, R_{be} \,||\, R_b)$$

$I_i = V_{gen}/R_{gen}$ C_{be} R_i $g_m V_{be}$ C_L R_L

Step 1 : Write Nodal Equations from KCL

$$\begin{bmatrix} G_i + sC_{be} + sC_{cb} & -sC_{cb} \\ g_m - sC_{cb} & G_L + sC_L + sC_{cb} \end{bmatrix} \begin{bmatrix} V_{in} \\ V_{out} \end{bmatrix} = \begin{bmatrix} I_i \\ 0 \end{bmatrix}$$

Tutorial: Transfer Function Analysis: Nodal Analysis III

Step 2 : Solve Nodal Equations :

$$V_{out} / I_{in} = N(s) / D(s)$$

$$N(s) = \begin{vmatrix} G_i + sC_{be} + sC_{cb} & 1 \\ g_m - sC_{cb} & 0 \end{vmatrix} = -(g_m - sC_{cb})$$

$$D(s) = \begin{vmatrix} G_i + sC_{be} + sC_{cb} & -sC_{cb} \\ g_m - sC_{cb} & G_L + sC_L + sC_{cb} \end{vmatrix}$$

$$D(s) = \left(G_i + sC_{be} + sC_{cb}\right)\left(G_L + sC_L + sC_{cb}\right) - \left(g_m - sC_{cb}\right)\left(-sC_{cb}\right)$$

Step 3 : Organize in powers of s

$$\begin{aligned} D(s) = {} & G_i G_L \\ & + s(G_i C_L + G_i C_{cb} + G_L C_{be} + G_L C_{cb} + g_m C_{cb} \\ & + s^2(C_{be} C_L + C_{be} C_{cb} + C_{cb} C_L + \cancel{C_{cb} C_{cb}} - \cancel{C_{cb} C_{cb}}) \end{aligned}$$

Tutorial: Transfer Function Analysis: Nodal Analysis IV

Step 4 : Separate into dimensionless ratio - of - polynomials form, separating constants and gains from the transfer function...

$$\frac{V_{out}}{I_{in}} = \frac{V_{out}}{V_{gen}/R_{gen}} = \frac{N(s)}{D(s)}$$

$$= \frac{-(g_m - sC_{cb})}{\left(\begin{array}{c} G_i G_L + s(G_i C_L + G_i C_{cb} + G_L C_{be} + G_L C_{cb} + g_m C_{cb} \\ + s^2 (C_{be} C_L + C_{be} C_{cb} + C_{cb} C_L) \end{array} \right)}$$

$$\frac{V_{out}}{V_{gen}} = \frac{-(g_m - sC_{cb}) R_i R_L / R_{gen}}{\left(\begin{array}{c} 1 + s(R_L C_L + R_L C_{cb} + R_i C_{be} + R_i C_{cb} + g_m R_i R_L C_{cb} \\ + s^2 (C_{be} C_L + C_{be} C_{cb} + C_{cb} C_L) R_i R_L \end{array} \right)}$$

Tutorial: Transfer Function Analysis: Nodal Analysis V

$$\text{note that } \frac{R_i}{R_{gen}} = \frac{(R_{be} \| R_b \| R_{gen})}{R_{gen}} = \frac{(R_{be} \| R_b)}{(R_{be} \| R_b) + R_{gen}} = \frac{R_{in,Amp}}{R_{in,Amp} + R_{gen}}$$

so...

$$\frac{V_{out}}{V_{gen}} = \left(\frac{R_{in,Amp}}{R_{in,Amp} + R_{gen}} \right) (-g_m R_L)$$

$$\times \frac{-(1 - sC_{cb} / g_m)}{\left(\begin{array}{c} 1 + s(R_L C_L + R_L C_{cb} + R_i C_{be} + R_i C_{cb} + g_m R_i R_L C_{cb}) \\ + s^2 (C_{be} C_L + C_{be} C_{cb} + C_{cb} C_L) R_i R_L \end{array} \right)}$$

b_1

a_1

a_2

$$\Rightarrow \frac{V_{out}(s)}{V_{gen}(s)} = \left. \frac{V_{out}}{V_{gen}} \right|_{mid-band} \frac{1 + b_1 s}{1 + a_1 s + a_2 s^2}$$

Tutorial: Transfer Function Analysis: Nodal Analysis VI

Step 5 : Find the roots (poles & zeros) of the polynomial

$$\frac{V_{out}(s)}{V_{gen}(s)} = \left.\frac{V_{out}}{V_{gen}}\right|_{mid-band} \frac{1+b_1 s}{1+a_1 s+a_2 s^2} = \left.\frac{V_{out}}{V_{gen}}\right|_{mid-band} \frac{1+b_1 s}{(1-s/s_{p1})(1-s/s_{p2})}$$

what are efficient methods of finding the poles ?

Finding Poles
from Transfer Functions

Finding Poles and Zeros

Ratio - of - Polynomial Form :

$$\frac{V_{out}(s)}{V_{gen}(s)} = \left.\frac{V_{out}}{V_{gen}}\right|_{\text{at mid-band}} * s^m \frac{1 + b_1 s + b_2 s^2 + \ldots}{1 + a_1 s + a_2 s^2 + \ldots}$$

Poles and Zeros :

$$\frac{V_{out}(s)}{V_{gen}(s)} = \left.\frac{V_{out}}{V_{gen}}\right|_{\text{at mid-band}} * s^m \frac{(1 - s/s_{z1})(1 - s/s_{z1})(1 - s/s_{z1})\ldots}{(1 - s/s_{p1})(1 - s/s_{p1})(1 - s/s_{p1})\ldots}$$

Finding Poles: Complex Poles

$$\frac{V_{out}}{V_{gen}} = k\frac{1+b_1 s+b_2 s^2+\ldots}{1+a_1 s+a_2 s^2+a_3 s^3}$$

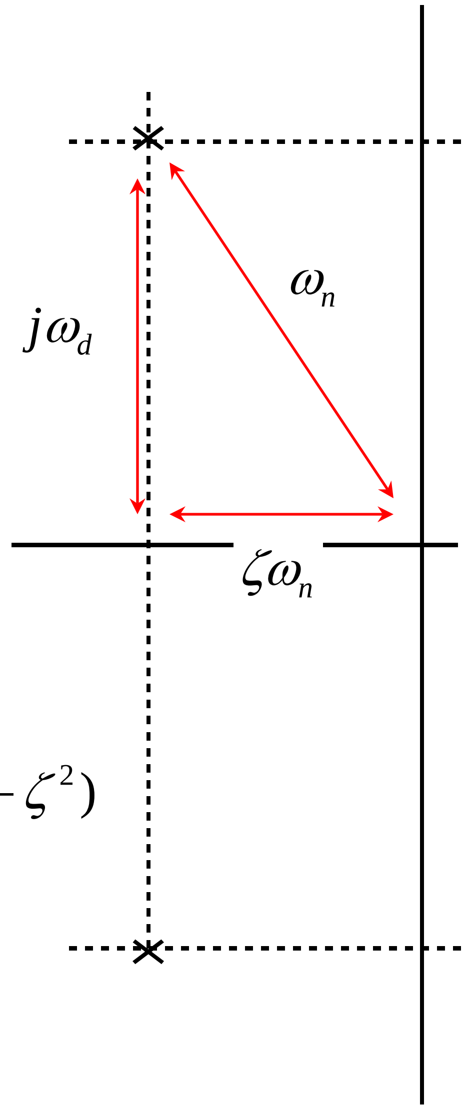
If $a_3/a_2 << a_2$ then we can ignore the s^3 at moderate frequencies and

$$\frac{V_{out}}{V_{gen}} \approx k\left(\frac{1+b_1 s+b_2 s^2+\ldots}{1+a_1 s+a_2 s^2}\right)$$

If the roots of this are complex, then

$$\frac{V_{out}}{V_{gen}} = k\left(\frac{1+b_1 s+b_2 s^2+\ldots}{1+a_1 s+a_2 s^2}\right) = k\left(\frac{1+b_1 s+b_2 s^2+\ldots}{1+(2\zeta/\omega_n)s+s^2/\omega_n^2}\right)$$

$$\frac{V_{out}}{V_{gen}} = k\left(\frac{1+b_1 s+b_2 s^2+\ldots}{\left(1-\dfrac{s}{-\zeta\omega_n+j\omega_d}\right)\left(1-\dfrac{s}{-\zeta\omega_n-j\omega_d}\right)}\right)$$



$$\omega_d^2 = \omega_n^2(1-\zeta^2)$$

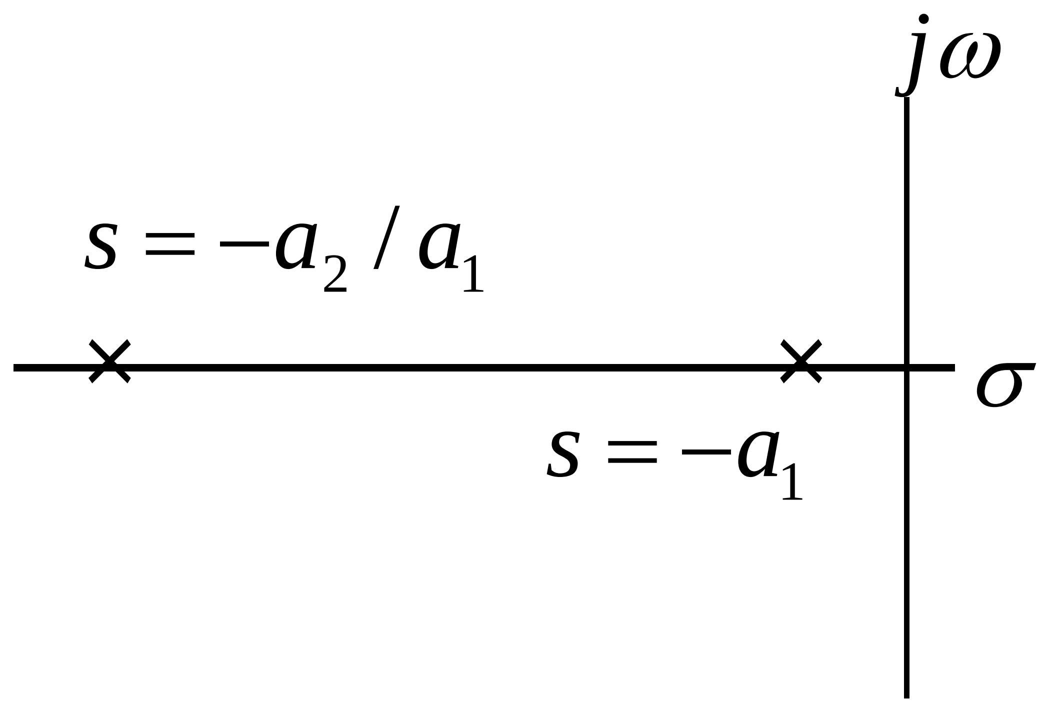
Finding Poles: Separated Pole Approximation

If the roots are widely separated

e.g. $(a_2/a_1) << a_1$, then

$$\frac{V_{out}}{I_{in}} = k\left(\frac{1 + b_1 s + b_2 s^2 + \ldots}{1 + a_1 s + a_2 s^2}\right)$$

$$\frac{V_{out}}{I_{in}} \cong k\,\frac{1 + b_1 s + b_2 s^2 + \ldots}{(1 + a_1 s)\left(1 + \left(\dfrac{a_2}{a_1}\right)s\right)}$$

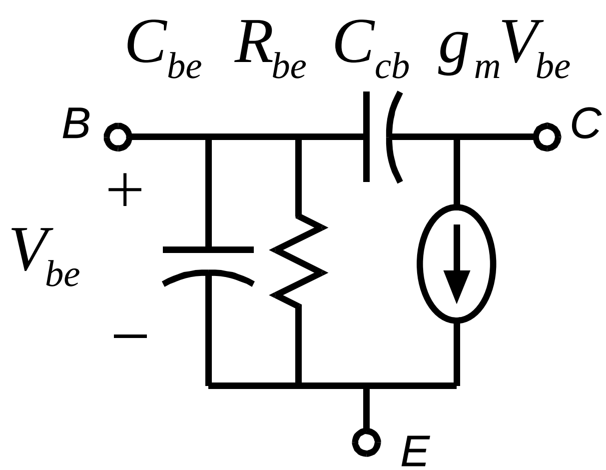


a_1 is the dominant pole.

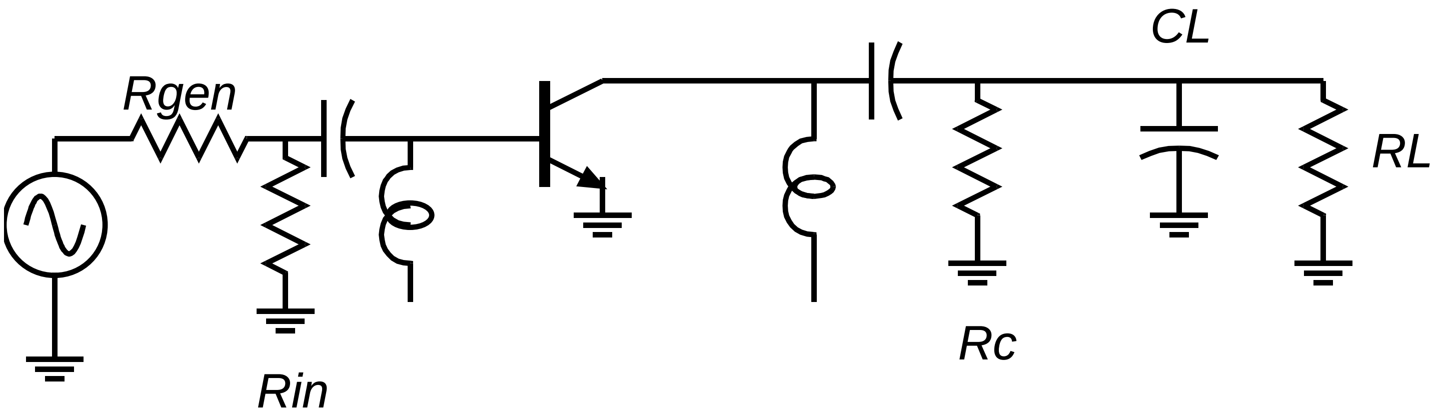
Introductory Circuit Design: summary

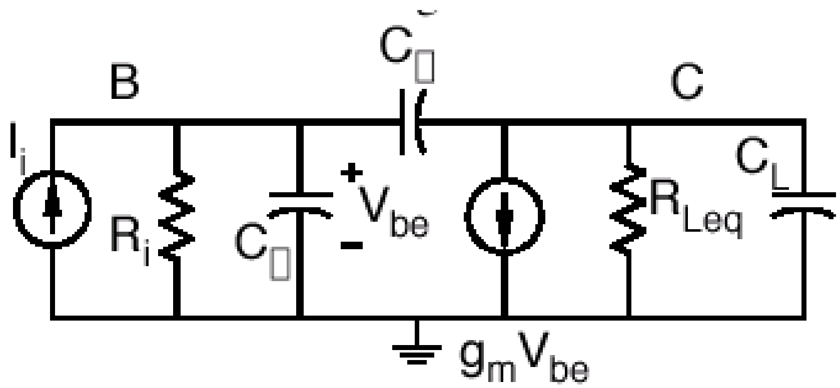
Gain Stages: Elementary Bandwidth Analysis

Using the oversimplified device model below, with Cpi denoting the sum of base-emitter depletion and diffusion capacitances, bandwidth of CE/CB/CC stages can be found….



CE Stage: Elementary Bandwidth Analysis





$$V_{out}/V_{gen} = \left(V_{out}/V_{gen}\right)_{MB} \frac{1+s\tau_{zero}}{1+a_1 s + a_2 s^2}$$

$$a_1 = R_i\left(C_\pi + C_\mu\left(1+g_m R_{Leq}\right)\right) + R_{Leq}\left(C_\mu + C_L\right)$$

$$a_2 = R_i R_{Leq}\left(C_\mu C_L + C_\mu C_\pi + C_\pi C_L\right)$$

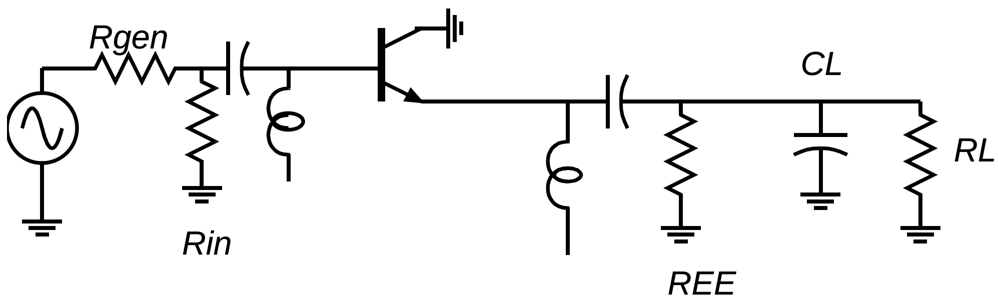
$$\tau_{zero} = -C_\mu / g_m$$

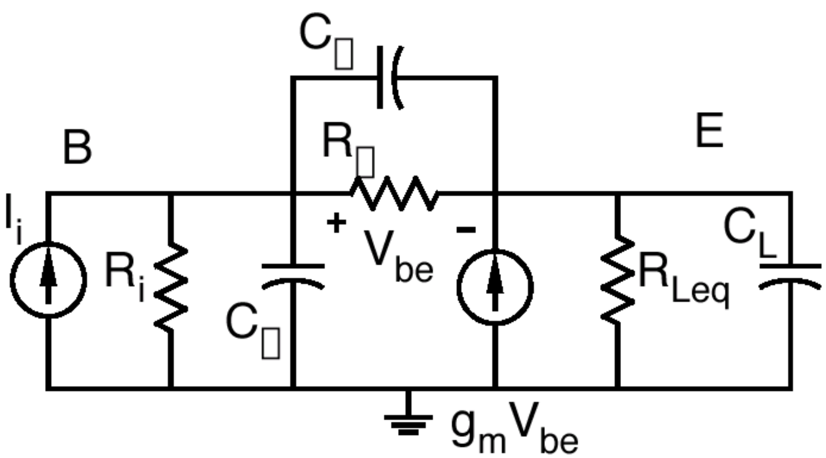
Ri is the parallel combination of Rgen, Rin, and Rpi

RLeq is the parallel combination of RL, Rc, and Ro

Note in the dominant pole (a1) the miller-multiplication of the collector base capacitance

CC Stage: Elementary Bandwidth Analysis





$$V_{out}/V_{gen} = \left(V_{out}/V_{gen}\right)_{MB} \frac{1 + s\tau_{zero}}{1 + a_1 s + a_2 s^2}$$

given that $A_{vmb} = \left(r_e / \left(r_e + R_{Leq}\right)\right)$:

$$a_1 = C_\pi\left(R_\pi \| \left(r_e \| R_{Leq} + R_i\left(1 - A_{vmb}\right)\right)\right)$$

$$+ C_\mu\left(R_i \| \text{transistor input resistance}\right)$$

$$+ C_L\left(R_{Leq} \| \text{transistor output resistance}\right)$$

$$a_2 = \left(R_i \| \text{transistor input resistance}\right)\left(R_{Leq} \| r_e\right)$$

$$\times\left(C_\mu C_\pi + C_\mu C_L + C_L C_\pi\right)$$

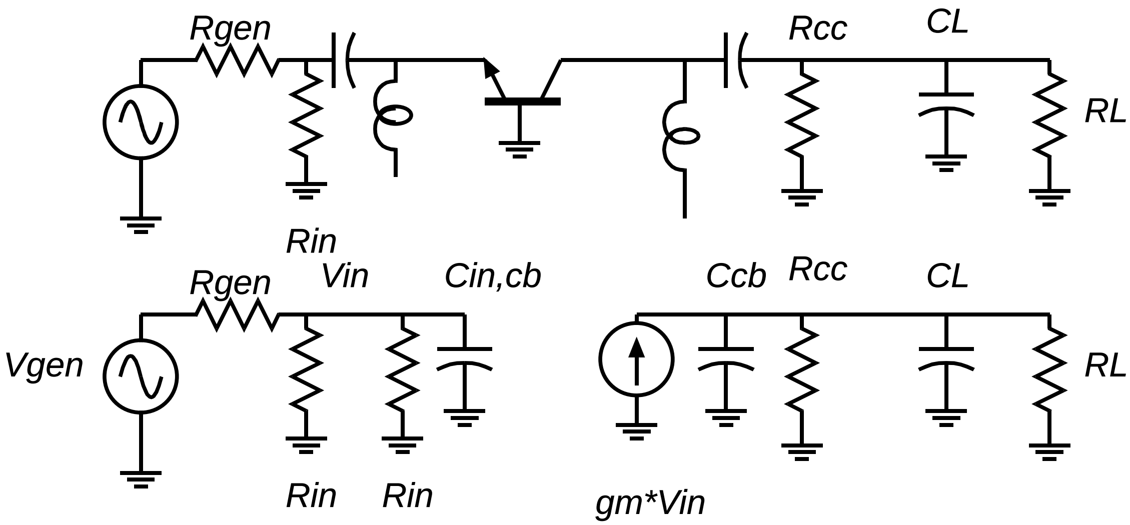
$$\tau_{zero} = g_m / C_\pi$$

Ri is the parallel combination of Rgen, and Rin,

RLeq is the parallel combination of Ree and RL

Note that the frequency response is a mess. Given CL, the transfer function very often has complex poles, and may show strong gain peaking, hence ringing in the pulse response.

CB Stage: Elementary Bandwidth Analysis



$$C_{in,cb} = C_{je} + g_m \tau_b$$

$$g_m(j\omega) = \frac{qI/kT}{1 + j\omega\tau_c}$$

Here we have a problem. To the extent that the CB stage is modeled by a very very simple hybrid-pi model (explicitly, with zero Rbb), we find (by very simple analysis) very high bandwidth, with poles having time constants equal to tau_b, to tau_c, and to the product of the load resistance times (Ccb+CL).

Note that
1) Input capacitance is indeed as noted. Does not include effect of tau_c

2) Ignoring Rbb in CB stage analysis, while appealing for simplicity (e.g. undergrad classes) is quite unreasonable, as CcbRbb often dominates high frequency rolloff. More regarding this later.

Method of
Time Constants

make revision for 2008----first before MOTC, give by summary without derivation the standard stage expressions.

then define MOTC, first and second order
then show a 1-stage Darlington diff amp, and say caps to ground, caps between inputs and outputs.

Give expression for caps to ground
Give expression for caps between in and out of general block

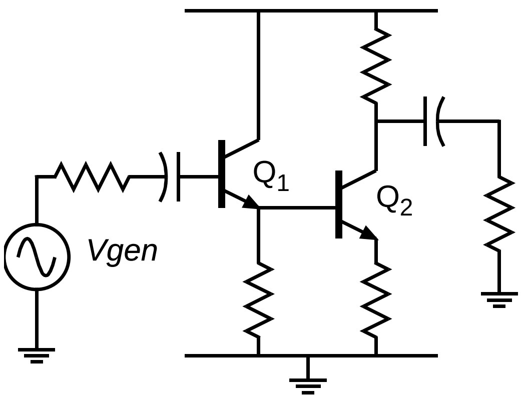
then use this for CD stage   Cgs only
then use this for CC stage Cbe only
then do for CE stage Ccb only

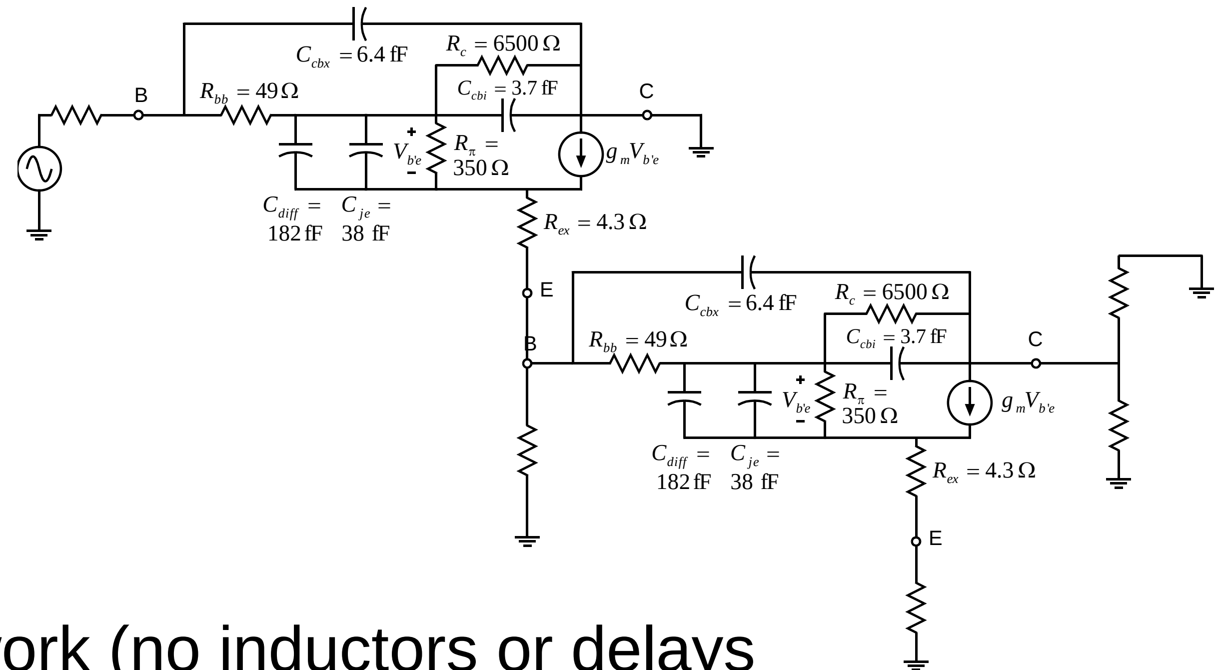
then work the full Darlington diff amp

then show how CE (with degen) CB CC are same problem

then re-show stage relationship

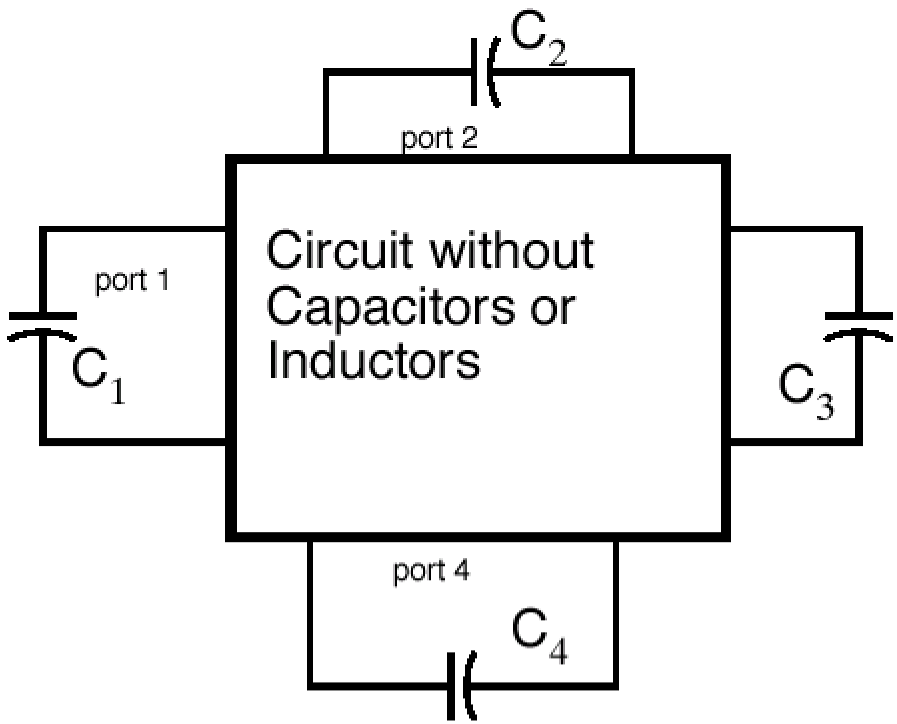
Finding Bandwidth: Method of Time Constants





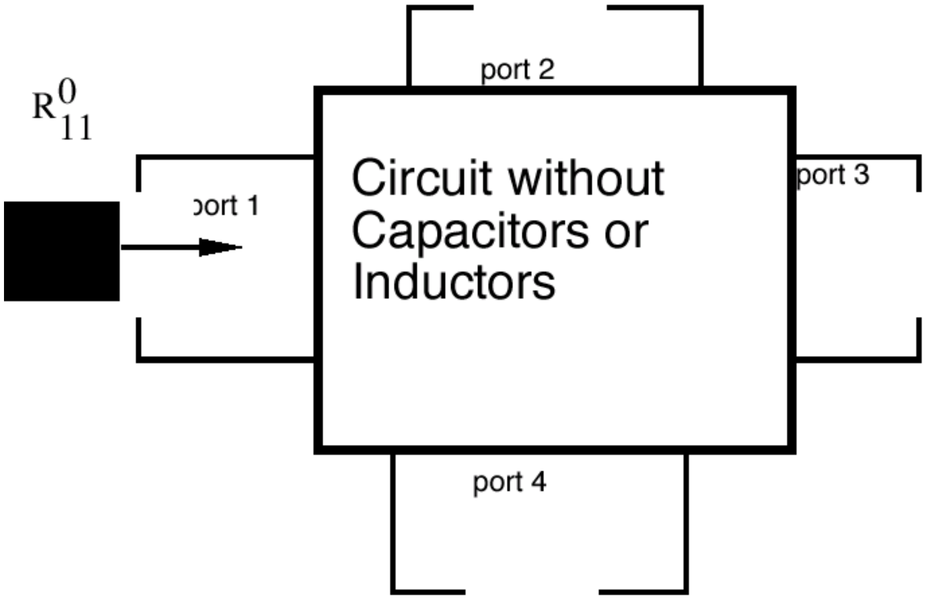
take a general RC network (no inductors or delays tau), and separate into 2 parts, network without capacitors, and the capacitors:

MOTC: Separation into Capacitors & Resistive N-port



The internal capacitor-free network is now frequency-independent. The MOTC method (not proven here) relies on results from n-port network theory

MOTC: Open-Circuit Resistances



work examples to illustrate this

R_{11}^0 is the small signal resistance measured at port one with all other ports open - circuited. This is determined by applying a test voltage (or current) at the port and computing from this the resulting current (or voltage)

MOTC: the Dominant Time Constant

$$\frac{V_{out}}{V_{gen}} = \left(\frac{V_{out}}{V_{gen}}\right)_{mb} \frac{1 + b_1 s + b_2 s^2 + \cdots}{1 + a_1 s + a_2 s^2 + \cdots}$$

$$a_1 = R_{11}^0 C_1 + R_{22}^0 C_2 + R_{33}^0 C_3 + R_{44}^0 C_4$$

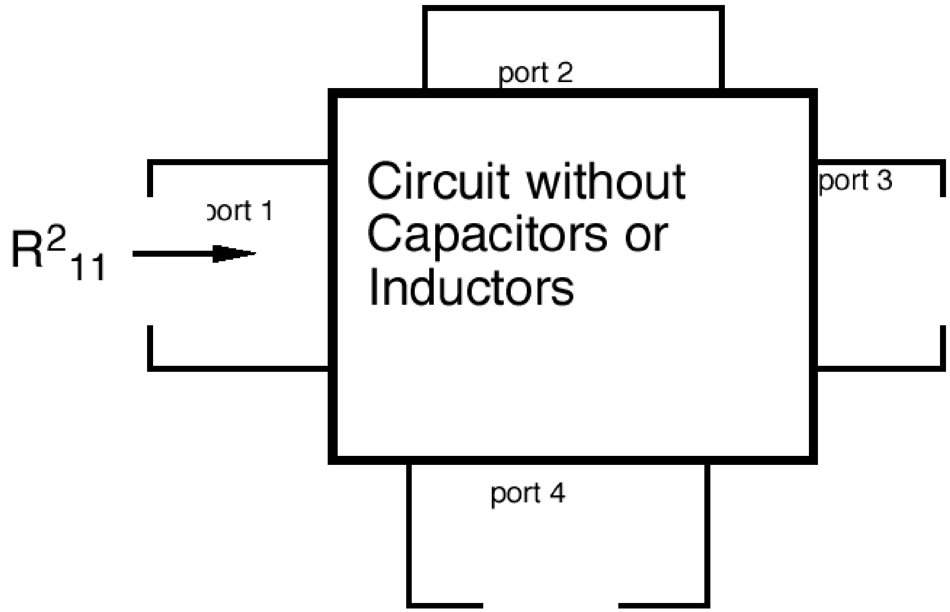
The MOTC first-order time constants directly give us the dominant time constant a_1 of the circuit. If (and only if) the secondary time constant a_2 is negligible, the 3-dB bandwidth is $1/2\pi a_1$. We must use the second-order (short-circuit) time constants to determine a_2.

MOTC: Are We Saving Any Work ?

Are we saving work relative to brute-force nodal analysis: MOTC would be of only moderate value if we had to calculate all the Ri's each time. Fortunately, most terms involve quantities ***already found in midband stage analysis: input and output impedances, load impedances, etc.***

work examples to illustrate this

MOTC: Short-Circuit Resistances



R_{11}^{2} is the small signal resistance measured at port one with all other ports open-circuited, except for port 2, which is shorted

MOTC: The Second-Order Time-Constant

$$\frac{V_{out}}{V_{gen}} = \left(\frac{V_{out}}{V_{gen}}\right)_{mb} \frac{1 + b_1 s + b_2 s^2 + \cdots}{1 + a_1 s + a_2 s^2 + \cdots}$$

$$a_2 = R_{11}^0 R_{22}^1 C_1 C_2 + R_{11}^0 R_{33}^1 C_1 C_3 + R_{11}^0 R_{44}^1 C_1 C_4$$
$$+ R_{22}^0 R_{33}^2 C_2 C_3 + R_{22}^0 R_{44}^2 C_2 C_4 + R_{33}^0 R_{44}^3 C_3 C_4$$

notethat $R_{xx}^0 R_{yy}^x = R_{xx}^y R_{yy}^0$

MOTC: An Example

work example…second order terms in either CE stage or CC stage….

MOTC: Working these Efficiently

Because $R_{xx}^{y} R_{yy}^{0} = R_{xx}^{0} R_{yy}^{x}$, we always have 2 choices in finding each term in the MOTC. The trick is to work the problem so that as much as possible:

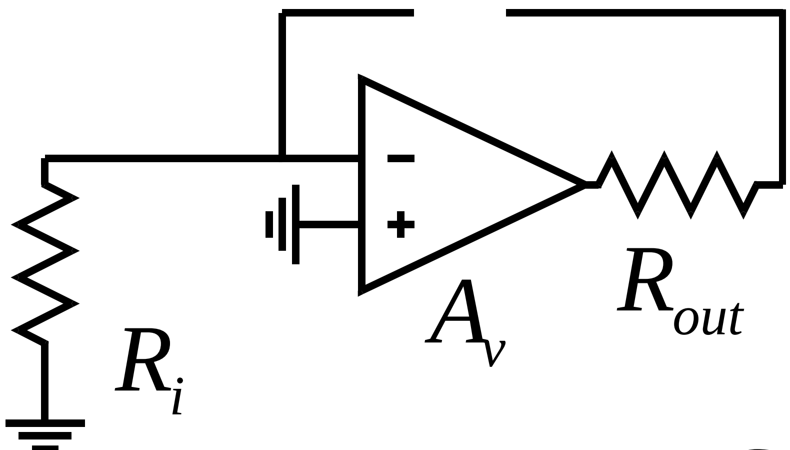
1) terms are related to input, ouput, load impedances
2) terms are ones found earlier, in a_1 analysis.

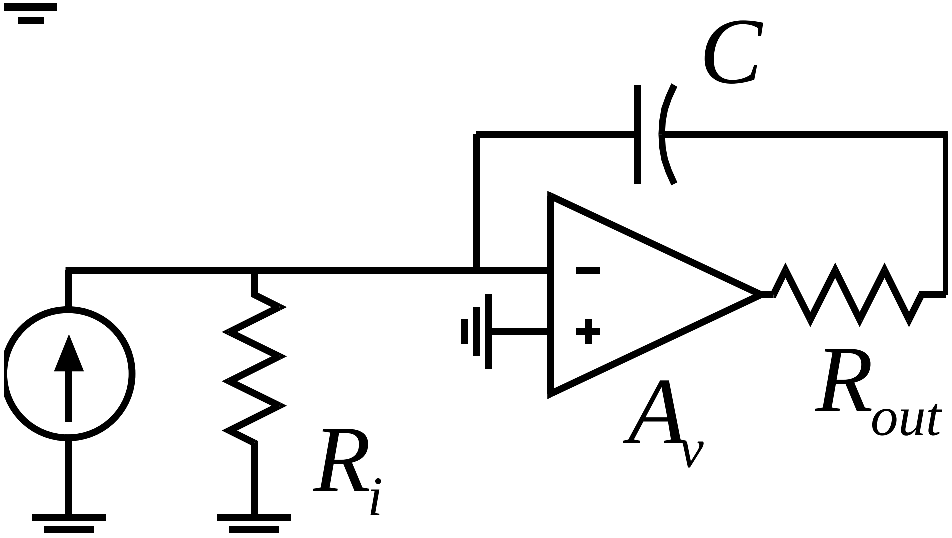
There are 2 "funny" cases which arise so often that I will give them on the next 2 pages (note these are intimately related to the well-known Miller effect)

MOTC and the Miller Effect

derive

$$R_{xx}^{y} = R_i(1+A_v) + R_{out}$$

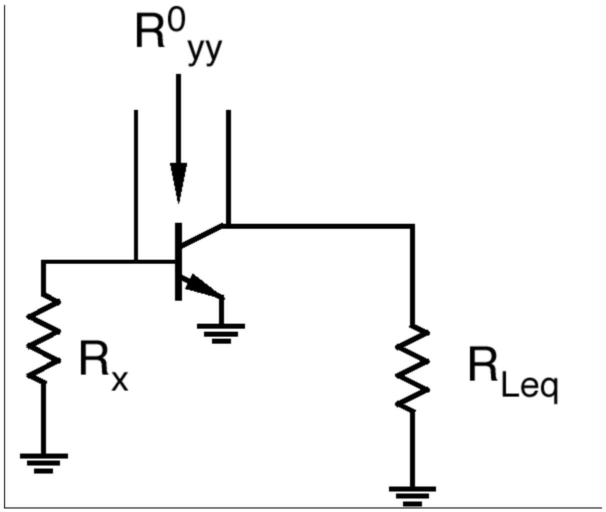




$$a_1 = \tau = \left[R_i(1+A_v) + R_{out}\right] \bullet C$$

MOTC: port impedances between collector and base

derive



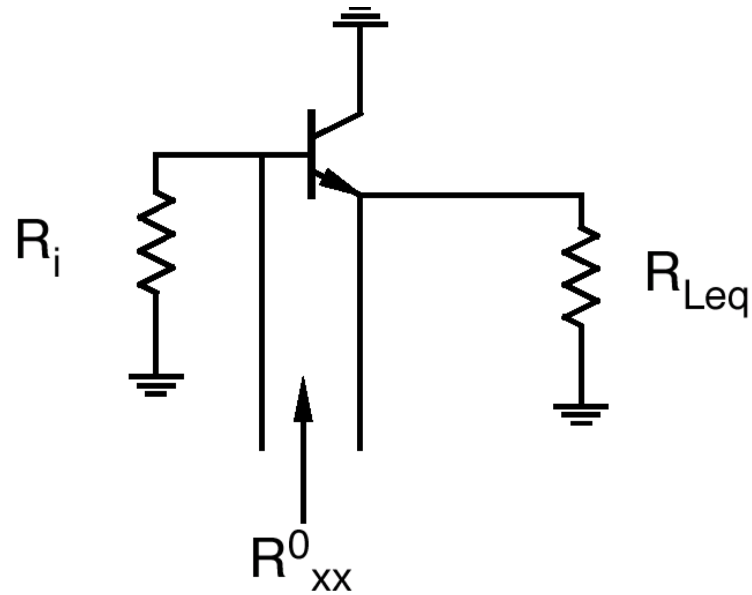
If we decide explicitly that R_x is to denote the parallel combination of any external circuit resistances and R_{be}, and that R_{Leq} similarly denotes the combined effect of external resistors and R_{ce}, then

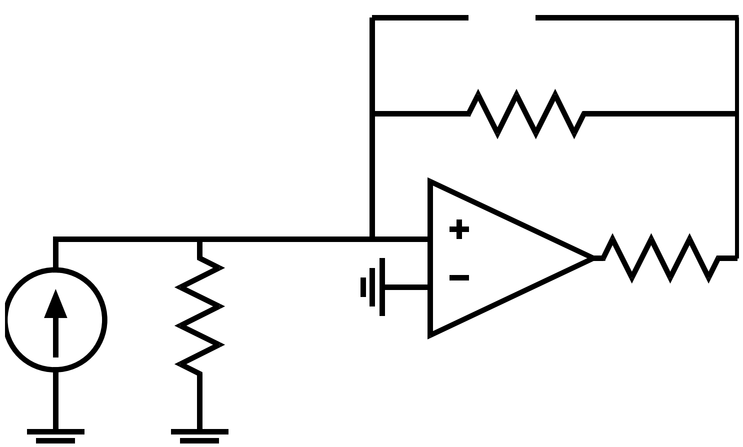
$$R_{yy}^0 = R_x(1+g_m R_{Leq}) + R_{Leq}$$

MOTC: Port Impedances Between Emitter & Base

$$R_{xx}^{0} = R_{\pi} \| \left(r_e \| R_{Leq} + R_i \left(1 - A_{vmb} \right) \right)$$

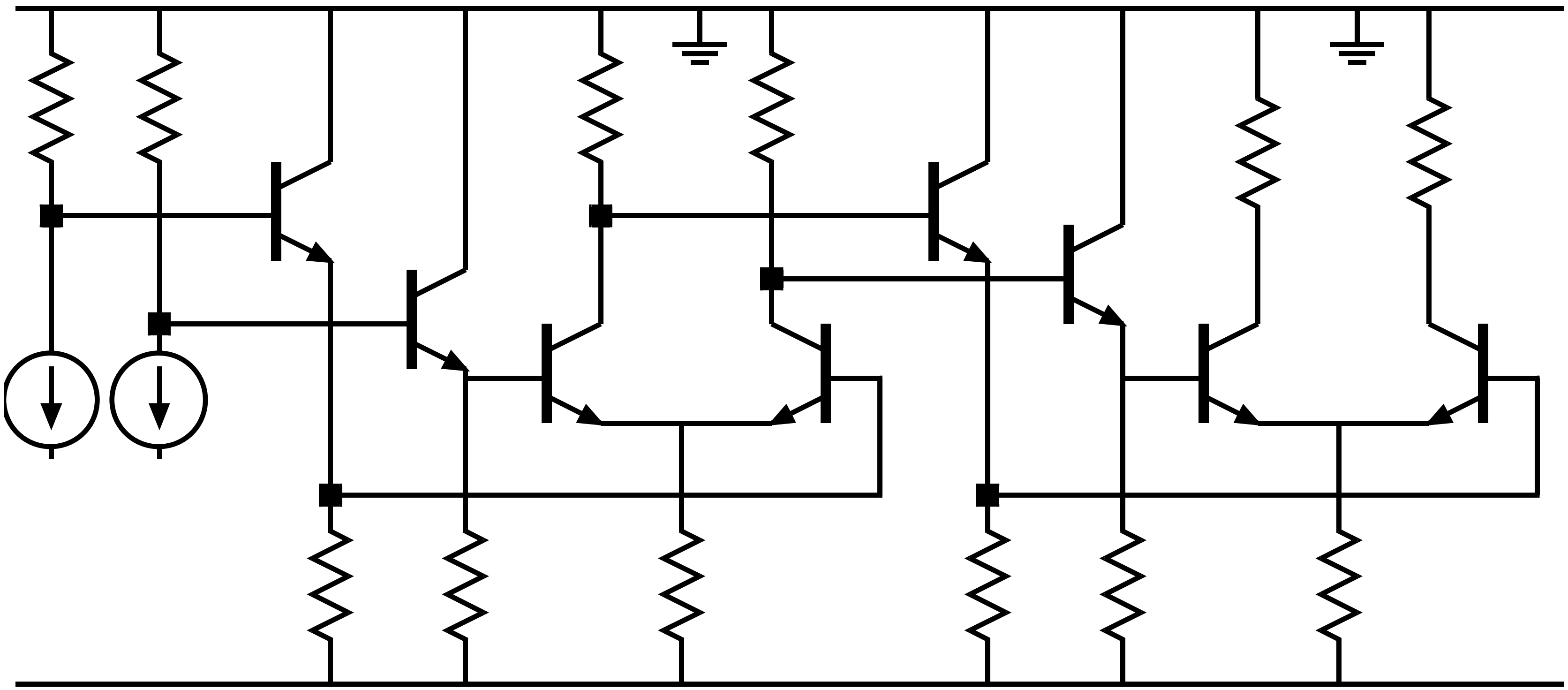
$$A_{vmb} = \left(R_{Leq} / \left(r_e + R_{Leq} \right) \right)$$



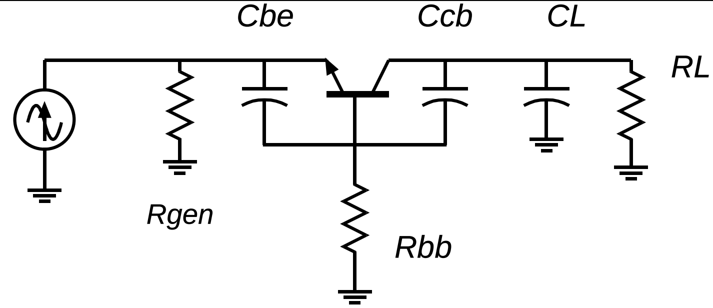


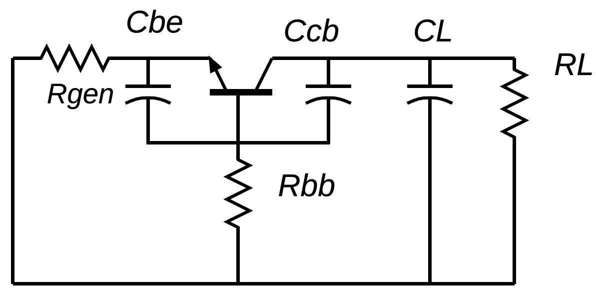
MOTC: Multistage Example

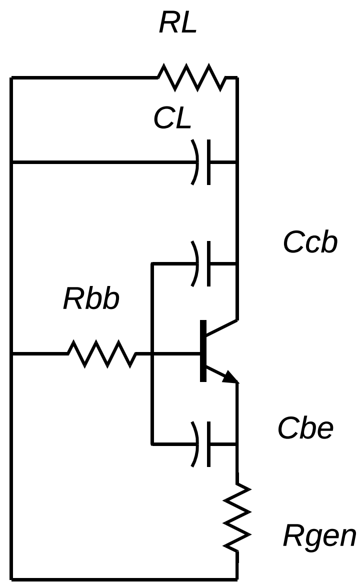
work on the board...



Common-base stage by MOTC







$$a_1 = C_{be}\left(\left(R_{bb}\left(1-\frac{R_{gen}}{R_{gen}+r_e}\right)+r_e \| r_{gen}\right)\middle\| r_{be}\right)$$

$$+C_{cb}\left(R_{bb}\left(1+\frac{R_L}{r_e+R_{gen}}\right)+R_L\right)+C_L R_L$$

$$a_2 = \ldots$$

note that because a_1, a_2 are independent of location of input and output, the form is identical to that of CE stage.

Note also the Miller multiplication effect with $R_{bb}C_{cb}$

What's in next lecture ?

Relating amplifier gains to S-parameters
Cascaded common-emitter amplifiers,
gain-bandwidth and ft limits
Resistive feedback amplifiers for higher bandwidths
The Cherry-Hooper (transcondcuctand-transimpedance) design
Darlington stages, benefits, limits, and headaches
Ft-doubler stages
Distributed amplifiers (breifly)

And later: input tuning for (1) improving S11, S22 and (2) improving bandwidth.

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End