High Speed Mixed Signal IC Design notes set 9

ICs for Optical Transmission

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ICs for Optical Transmission: topics

Systems:

block diagrams, eye diagrams, waveforms

Transmitters:

Laser diodes, diode drivers

Optical modulators, modulator drivers

Receivers

Photodiodes

Receiver block diagrams: AGC and limiting

AGC amplifier and detector,

SNR constraints on limiting amplifier design

Limiting amplifiers

TIA: SNR analysis, topologies

DC restoration loops

SNR analysis; Personik Integrals

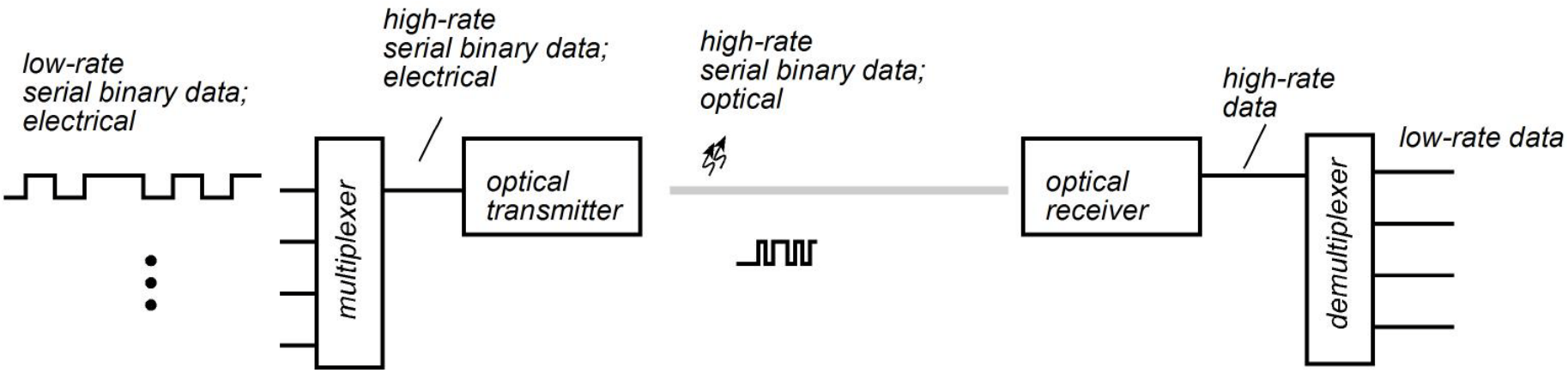
Timing recovery

PLLs, phase detectors for data steams, frequency locking

Mux and Demux

basic structures, timing thereof

Digital Optical Fiber Links



Typical form of optical link : mux, transmitter, receiver, demux

Motivation :

Copper wires have high losses at high frequencies (see notes; skin effect)

Optical fibers have low losses (~ 0.3 dB/km @1310 nm, 0.17 dB/km @1550 nm)

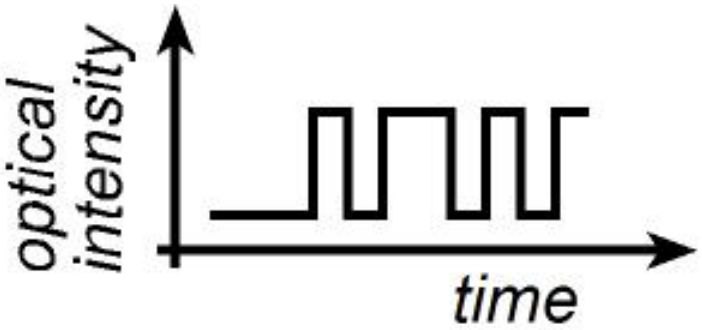
Prevalent Mode of operation (2008) :

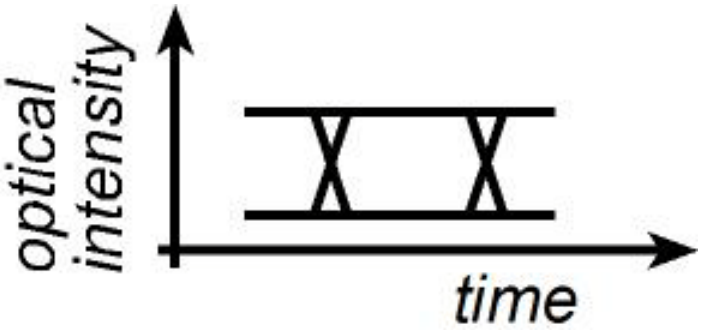
Digital transmission

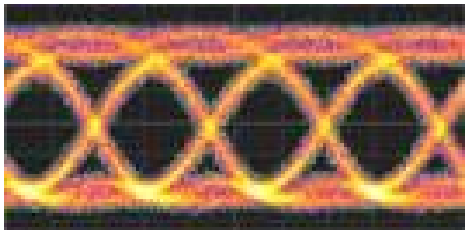
Binary Intensity Modulation (On/Off)

Incoherent (power) detection

Typical Signal Format: NRZ Modulation







In each bit period,

Intensity is modulated high / low to communicate 1 vs 0 sent.

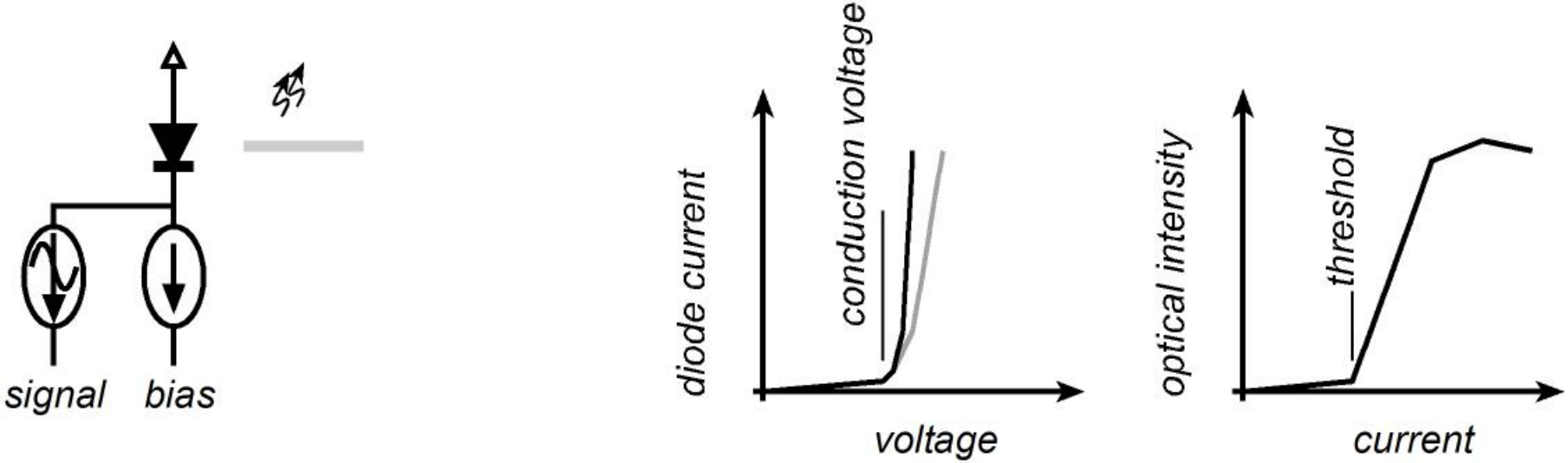
Modulated intensity for "0" is not quite zero

Extinction ratio = $P_{\text{optical,1}} / P_{\text{optical,0}}$

Eye pattern represents waveform vs. time modulo one bit period.

Represents data trajectories for all possible sequences

Optical Transmitter: Directly Modulated Laser Diode



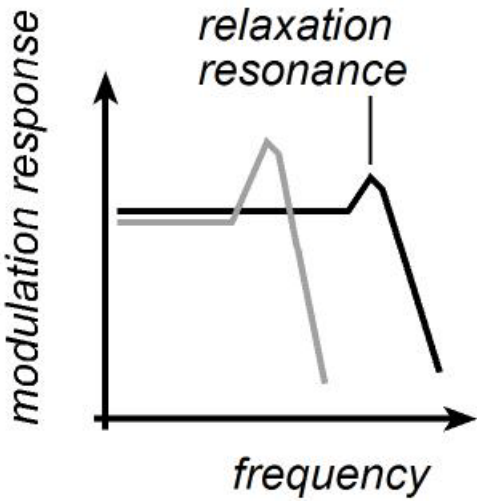
Diode is driven by superposition of bias and AC drive current.

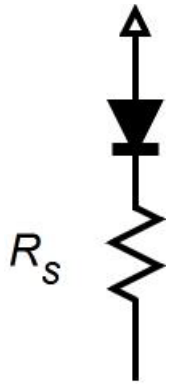
Diode shows a sharp increase in light output when drive current exceeds laser threshold : $P_{optical} \cong \eta(h\nu / q)(I - I_{th})$

η = quantum efficiency, ν = optical frequency in Hz

Laser diode I - V characteristics resemble those of a PN diode, except that forward voltage increases only slowly once threshold current is exceeded.

Laser Diode Characteristics





Laser small - signal modulation reponse depends upon bias current.

Bandwidth increases as bias current increases - - - then saturates, collapses.

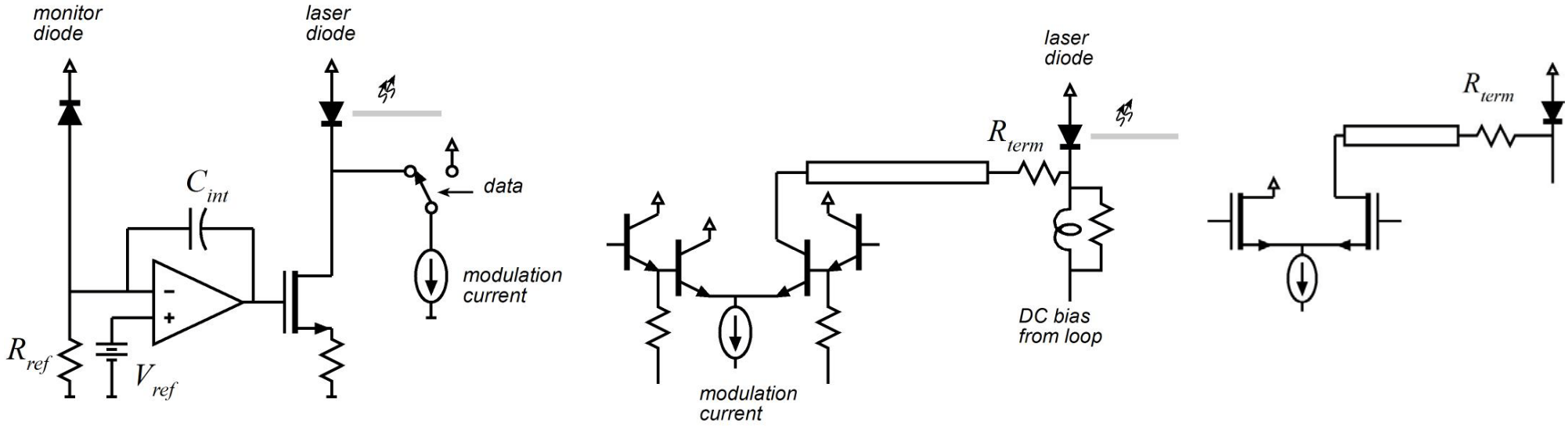
Response is 2nd - order; damping increases at high currents.

Few diode lasers exceed 25 GHz bandwidth (2008).

Undesired wavelength modulation (chirp) makes lasers less attractive for long - range high - speed links.

Though laser rate equations suggest a more complex model, laser electrical parameters are well - approximated by an ideal diode in series with a small (~ 5 - 10 Ω) series resistance.

Laser Transmitters



Basic Form; sometimes uses DC feedback loop to maintain laser bias.

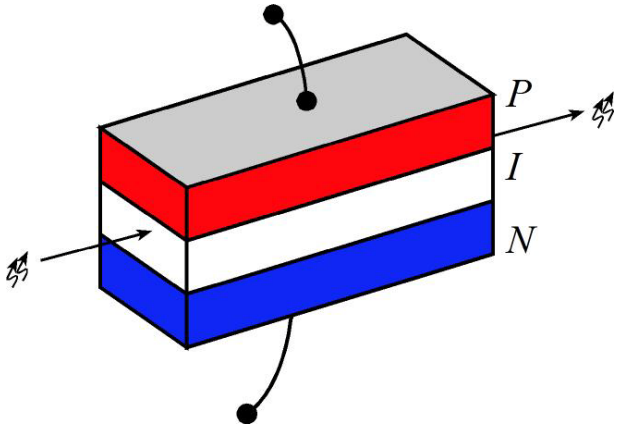
Monitor diode generally on laser backside.

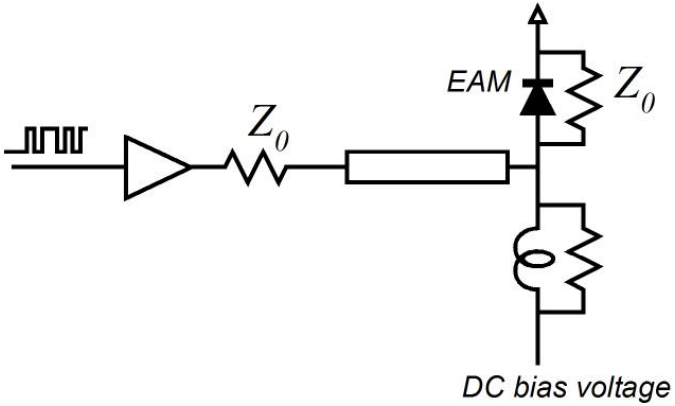
DC loops not needed with modern low threshold lasers

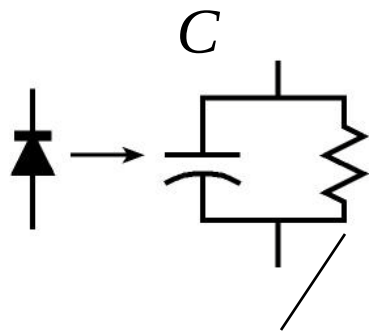
Laser & driver are not on same die.

Interconnect is likely long and likely needs series padding ($R_{term} + R_{diode} = Z_0$) to control line ringing.

Optical Modulators: EAMs





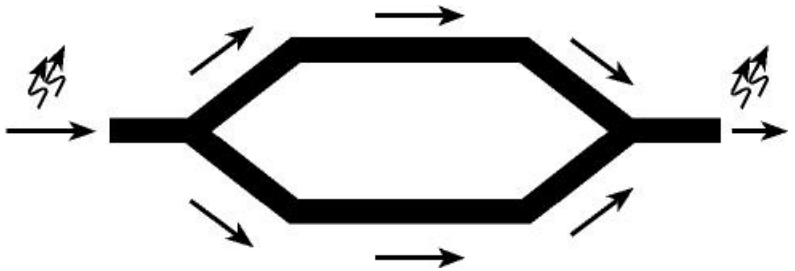


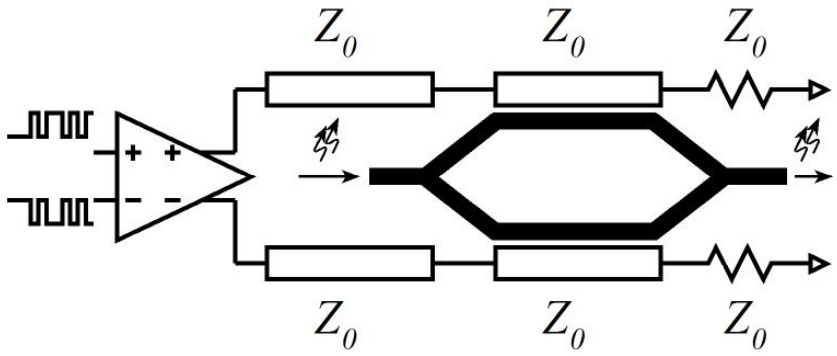
$$1/R = \frac{q}{h\nu}\frac{dP_{absorbed}}{dV_{control}}$$

Electro - Absorbion modulators : A reverse - biased PIN junction containing an optical waveguide in the I region. Varying the reverse bias varies the optical attenuation. Electrical model is that of a reverse - biased diode, but with a parallel resistance representing the absorbed light.

Device is loaded with a 50 Ohm parallel load,
and driven with combined DC bias and pulse train.

Optical Modulators: Electo-optic Modulators





Interferometer :

split optical waveguide, give paths a relative phase shift, recombine.

Output optical E - field intensity : $E_{out} = E_o \cos(\Delta\phi)$

Output optical power ($P_{out} \propto E_{out}^2$); $P_{out} = P_{in} \cos^2(\Delta\phi) = (P_{in}/2)\left[1 + \cos(2\Delta\phi)\right]$

Electro - optic Modulator :

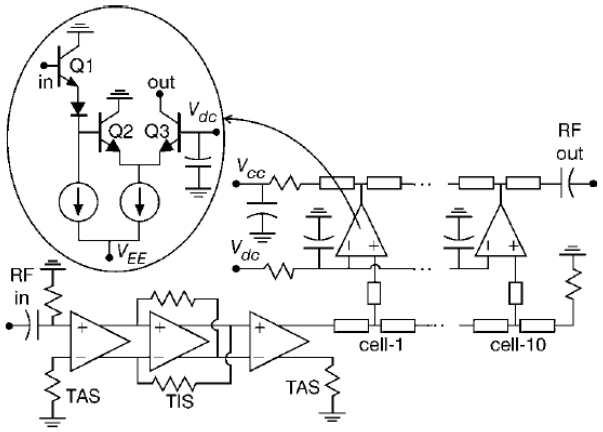
Optical waveguide refractive index varies weakly with applied E - field.

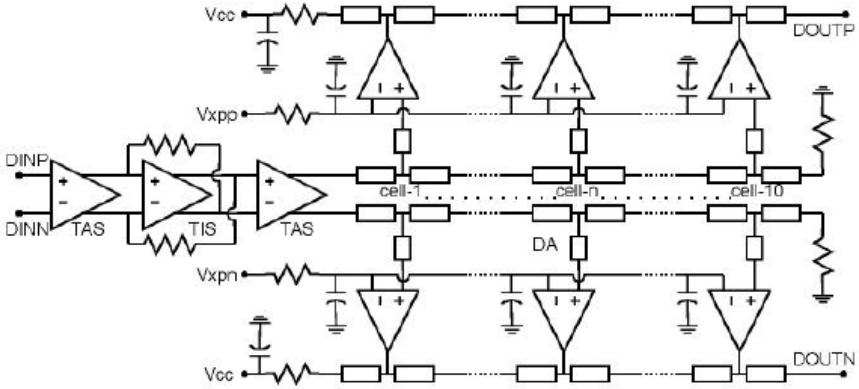
Voltage induces optical phase shift, changes output intensity

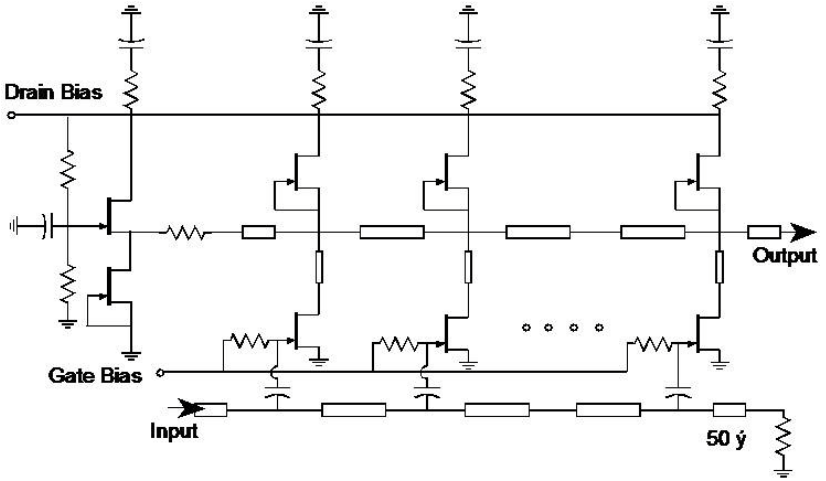
$P_{out} = (P_{in}/2)\left[1 + \cos(\pi V_{signal}/V_\pi)\right]$

V_π is ~ 4 - 6 V for 40 Gb/s modulators : need high - power driver.

Drivers for Electo-optic Modulators







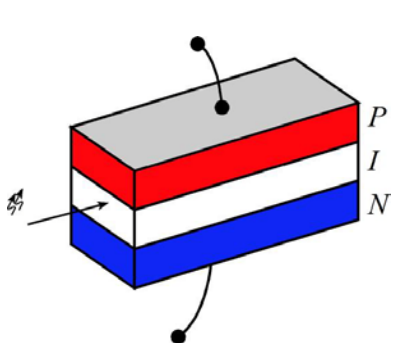
Combination of high bandwidth and high drive (V, I) :

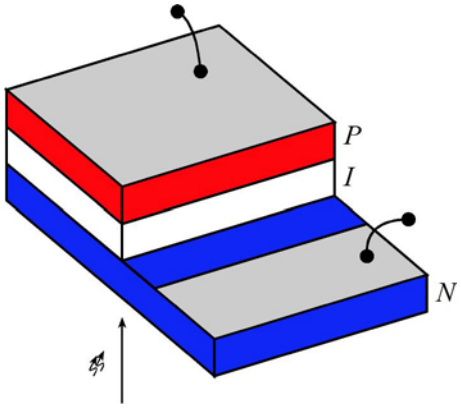
Nearly always a distributed amplifier.

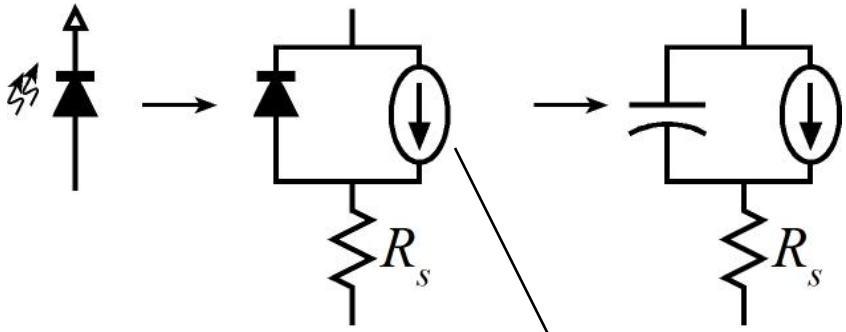
InP HBT or InGaAs/InP HEMT

Single - ended or differential.

Optical Receivers: PIN Photodiodes







$$I_{ph} = \frac{\eta q}{h\nu} P_{opt}$$

Reverse - biased diode with illumination of I - region.

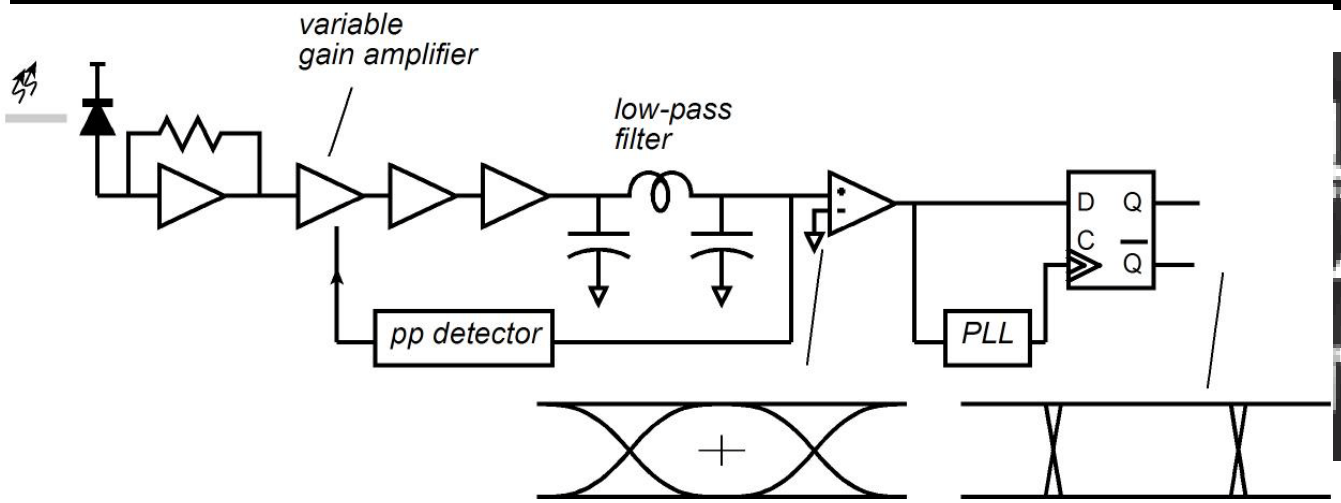
$$I = \frac{\eta q}{h\nu} P_{optical}$$

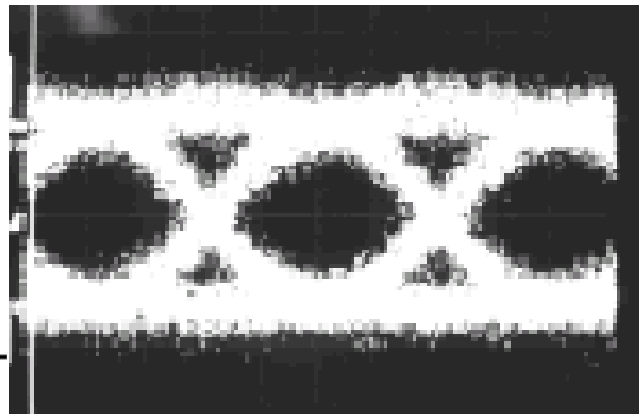
$h\nu / q = 0.954$ V at $\lambda = 1310$ nm

$h\nu / q = 0.800$ V at $\lambda = 1550$ nm

$$C = \varepsilon A / D$$

Optical Receiver; with AGC





Functions :

Transimpedance amplifier : low input noise current, wideband

Linear amplifier chain with variable gain; accomodate range of received power

Low - pass filter * to bandlimit noise from f_{low} to ~ $0.75 \cdot B$ (bit rate)

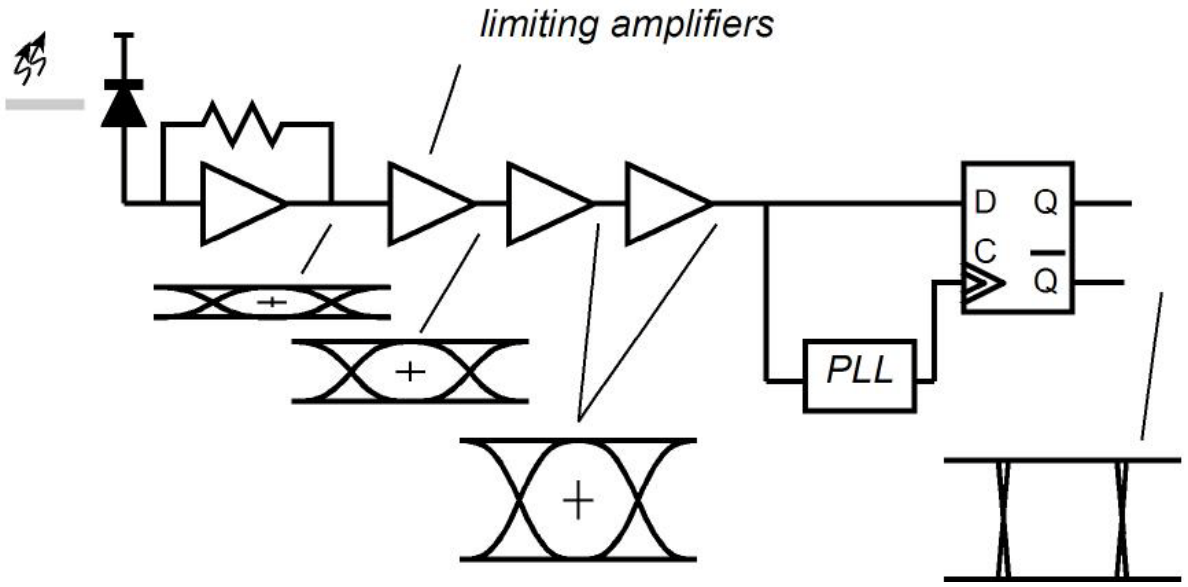
(Not shown) AC coupling or DC restore loop : remove DC from signal

Comparator to quantize in voltage

M/S latch + PLL to set decision time points

* Filter bandwidth is the minimum sufficient for zero intersymbol interference, so as to minimize noise within decision system bandwidth

Limiting Optical Receiver



Simpler form for highest - speed operation,

No AGC; instead, amplifiers limit for stronger input signals.

Each amplifier has bandwidth ~ 75% of B; bandlimits noise.

As input power is increased, more stages driven into limiting.

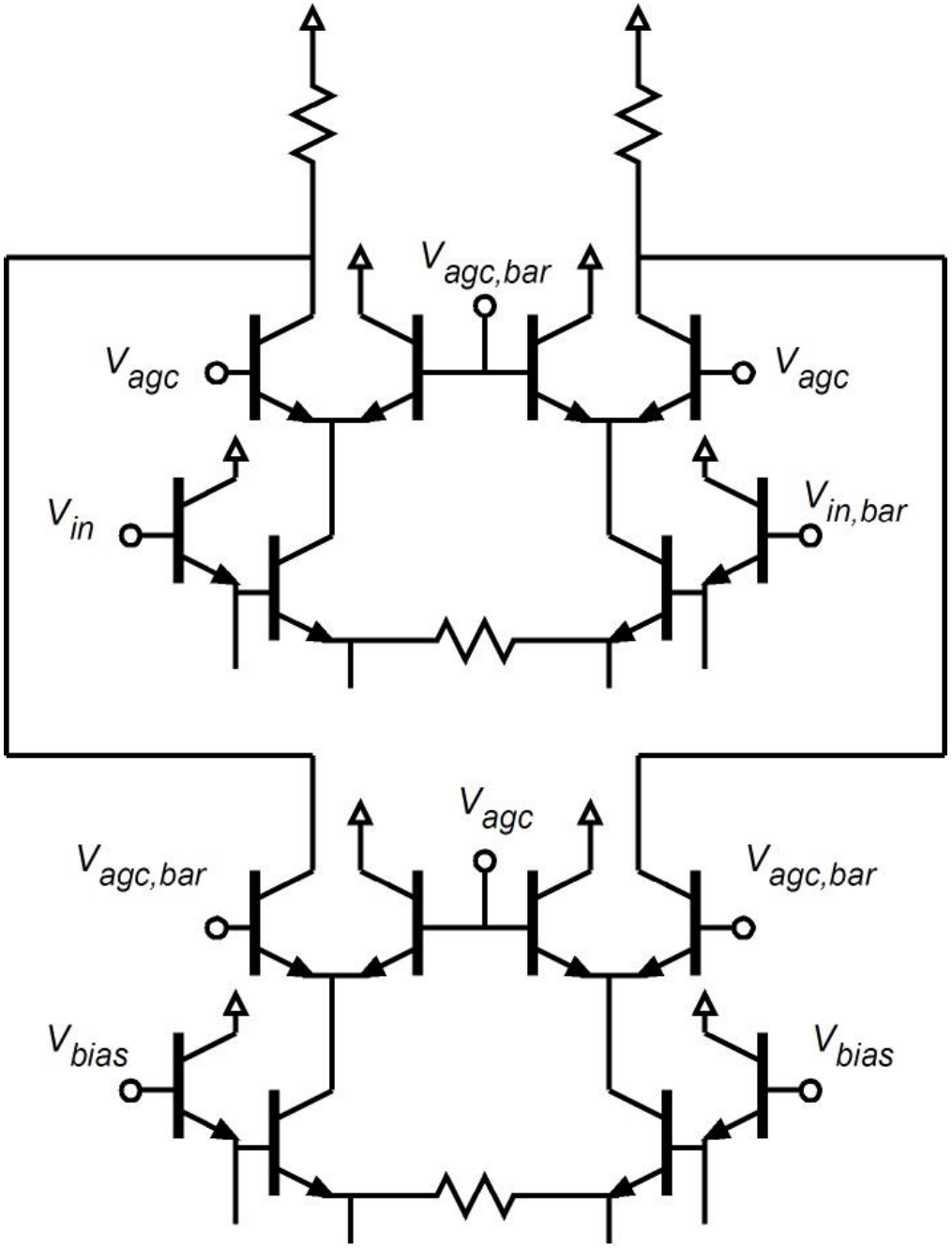
Effective voltage comparison point is first limiting stage.

Bandwidth exceeding $> 0.75 \cdot B$ prior to limiting point degrades sensitivity.

Form does not accomodate dispersion compensation

AC coupling or DC restore needed ; not shown

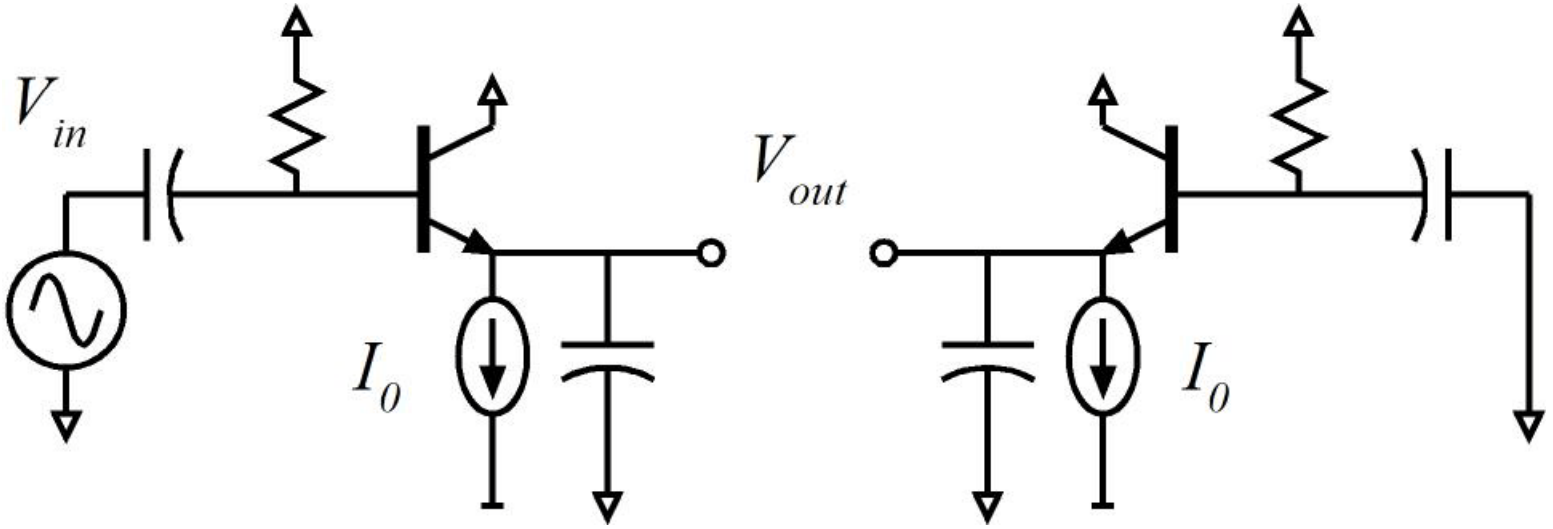
AGC Amplifier: Bipolar



Upper half is basic AGC cell : Differential pair with variable current shunt.

Lower half is DC compensation : Adds DC as gain is reduced, compensates current reduction from upper block.

AGC Detector: Bipolar

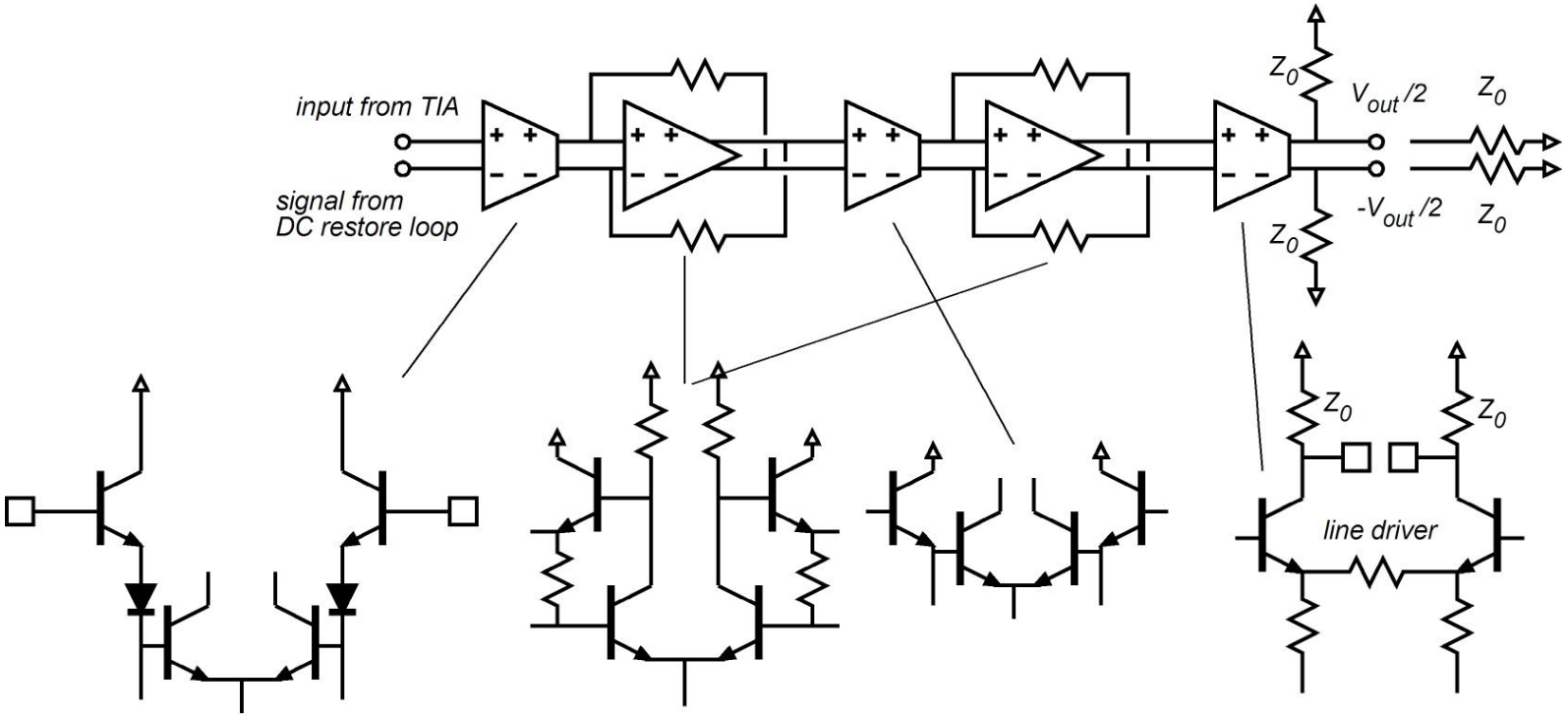


DC currents in the 2 BJTs are forced by current sources all to be I_0.

Analysis (work in lecture) shows that for a inputs much larger than kT/q,

$$V_{out} = V_{in,peak-peak}/2 - kT/q - I_o T_{bit}/C$$

Limiting Amplifier Chain: Bipolar

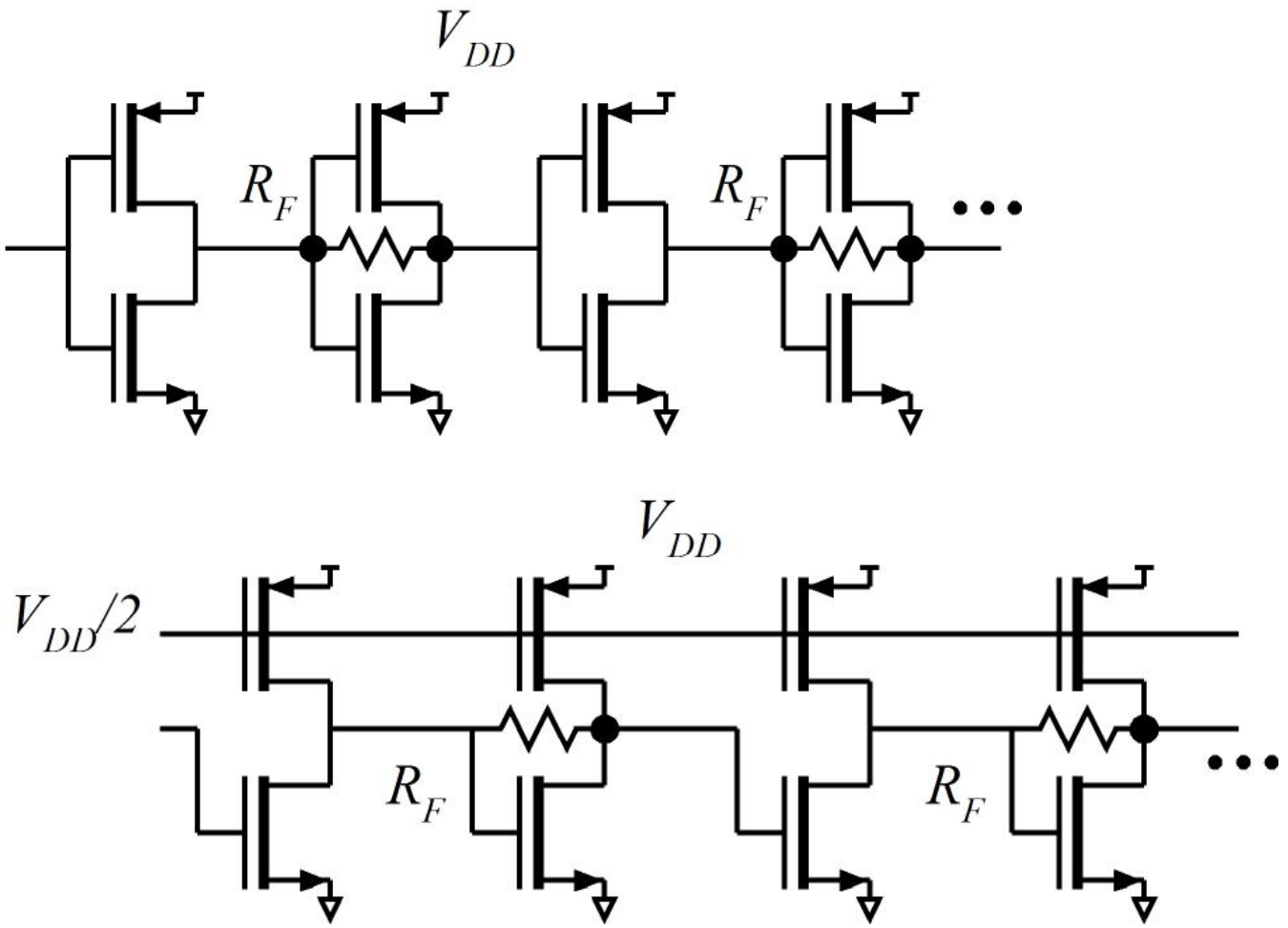


Note input level - shift.

Interconnect drivers /receivers might be current - steering or TAS/TIS.

Anticipate multiple TASTIS stages; more than shown.

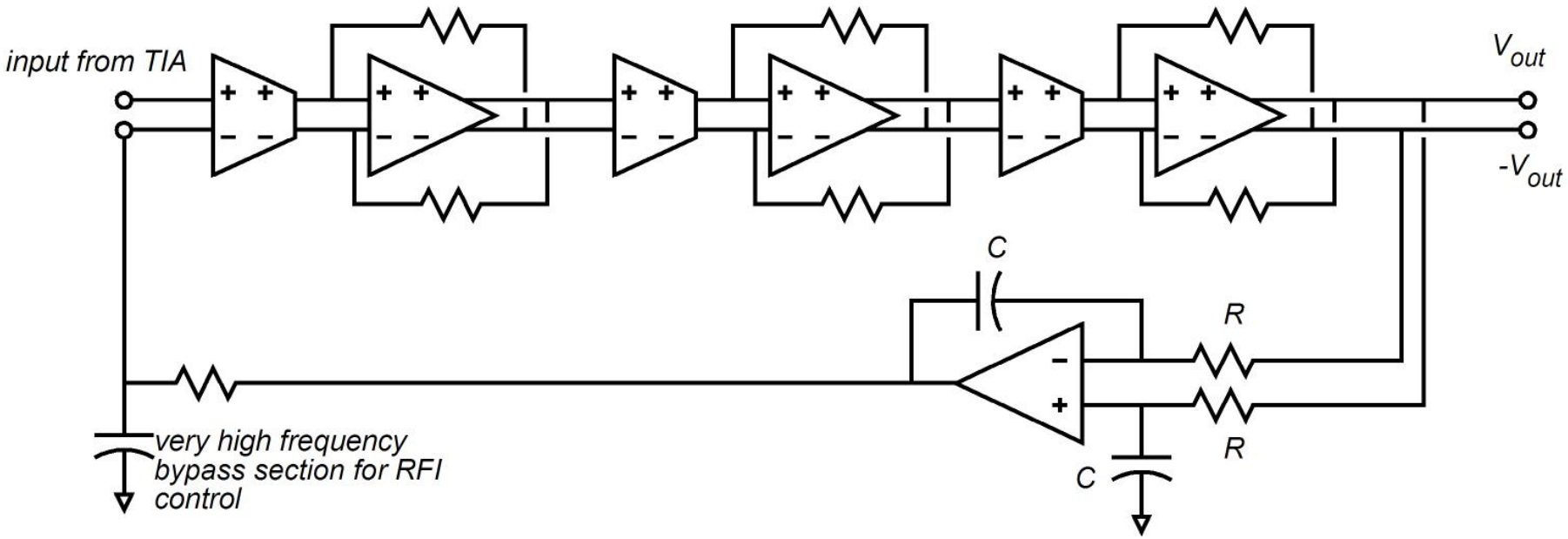
Limiting Amplifier Chain: CMOS & NMOS



DC levels at V_{dd} / 2

Differential forms are also feasible; ask me.

DC Restoration Loop: Instead of AC Coupling



Forward Gain : $A_{OL} = A_v$ Reverse Gain : $\beta = 1/sRC$

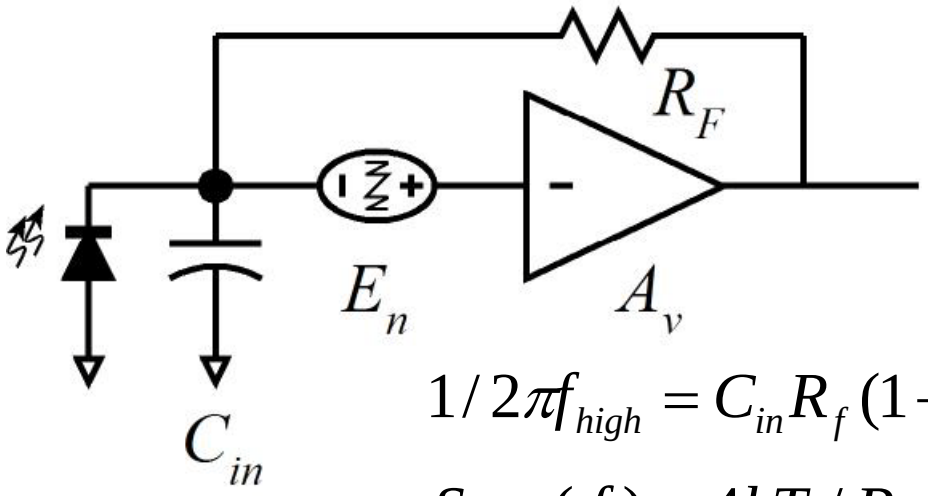
Loop Transmission : $T = A_v/sRC$

Closed - Loop Gain :

$$A_{CL} = \frac{1}{\beta}\frac{T}{1+T} = sRC\,\frac{A_v/sRC}{1+A_v/sRC} = A_v\,\frac{sRC/A_v}{1+sRC/A_v}$$

$$= A_v\,\frac{jf/f_{low}}{1+jf/f_{low}} \quad \text{where} \quad f_{low} = A_v/2\pi RC$$

Why TIA input stage ?



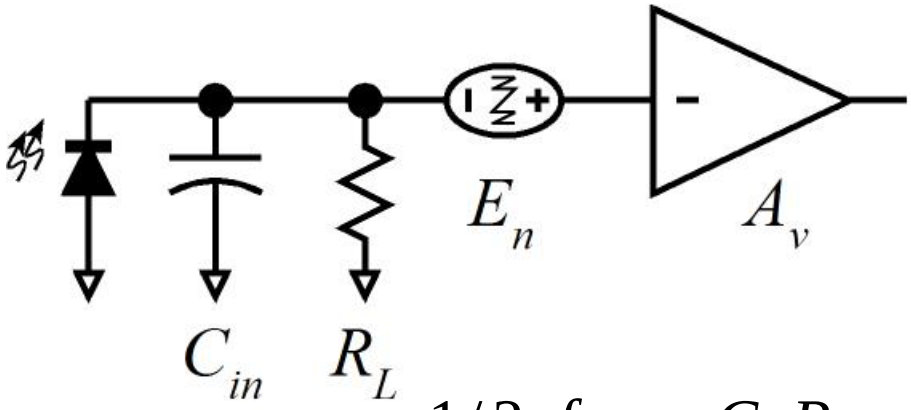
$$S_{E_nE_n}(f) = 4kT\Gamma / g_m + 4kT(R_s + R_g + R_i) + \ldots \quad \text{(FET)}$$

$$S_{E_nE_n}(f) = 2kT / g_m + 4kT(R_{bb} + R_{ex}) + 2qI_bR_{bb}^2 + \ldots \quad \text{(BJT)}$$

Detailed TIA noise analysis left to reader; see noise notes.

$$1/2\pi f_{high} = C_{in}R_f(1+A_v) \quad \text{(Miller effect)}$$

$$S_{I_{in}I_{in}}(f) = 4kT / R_f + (2\pi f C_{in})^2 S_{E_nE_n}(f) + S_{E_nE_n}(f) / R_f^2 + \ldots$$

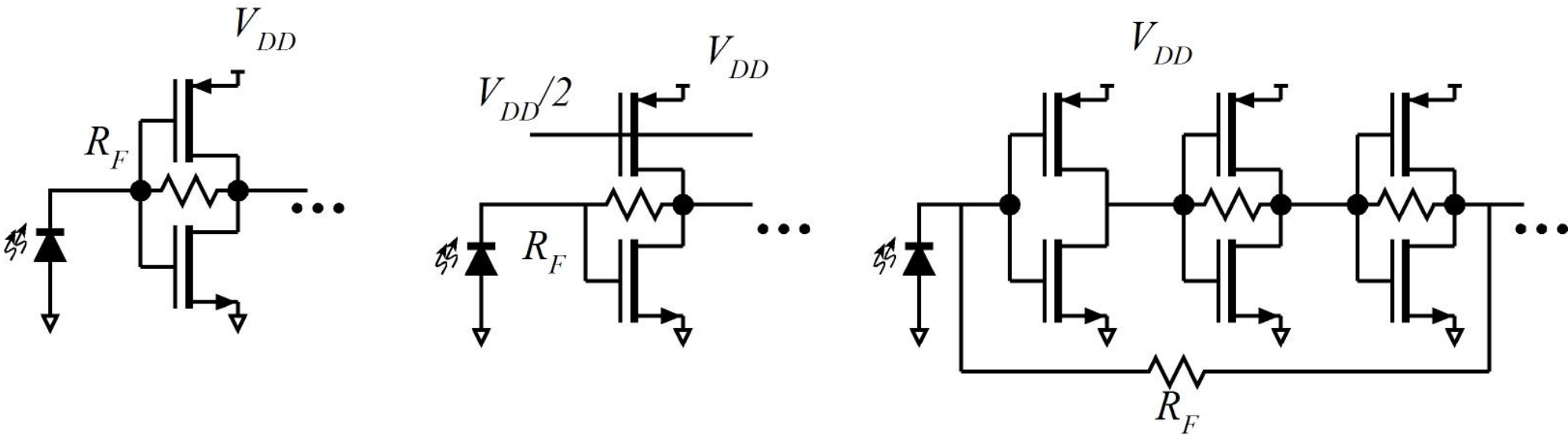


$$1/2\pi f_{high} = C_{in}R_L \quad \text{(need smaller } R \text{ for same bandwidth)}$$

$$S_{I_{in}I_{in}}(f) = 4kT / R_L + (2\pi f C_{in})^2 S_{E_nE_n}(f) + S_{E_nE_n}(f) / R_L^2 + \ldots$$

(more noise because R is smaller)

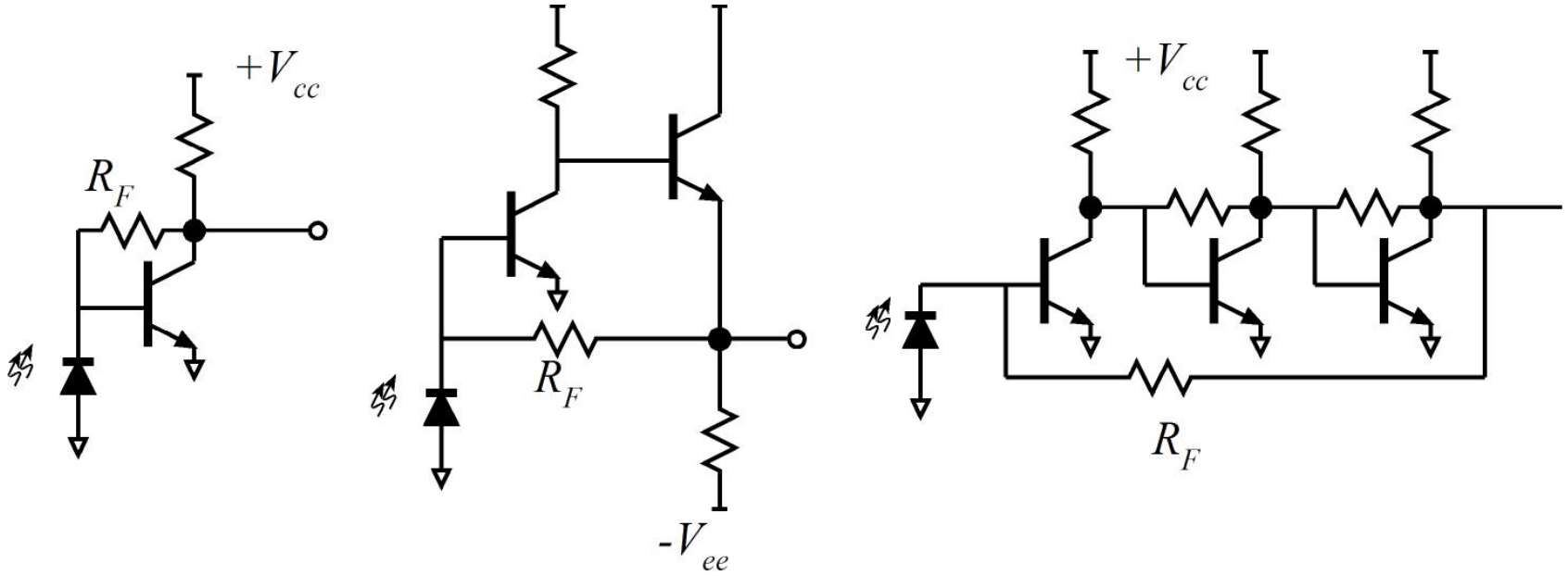
Wideband TIAs: CMOS & NMOS



Left 2 designs are low - gain, wideband designs for very high bit rates.

Right : Lower - rate design; larger open - loop voltage gain, permits larger R_f

Wideband TIAs: Bipolar

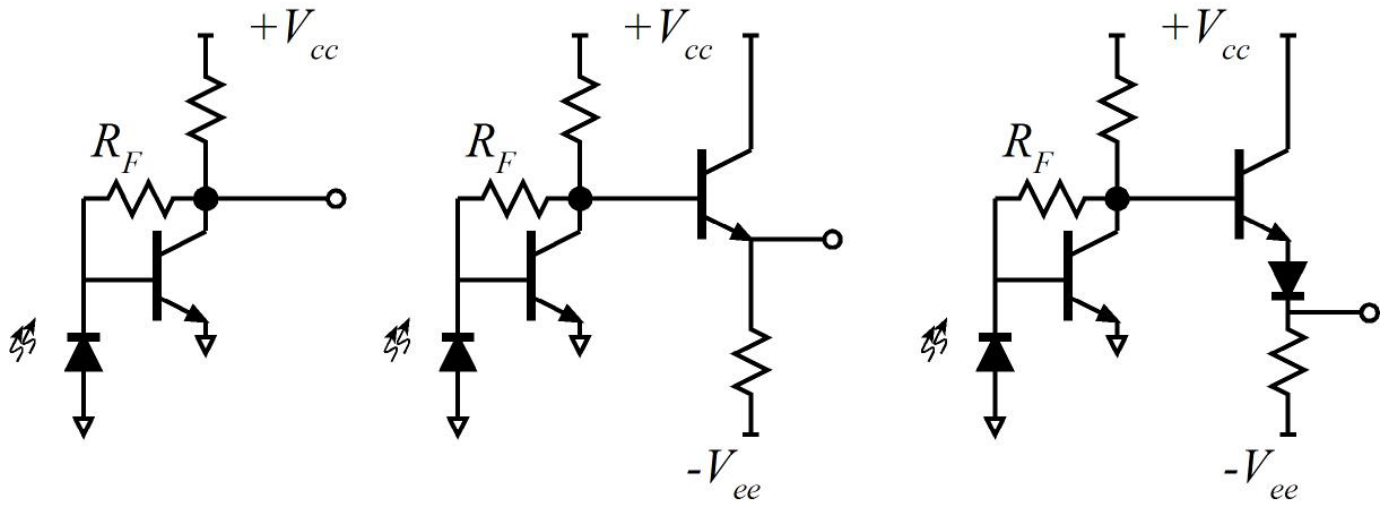


Left : low - gain, wideband design for very high bit rates.

Right : higher - gain, lower bandwidth design for moderate rates.

higher $A_v \rightarrow$ larger R_f feasible $\rightarrow$ less noise.

Wideband TIAs: Output DC Level



This sequence has DC output levels of $(+\phi, 0\ \text{V}, -\phi)$.

Consider what input DC levels TASTIS chain can accept...

Similar level - shifters can be /are used with all TIAs shown.

Designs with many diodes : slow.

Designs with cascaded EF level - shifters : badly damped.

Receiver Sensitivity

This will be derived in a subsequent notes set.

Assume input noise of the form $S_{I_{in}I_{in}}(f) = a + bf^2$

Then

$$P_{\min} = \frac{h\nu}{q\eta} \cdot Q \cdot \sqrt{I_n^2}$$

where :

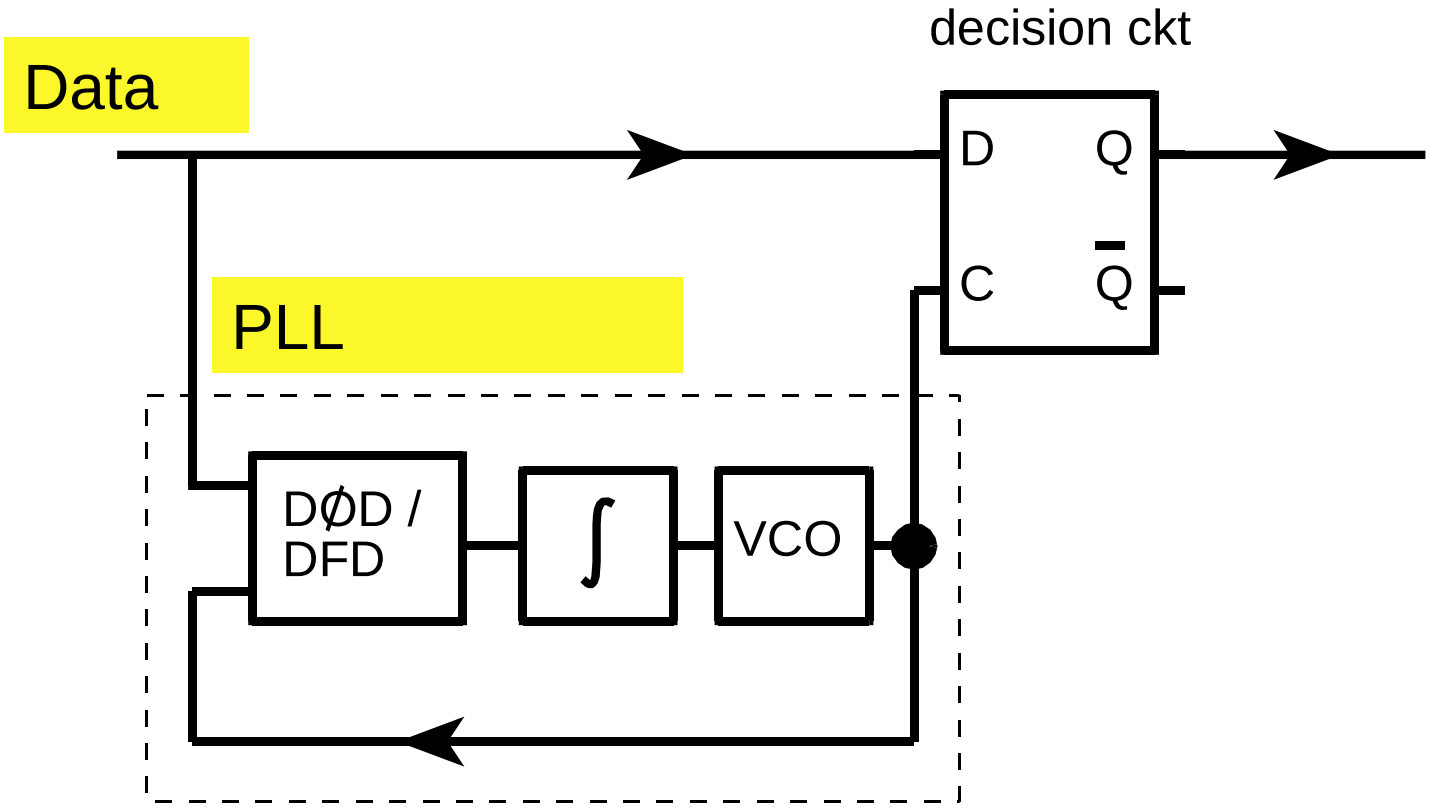
$Q = \text{SNR} = 6$ for 10^{-9} uncoded bit error rate

$$I_n^2 = a \cdot BI_2 + b \cdot B^3 I_3$$

$I_2 \cong 0.68 \qquad I_3 \cong 0.12$

This assumes channel filters having bandwidth ~ 75% of the bit rate B

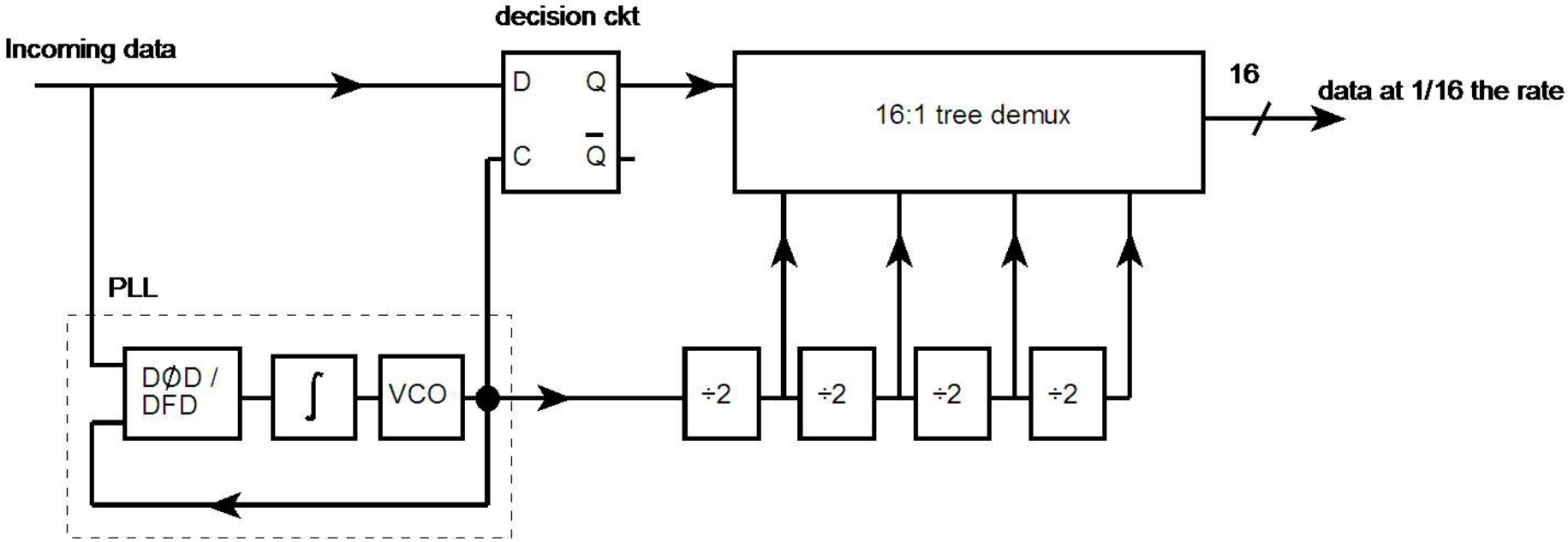
Timing Recovery



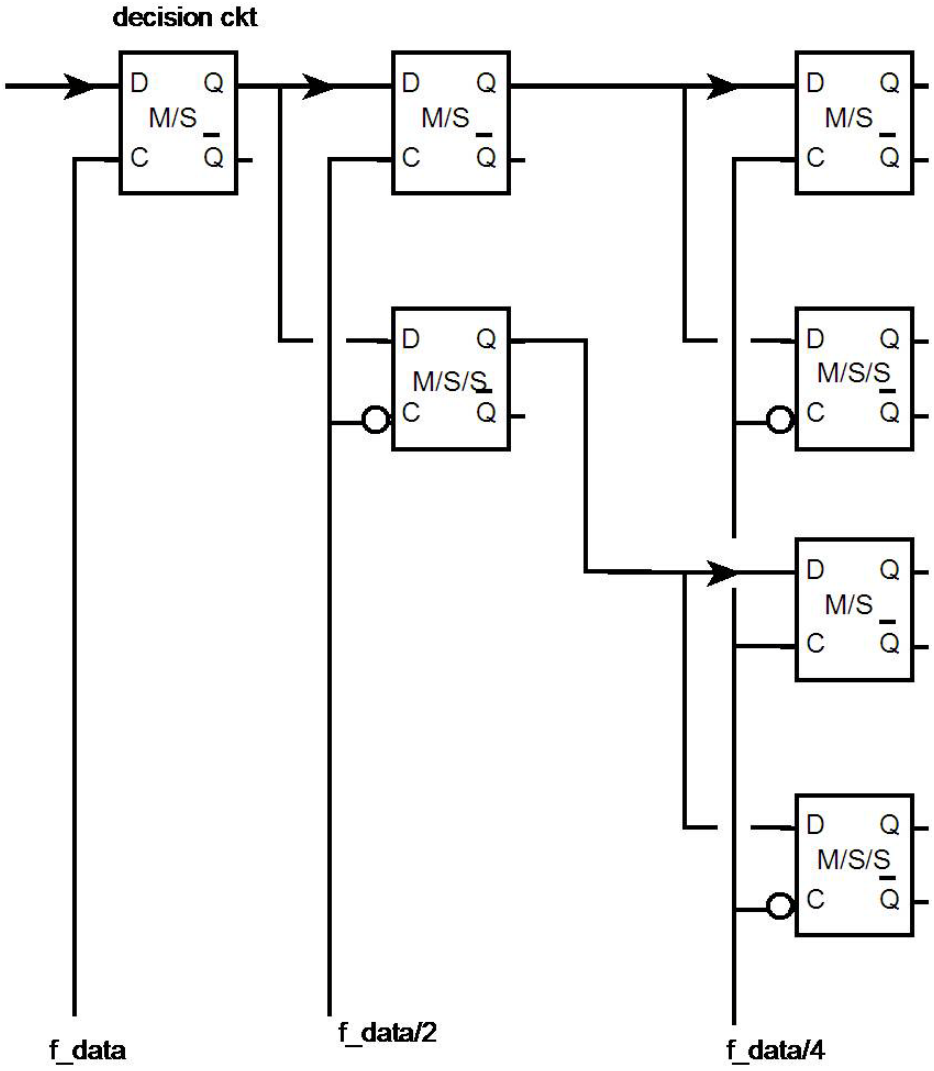
System synchronizes a VCO to the average pulse period of the incoming data

Phase detector must be tolerant of phase reversals inherent to modulated data.

Demultiplexer and interface with timing recovery



Tree demultiplexer



Note that M/S/S latches are required to prevent timing skew.