Submicron Lateral Scaling of Vertical-Transport Devices: Transferred-Substrate Bipolar Transistors and Schottky-Collector Tunnel Diodes

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Transferred-substrate HBTs, fabricated with 0.7 micron emitters and 1.6 micron collectors, obtain 277 GHz power-gain cutoff frequencies f_{max}. At 0.1 μm lithography, the device should obtain $\sim$ 500 GHz f_{max}. Deep submicron Schottky-collector resonant tunnel diodes (SRTDs) have estimated 2.2 THz cutoff frequencies. A 64-element monolithic SRTD array oscillated at 650 GHz.

In the 34–year history of the integrated circuit, the dimensions of semiconductor devices have been progressively reduced. In addition to increased packing density, this device scaling has resulted in greatly increased device bandwidths. Clock rates of CMOS VLSI microprocessors have increased 10:1 in the past decade, and should surpass 1 GHz as the gate lengths approach 0.1 microns. Scaling has also been exploited to great success with III-V high-electron-mobility field-effect transistors (HEMTs). HEMTs fabricated with $0.1\mu m$ gate lengths obtain maximum frequencies of oscillation (f_{max}) above 500 GHz. Given the successful deep submicron scaling of MOSFETs and HEMTs, it is remarkable that both heterojunction bipolar transistors (HBTs) and resonant tunnel diodes (RTDs) are typically fabricated at junction dimensions of 1–2 μm.

HEMTs and MOSFETs are lateral-transport devices, with the electron flux parallel to the plane of the wafer. Decreasing the lithographic dimensions – e.g. the gate length – directly decreases the electron transit times. To maintain low output conductance, as the lateral dimensions are reduced, so must the vertical dimensions be proportionally scaled. In contrast, HBTs and RTDs are vertical transport devices, with the carrier transit times controlled by epitaxial layer thicknesses. In vertical transport devices, there are parasitic RC time constants whose magnitudes are strongly controlled by the widths of the semiconductor junctions. With the correct device structure, reducing the lateral dimensions reduces the parasitic RC charging times, and the device bandwidth increases rapidly with scaling. To render the device scalable, significant changes are first made to the device structure.

In the case of normal double-mesa HBTs, the transfer length of the base Ohmic contact sets a minimum size for the collector-base junction, regardless of lithographic limits. The parasitics ($r_{bb}C_{cb}$) associated with the HBT base-collector junction are thereby not addressed by scaling. We have developed HBTs fabricated in a substrate transfer process. The process allows fabrication of narrow emitter and collector stripes on opposing sides of the base epitaxial layer. $r_{bb}C_{cb}$ becomes proportional to the process minimum feature size, and f_{max} increases rapidly with scaling (fig. 1).

To build the device, normal fabrication processes form the emitter-base junctions and their associated contacts. The wafer is then coated with a polymer (BCB) dielectric, and thermal vias and a wafer ground plane formed by etching and electroplating. The wafer is die-attached to a transfer substrate, and the InP growth substrate removed by a selective etch. The device is completed by deposition of the Schottky collector contacts. Recent devices with 0.7 μm emitters (fig. 2) have 277 GHz f_{max}. Deep submicron devices should obtain f_{max} exceeding 500 GHz. The process also has significant potential advantages in IC packaging, including high thermal conductivity and a microstrip wiring environment with a low-inductance interface between the IC and package ground systems. Target applications include 100 Gb/s fiber transmission, microwave analog-digital-converters, and mm-wave frequency synthesis.

Resonant-tunnel-diodes also benefit from deep submicron scaling. In addition to the effect of the tunneling time, RTD bandwidths are strongly controlled by RC charging times associated with the device parasitic series resistance. In the case of the normal (Ohmic-collector) RTD, the resistance of the top Ohmic contact increases progressively as the device junction area is reduced. The normal RTD is consequently not scalable. In the Schottky-collector RTD (SRTD), the parasitic top-Ohmic-contact resistance is eliminated. The remaining components of the device parasitic series resistance are minimized by scaling the device to deep submicron dimensions. The SRTD f_{max} increases rapidly (fig. 1). With these devices, we have recently constructed submillimeter-wave monolithic quasi-optical array oscillators (fig. 3). The arrays incorporate 0.1 μm SRTDs, resistors, Si_3N_4 MIM capacitors, airbridges, and Schottky-diode bias regulators, fabricated in an 8-mask process. A 64-element SRTD array oscillated at 650 GHz.

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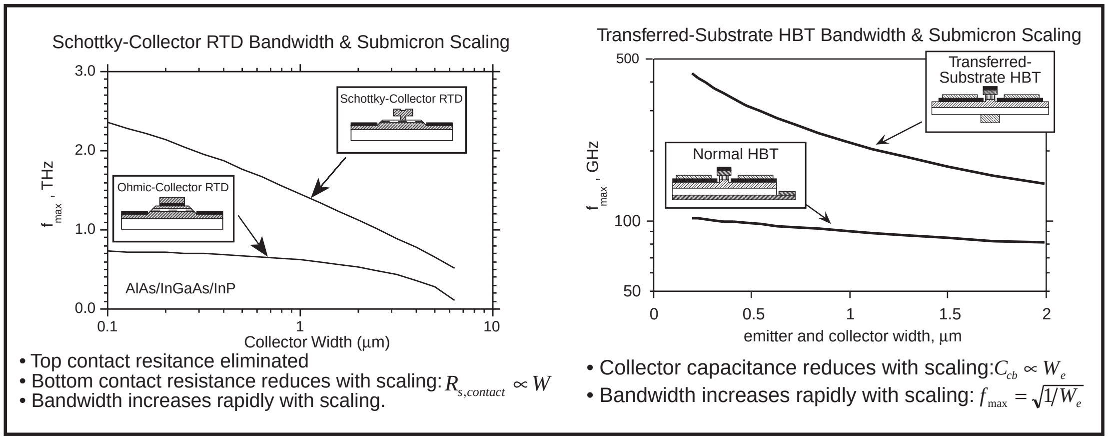

Figure 1: RTD and HBT scaling laws

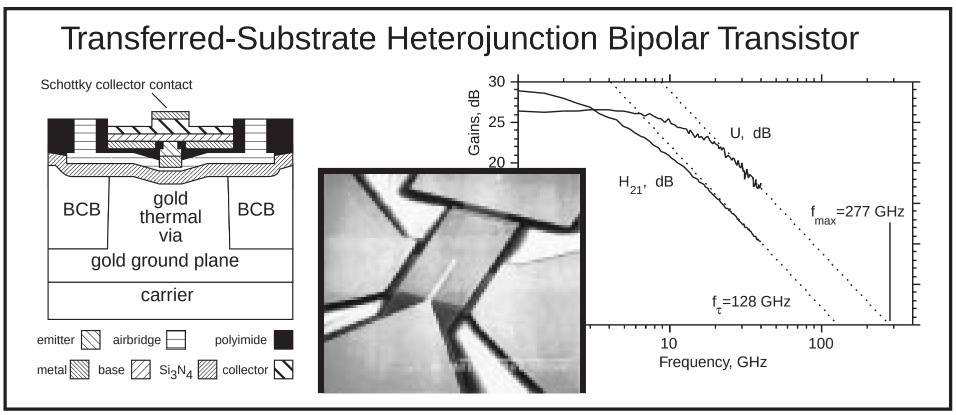

Figure 2: Transferred-Substrate HBT; cross-section, SEM, and performance

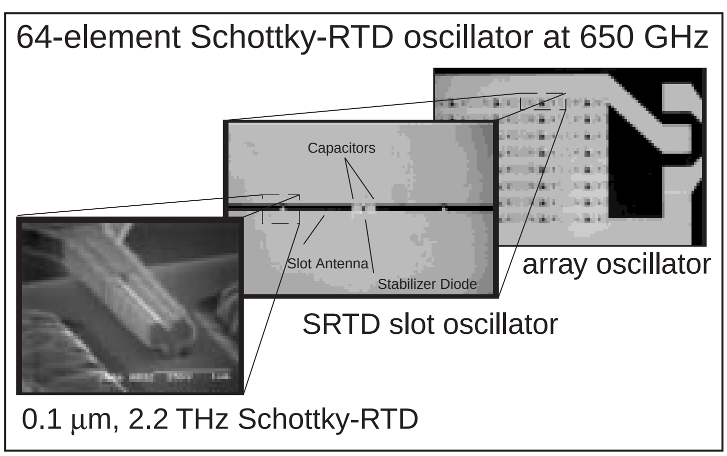

Figure 3: 650 GHz SRTD oscillators; device, oscillator, and array