A >400 GHz f_{max} Transferred-Substrate Heterojunction Bipolar Transistor IC Technology

Q. Lee, B. Agarwal, D. Mensa, R. Pullela, J. Guthrie, L. Samoska and M. J. W. Rodwell

Abstract—**We report transferred-substrate AlInAs/GaInAs heterojunction bipolar transistors. A device having a 0.6 μm $\times$ 25 μm emitter and a 0.8 μm $\times$ 29 μm collector exhibited $f_\tau = 134$ GHz and $f_{max} > 400$ GHz. A device with a 0.6 μm $\times$ 25 μm emitter and a 1.8 μm $\times$ 29 μm collector exhibited 400 GHz f_{max} and 164 GHz f_τ. The transferred-substrate fabrication process provides electroplated gold thermal vias for transistor heatsinking and a microstrip wiring environment on a low dielectric constant polymer substrate.**

I. Introduction

HETEROJUNCTION bipolar transistors (HBTs) have applications in gigabit optical fiber transmission, wideband analog-digital conversion, and direct digital frequency synthesis. High circuit bandwidths are desirable; in Δ-Σ analog-digital converters, increased clock frequencies provide increased signal-noise ratios, while future optical transmission systems will require multiplexers, PLLs, and decision circuits with $\sim$ 100 GHz clock rates.

To permit clock rates exceeding 100 GHz, the transistor current gain (f_τ) and power-gain (f_{max}) cutoff frequencies must be several hundred GHz. The interconnects must have small inductance and capacitance per unit length, and wire lengths, hence transistor spacings, must be small. Given that fast HBTs operate at $\sim 10^5$ A/cm^2 current density, efficient heat sinking is then vital.

Using a substrate transfer process [1], [2], [3], HBTs can be fabricated with narrow emitter and collector stripes aligned on opposing sides of the base epitaxial layer. The base resistance - collector capacitance product ($r_{bb}C_{cb}$) becomes proportional to the process minimum feature size, and f_{max} increases rapidly with scaling [1]. We had earlier reported transferred-substrate HBTs [2] with 277 GHz f_{max}. Here, we report greatly improved devices. A transferred-substrate HBT having a 0.6 μm $\times$ 25 μm emitter and a 0.8 μm $\times$ 29 μm collector exhibited a record $f_{max} > 400$ GHz and $f_\tau = 134$ GHz. A device with a similar 0.6 μm $\times$ 25 μm emitter but having a wider 1.8 μm $\times$ 29 μm collector had 400 GHz f_{max} and 164 GHz f_τ. The interconnects, microstrip on Benzocyclobutene (BCB), have a low ($\epsilon_r = 2.7$) dielectric constant for low capacitance and a ground plane for low ground-return inductance. Transistor heatsinking is provided by electroplated gold thermal vias.

II. Fabrication

The MBE layer structure is similar to that reported in [2] (fig. 1(a)). The 500 Å GaInAs base is graded in both doping and bandgap. The 100 Å of the $Ga_{0.47}In_{0.53}As$ base immediately adjacent to the collector is Be-doped at 3×10^{19}/cm^3. The remaining 400 Å of the base is Be-doped at 5×10^{19}/cm^3. By increasing the Ga cell temperature progressively during growth of the 400 Å layer, the Ga:In ratio is progressively increased, introducing a $\sim$ 0.03 eV bandgap gradient across the 400 Å layer.

The fabrication process is similar to that described in [2], except that the transistor active layers are bonded to the GaAs transfer substrate with a In/Pb/Ag alloy. The alloy has higher thermal conductivity than the epoxy used

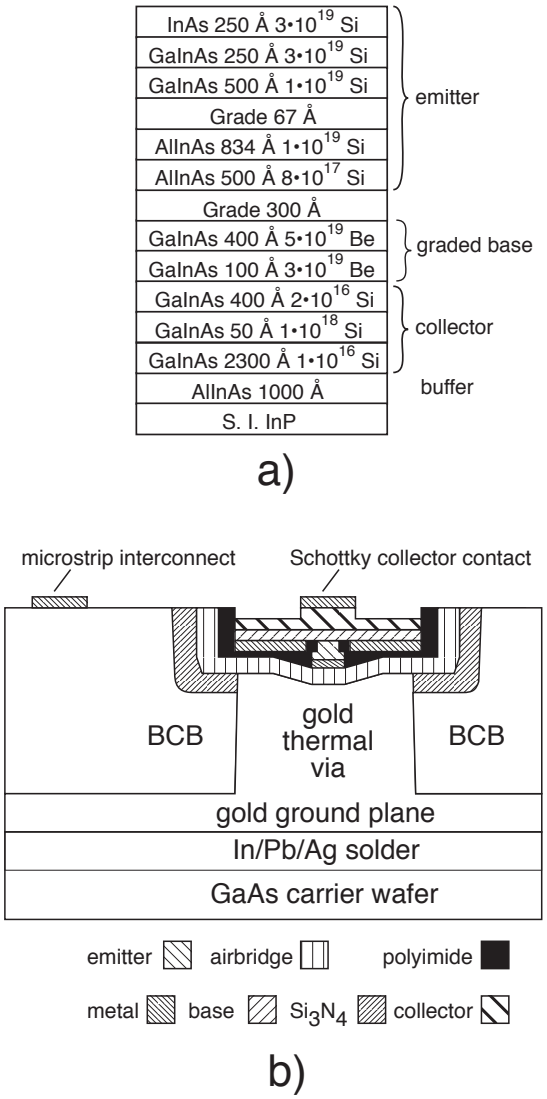

Fig. 1. a) MBE layer structure and b) schematic cross section of transferred-substrate HBT.

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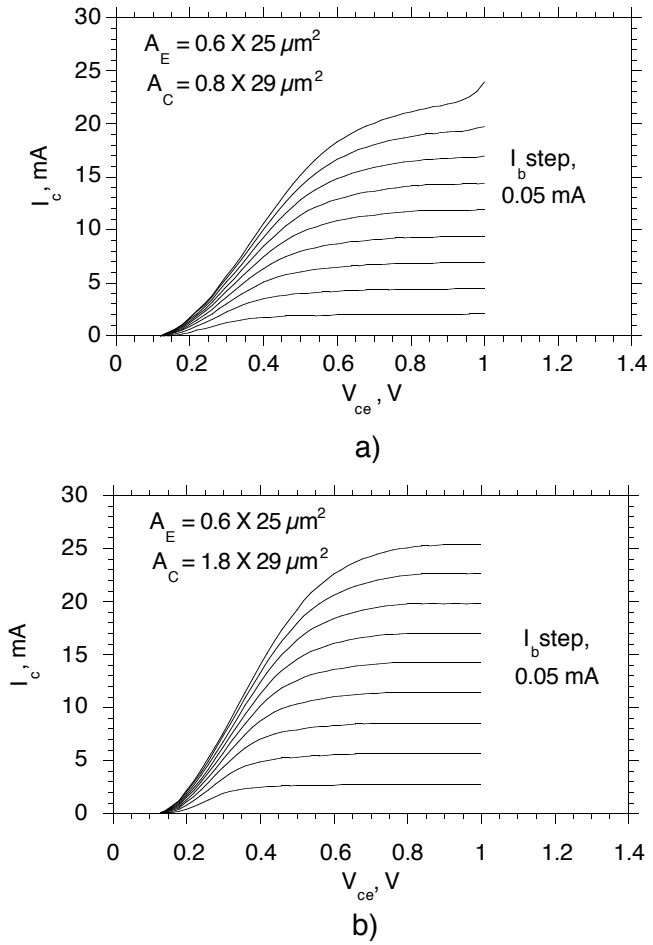

Fig. 2. DC common-emitter characteristics of transferred-substrate HBTs with 0.6 μm by 25 μm emitters and with collector dimensions of (a) 0.8 μm by 29 μm and (b) 1.8 μm by 29 μm.

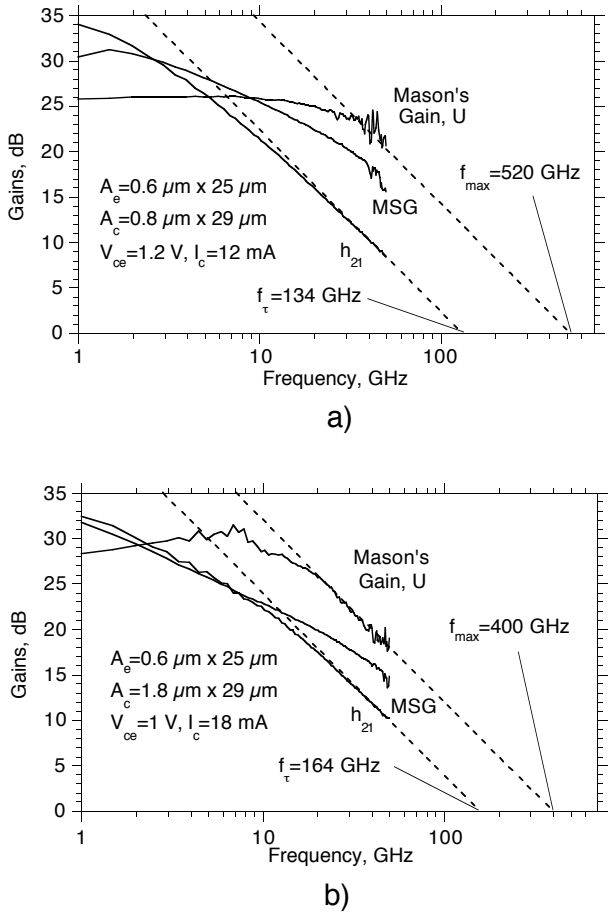

Fig. 3. RF characteristics of transferred-substrate HBTs with 0.6 μm by 25 μm emitters and with collector dimensions of (a) 0.8 μm by 29 μm and (b) 1.8 μm by 29 μm.

in [2], and, provides a more planar bond. To permit IC fabrication, the process incorporates thin-film NiCr resistors with 50 $\Omega/\Box$ sheet resistivity, SiN MIM capacitors and three levels of wiring metallization.

Devices were fabricated with 25 μm by 0.6 μm emitters and with collector dimensions of 29 μm by 0.8 μm (narrow-collector) and 29 μm by 1.8 μm (wide-collector). A schematic cross section of the HBT is shown in fig. 1(b). Wet chemical etches with lateral undercuts are used to reduce both the emitter-base and collector-base junction areas to below their lithographically defined dimensions. Junction dimensions are determined by measuring (with a microwave network analyzer) the junction capacitances vs. the lithographically defined junction widths.

III. Results

DC common-emitter characteristics of the HBTs are shown in fig. 2. The small signal DC current gain is 55. At high current densities, narrow-collector devices show significantly larger collector-emitter saturation voltages ($V_{CE,sat}$), arising from screening of the collector electrostatic field by the electron space charge. Screening occurs at a *collector* current density J_c satisfying the relationship $(V_{CB} + \phi) = T_c^2(J_c/v_{sat} - qN_d)/2\epsilon$, where T_c is the collector depletion layer thickness, N_d the collector doping, ϕ the junction built-in potential, and v_{sat} the electron velocity. In wide-collector HBTs, there is significant lateral spreading of the electron flux at high current densities [4], reducing the collector space-charge density.

Lateral current confinement in narrow-collector HBTs results in both increased $V_{CE,sat}$ and decreased emitter current density at the onset of f_τ collapse (Kirk effect), resulting in increased emitter charging times and reduced f_τ.

The devices were characterized by on-wafer network analysis to 50 GHz. Fig. 3 shows the short-circuit current gain h_{21}, maximum stable gain (MSG), and Mason's invariant (unilateral) power gain U. Pad parasitics have not been stripped. Extrapolating at -20 dB/decade, $f_{max} = 400$ GHz and $f_\tau = 164$ GHz for the wide-collector devices (fig. 3(b)).

RF measurements (fig. 3(a)) of the narrow-collector devices yield 134 GHz f_τ and $\sim$ 450-550 GHz extrapolated f_{max}. Such measurements are however at the limits of reliability for a 50 GHz instrument. We now estimate f_{max} by calculation from $f_{max} \simeq \sqrt{f_\tau/8\pi r_{bb}C_{cbi}}$. Here C_{cbi}

is the intrinsic base-collector capacitance, the fraction of C_{cb} charged through the base resistance r_{bb}. r_{bb} consists of sheet resistance and contact resistance. The measured base sheet resistance is 600 $\Omega/\Box$. Because of poor test structure design, the specific base Ohmic contact resistivity falls below levels which can be reliably measured by the (TLM) test structures employed on the present wafer, and we therefore take reported values of specific contact resistivity for test structures (23 $\Omega - \mu m^2$, [5]) having similar levels of Be-doping. With these parameters, we calculate [1] a 2.4 Ω base spreading resistance and a 2.4 Ω base contact resistance. C_{cb} is extracted from s-parameter measurements by plotting the imaginary part of the reverse admittance parameter y_{12} vs. frequency. The C_{cbi}/C_{cb} ratio is not readily predicted from device geometry [6], [7], but is often fitted by comparing measured and modeled s-parameters. Here, we roughly estimate the C_{cbi}/C_{cb} ratio as being equal to the ratio of the emitter-base and collector-base junction areas. For wide-collector devices, measured $f_\tau = 164$ GHz, $C_{cb} = 22.7$ fF, $C_{cbi} = 7.5$ fF and $f_{max} = 426$ GHz. For narrow-collector devices, $f_\tau = 134$ GHz, $C_{cb} = 8.2$ fF, $C_{cbi} = 6.2$ fF, and $f_{max} = 423$ GHz. Both the above calculations and the microwave measurements indicate that f_{max} is at least 400 GHz. The MSG ($\simeq (\omega C_{cb})^{-1}(r_{ex} + (kT/qI_E))^{-1}$) is higher for the narrow-collector devices because of the reduced C_{cb}.

Fig 4 shows the variation of f_τ and f_{max} with bias. f_τ is similar for both devices. The narrow-collector devices exhibit the Kirk effect at lower current density than wide-collector devices. Fig. 4(b) shows a plot of f_τ and f_{max} vs. collector-emitter voltage, V_{CE}. At low V_{CE}, the collector is partially depleted leading to increased C_{cb} and reduced f_{max}. At high V_{CB}, f_τ and f_{max} decrease, suggesting a decrease in the electron velocity at high electric fields. By plotting $1/2\pi f_\tau$ vs. J_E, it is determined that the sum of the base and collector transit times ($\tau_b + \tau_c$) is 0.75 ps. With the device parameters given above, (and with $C_{je} = 132$ fF, $r_{ex} = 2.8\Omega$) the hybrid-π equivalent circuit model [2] is fully described and provides a reasonable fit to the measured RF parameters.

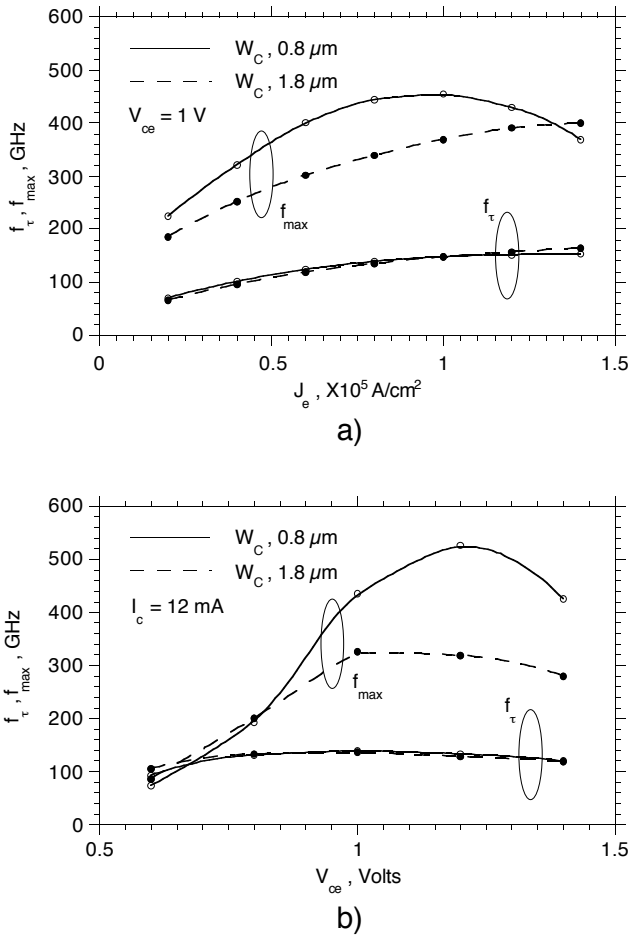

Fig. 4. Variation of f_τ and f_{max} with (a) emitter current density J_e and (b) collector-emitter voltage V_{ce}.

IV. Conclusions

We have demonstrated AlInAs/GaInAs transferred-substrate HBTs with extrapolated f_{max} exceeding 400 GHz. f_{max} is higher than that reported in [2] due to greatly improved base Ohmic contacts, substantially narrower emitter and collector junction areas and slightly reduced forward transit time. Devices in fabrication having $\sim 0.3\mu$m emitter and collector widths should obtain substantially larger f_{max}. Integrated circuits have been fabricated in the transferred-substrate process, and will be reported subsequently.

Acknowledgments

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