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ULTRAHIGH f_{max} AlInAs/GaInAs TRANSFERRED-SUBSTRATE HETEROJUNCTION BIPOLAR TRANSISTORS FOR INTEGRATED CIRCUITS APPLICATIONS

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Transferred-substrate heterojunction bipolar transistors (HBTs) have demonstrated very high bandwidths and are potential candidates for very high speed integrated circuit (IC) applications. The transferred-substrate process permits fabrication of narrow and aligned emitter-base and collector-base junctions, reducing the collector-base capacitance and increasing the device f_{max}. Unlike conventional double-mesa HBTs, transferred-substrate HBTs can be scaled to submicron dimensions with a consequent increase in bandwidth. This paper introduces the concept of transferred-substrate HBTs. Fabrication process in the AlInAs/GaInAs material system is presented, followed by DC and RF performance. A demonstration IC is shown along with some integrated circuits in development.

1. Introduction

Heterojunction bipolar transistors (HBTs)[1] have high transconductance, extremely reproducible DC parameters and wide bandwidth. These attributes make HBTs the device of choice for many precision high speed circuits. Important HBT applications include analog-to-digital conversion[2], chip-sets for fiber-optic transmission[3,4,5], and phase-locked loops for direct digital frequency synthesis. These are all medium-scale integrated circuits operating at frequencies of several tens of GHz and incorporating both precision broadband analog and very high clock-rate digital subcircuits. In these applications, both the transistor current gain cut-off frequency f_τ, and the power gain cut-off frequency f_{max} must be considerably higher than the signal frequencies involved. 100 Gbps optical-fiber transmission ICs will require HBTs having f_τ and f_{max} greater than 200-250 GHz[6]. A second-order $\Sigma - \Delta$ analog-digital converter having a 50 GHz sample rate would require HBTs with f_τ and $f_{max} \sim$ 200-300 GHz, but might provide 12 bits resolution at 1 GHz bandwidth. Broadband amplifiers for 40 & 100 Gbps communication would require HBTs with similar performance. HBTs with bandwidths of several hundred GHz will benefit

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many similar applications.

Progressive improvements in device bandwidths are needed to keep pace with the demand for integrated circuits operating at higher frequencies. High electron mobility transistors (HEMTs) with short gate lengths ($\sim$ 0.1 μm) are presently the largest bandwidth three terminal devices. HEMTs with a power gain cutoff frequency (f_{max}) of 450 GHz have been reported[7]. The superior bandwidths of HEMTs is a result of the rapid improvement in HEMT bandwidth with deep submicron scaling.

Reducing the lithographic dimensions (lateral) and/or the semiconductor layer thicknesses (vertical) of a device is termed device scaling. Scaling pertinent device dimensions is central to high frequency semiconductor device design. With several important semiconductor devices, the device bandwidth increases as critical lithographic dimensions and layer thicknesses are reduced. Examples of highly scaled devices with large bandwidths are 0.1 μm gate length high electron mobility transistors (HEMTs), 0.25 μm gate length complementary metal-oxide-semiconductor (CMOS) transistors, 0.1 μm Schottky-collector resonant tunnel diodes (SRTDs)[8] and submicron Schottky diodes used as sub-millimeter wave mixers.

Fig. 1 shows f_{max} vs. emitter width for some HBTs reported in the literature. It can be seen that there is no strong correlation between f_{max} and emitter width, at least for narrow emitters. Consequently, HBTs are not fabricated with deep submicron dimensions except where bias currents have to be limited for low power operation.

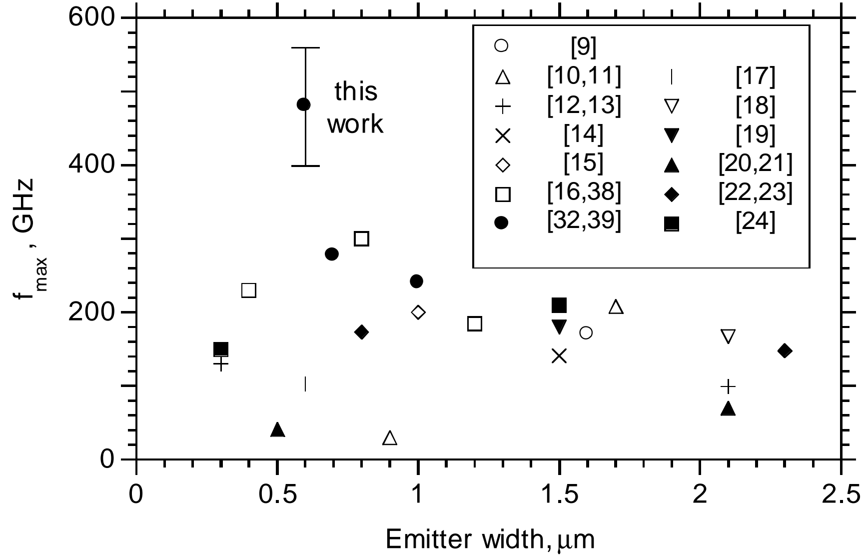


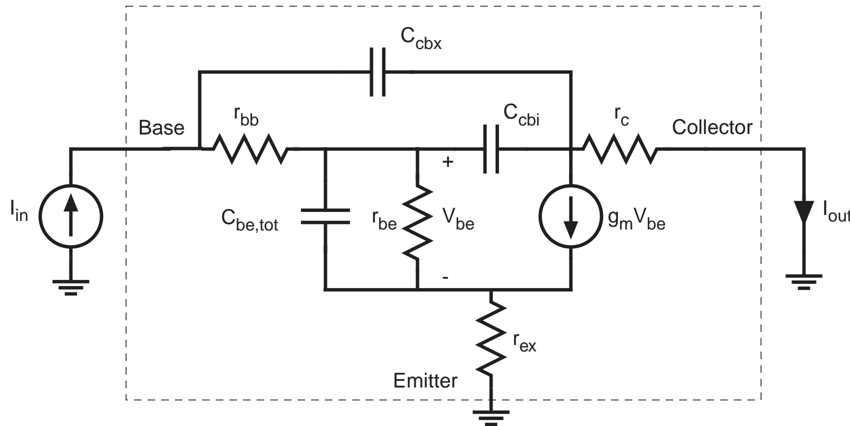
Figure 1: Comparison of f_{max} and emitter width for some HBTs in the literature.

We will now explore the relationship between f_{max} and emitter and collector

widths. A simple hybrid-π model of an HBT is shown in Fig. 2 with the model components related to the device parameters and biasing conditions. The expression for short circuit current gain corresponding to this device model is

$$A_I = \frac{-\beta}{1 + j\omega\beta\left[(1/g_m)\left(C_{be,\text{tot}} + C_{cb}\right) + (r_{ex} + r_c)C_{cb}\right]} \tag{1}$$

under the following conditions: DC short circuit current gain $\beta \gg 1$, $\omega C_{cb} \ll g_m/(1 + g_m r_{ex})$, only first order terms in angular frequency ω considered and the extrinsic C_{cb} charging time is small.



r_{bb} base resistance

r_c collector contact resistance

r_{ex} emitter contact resistance

$r_{be} = \beta/g_m$

$C_{be,tot} = g_m(\tau_b + \tau_c) + C_{be,depl}$

C_{cbi} intrinsic collector-base capacitance

C_{cbxi} extrinsic collector-base capacitance

$g_m = qI_c / kT$

Figure 2: Hybrid-π model of an HBT, connected externally for calculation of the short-circuit current gain.

The short circuit current gain cutoff frequency f_τ corresponds to the frequency at which the magnitude of A_I is unity. Near this frequency, the imaginary part of the denominator in Eq. (1) is much larger than unity. The expression for f_τ as a function of device parameters and biasing conditions is therefore approximately

$$\frac{1}{2\pi f_\tau} = \tau_b + \tau_c + \frac{kT}{qI_c}(C_{be} + C_{cb}) + (r_{ex} + r_c)C_{cb}. \tag{2}$$

Here τ_b is the base transit time, τ_c the collector transit time, kT/q the thermal voltage, I_c the collector current, C_{be} the base-emitter depletion capacitance, C_{cb} the collector-base capacitance, r_{ex} the emitter contact resistance, and r_c the collector

contact resistance. At a given current density, all terms except r_c in the above equation are independent of lateral scaling. The base and collector transit times can be reduced by reducing the appropriate semiconductor layer thicknesses. Hence, f_τ can be improved by vertical scaling of the device, but is independent of lateral scaling.

The power gain cutoff frequency f_{max} is another important figure-of-merit of high-frequency HBT performance. F_{max} defines the maximum frequency at which a device can provide power gain. F_{max} not only depends on f_τ, but also on the base-resistance-collector-base-capacitance time constant as

$$f_{max} = \frac{1}{2}\sqrt{f_\tau f_{cb}} \quad (3)$$

where

$$f_{cb} = \frac{1}{2\pi r_{bb} C_{cbi}} \quad (4)$$

where, r_{bb} is the base resistance and C_{cbi} is the fraction of the collector-base capacitance that is charged through the base resistance. No matter how large the value of f_τ is, power gain is available only at frequencies below f_{max}. Hence, to improve device bandwidth, is it important to improve f_τ and the $r_{bb}C_{cb}$ time constant. Note that while the extrinsic collector-base capacitance has no impact on f_{max}, it does impact the performance of many circuits, and should be minimized.

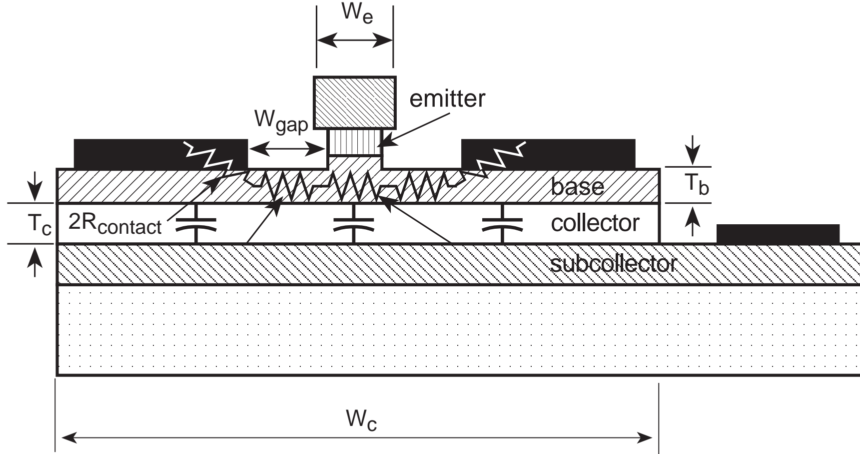


Figure 3: Schematic cross-section of a double-mesa HBT.

The cross section of a double-mesa HBT is shown in Fig. 3. The base resistance r_{bb} has three components. These are: the contact resistance from the base Ohmic contact, the sheet resistance from the gap between the emitter mesa and the base Ohmic contact, and the spreading resistance of the base layer underneath the

emitter mesa. The contact resistance is given by

$$R_{contact} = \sqrt{\rho_{bc}\rho_{bs}}/2l \tag{5}$$

where ρ_{bc} is the specific contact resistance per unit area of the metal-semiconductor interface (units of Ω-cm^2), and ρ_{bs} is the base sheet resistivity (units of $\Omega/\square$). The gap resistance is given by

$$R_{gap} = \rho_{bs}W_{gap}/2l \tag{6}$$

where W_{gap} is the separation between the emitter mesa and the base Ohmic contact. The spreading resistance is given by

$$R_{spread} = \rho_{bs}W_e/12l. \tag{7}$$

For HBTs fabricated with a self aligned base-emitter process, $W_{\text{gap}} \simeq 0.1$ μm and R_{gap} is negligible. We note also that R_{spread} is proportional to the emitter width W_e, but that R_{contact} is independent of W_e. Hence, for narrow-emitter devices, the base resistance is dominated by R_{contact} and is only weakly dependent upon W_e. The traditional "base spreading resistance" is not an appropriate description for the r_{bb} of a typical narrow-emitter HBT. The total collector base capacitance is given by

$$C_{cb} = \epsilon l W_c/T_c \tag{8}$$

where, W_c is the width of the collector (= width of the base mesa), l is the length of the emitter stripe and T_c is the thickness of the collector depletion region. Hence, C_{cb} is proportional to the width of the base mesa which in turn is much wider than, and, independent of W_e. Note that only a fraction C_{cbi} of C_{cb} is charged through the base resistance r_{bb}. Determination of the C_{cbi}/C_{cb} ratio from the HBT physical dimensions has not been fully explored in the literature. We estimate that

$$C_{cbi} \simeq \epsilon l(W_e + 2W_{gap} + 2l_{contact})/T_c \tag{9}$$

where

$$l_{contact} = \sqrt{\rho_{bc}/\rho_{bs}} \tag{10}$$

is the transfer length of the base Ohmic contact. This approximation is based upon taking the fraction of C_{cb} whose charging current shares a common path through the base with the currents associated with charging C_{be}. We note that the collector-base junction area of double-mesa HBTs is further increased by the presence of a base contact pad area necessary to bring interconnect metallization onto the base Ohmic metal. Lateral scaling below ~ 1 μm does not substantially improve the bandwidth of double-mesa HBTs.

We have developed a transferred-substrate HBT which can be scaled laterally to improve bandwidth[25]. The cross-section of a transferred-substrate HBT is shown in Fig. 4. Transferred-substrate HBTs have lithographically defined narrow emitter and collector stripes aligned to each other on opposite sides of the base epitaxial layer[26]. This is the special feature of the transferred-substrate HBT in contrast

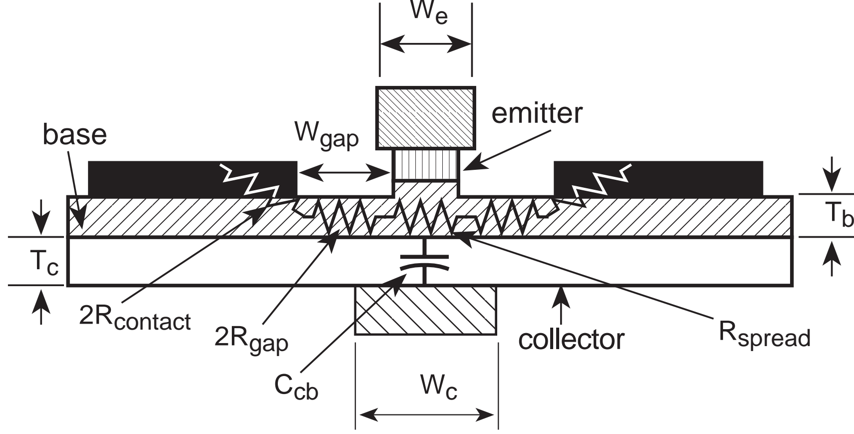


Figure 4: Schematic cross-section of a transferred-substrate HBT.

to the double-mesa HBT. The fabrication of transferred-substrate HBTs requires access to the emitter and the collector sides of the epitaxial film. The process of substrate transfer allows this access and is an essential step in the fabrication process.

The base resistance is dominated by R_{contact} and is independent of W_e, as for the double-mesa HBTs. The collector-base capacitance C_{cb} is proportional to the width of the collector stripe W_c, if fringing capacitance is negligible (Fig. 4); $C_{cb} = \epsilon l W_c/T_c$, where l is the length of the collector or the emitter stripe and T_c is the thickness of the collector depletion region. If a constant ratio is maintained between the emitter and the collector widths, C_{cb} is proportional to the emitter width W_e. Noting that $r_{bb} \simeq R_{\text{contact}} = \sqrt{\rho_{bc}\rho_{bs}}/2l$, and $C_{cb} = \epsilon l W_c/T_c$ (where $W_c \propto W_e$), the $r_{bb}C_{cb}$ time constant is proportional to W_e. This, when used in Eq. (4) yields the relationship

$$f_{cb} \propto \frac{1}{W_e}. \tag{11}$$

Using Eq. (11) in Eq. (3), it is observed that the maximum frequency of oscillation f_{max} depends on W_e as

$$f_{max} \propto \frac{1}{\sqrt{W_e}}. \tag{12}$$

Hence, f_{max} rapidly improves with submicron lateral scaling of the device.

The cross-section of the transferred-substrate HBT in Fig. 4 shows a direct Schottky contact to the collector depletion layer. An Ohmic collector contact having the same width as the Schottky contact will also show the same variation of f_{max} with scaling. The two devices are almost identical except for an extra potential drop across the collector-base junction of the Schottky-collector device. This potential drop, due to the Schottky contact, is the difference between the work function of

the metal Schottky contact and the electron affinity of the collector semiconductor. A Schottky collector contact provides a slight improvement in f_τ because of the absence of a collector contact resistance (Eq. (2)). It is also easier to fabricate deep submicron Schottky collector contacts (e.g. 0.1 μm T-gate) than deep submicron Ohmic contacts.

The scaling law of Eq. (12) suggests that the operating bandwidth of HBTs can be increased without bounds by lithographic scaling alone. In fact, to obtain usable devices, vertical scaling of the epitaxial layer thicknesses must accompany the lithographic scaling. Except in the case of reactively-matched amplifiers and distributed circuits where f_{max} is the sole determinant of circuit bandwidth, both f_τ and f_{max} are generally important for optimum circuit performance in a given technology. Devices with $f_{max} \ll f_\tau$, obtained by thinning the epitaxial layers *without* lateral lithographic scaling will show circuit bandwidth determined by r_{bb} and C_{cb}. Devices with $f_{max} \gg f_\tau$ (e.g. devices with relatively thick epitaxial layers and significant lateral lithographic scaling) will show circuit bandwidth dominated by $(\tau_b + \tau_c)$. Reduction of $(\tau_b + \tau_c)$ is obtained by thinning the epitaxial layers, which unfortunately increases $r_{bb}C_{cb}$. The transferred-substrate HBT allows for the subsequent reduction of $r_{bb}C_{cb}$. A device having high values for *both* f_τ and f_{max} is thus possible.

Several approaches have been reported for reducing the collector-base capacitance of HBTs, and thereby improving f_{max}. One approach is the reduction of the width of the base mesa[27]. This relies on improvements in base contact technology because a narrow base mesa results in a smaller base Ohmic contact area. The base contact width must be at least one transfer length if the contact resistance is to be kept small. In contrast, the transferred-substrate technique provides independent control of the base and collector contact widths. There have been other approaches to make the collector contact width independent of the size of the base mesa, such as selective etching to undercut the collector[28], collector isolation implant[29], contacting the base with a very narrow L-shaped contact[30], and selective lateral oxidation of the emitter[31] for a collector-up growth. However, for deep submicron scaling, powerful fine-line lithography is likely to be the technique of choice for defining the collector and emitter contacts of HBTs.

In addition to high device bandwidths, integrated circuit processes must incorporate a low capacitance wiring environment and low ground return inductance. Wire lengths, and hence, transistor spacings must be small. Given that fast HBTs operate at $\sim 10^5$ A/cm^2 current density, efficient heat sinking is then vital. The transferred-substrate HBT IC process[32] uses benzocyclobutene (BCB), a low-loss, low dielectric-constant ($\epsilon_r = 2.7$), spin-on dielectric as the substrate for microstrip interconnects, thus providing low capacitance. The thin ($\simeq 10$ μm) BCB substrate with a gold ground plane underneath also provides low inductance ground vias. Transistor heat-sinking is through electroplated gold thermal vias.

2. Fabrication

The AlInAs/InGaAs material system was chosen for the fabrication of transferred-substrate HBTs. The HBT epitaxial layer structure (Fig. 5(a)) is grown by molecular beam epitaxy on a Fe-doped semi-insulating (100) InP substrate, starting with a 2500 Å AlInAs buffer layer. The GaInAs collector is 2700 Å thick, is Si-doped at $1\times10^{16}/\text{cm}^3$ and contains a $5\times10^{11}/\text{cm}^2$ Si pulse-doped layer 400 Å from the base. This pulse-doped layer delays the onset of base push-out[33]. The 500 Å GaInAs base is graded in both doping and bandgap. The 100 Å of the $Ga_{0.47}In_{0.53}As$ base immediately adjacent to the collector is Be-doped at $3\times10^{19}/\text{cm}^3$. The remaining 400 Å of the base is Be-doped at $5\times10^{19}/\text{cm}^3$. By increasing the Ga cell temperature progressively during growth of the 400 Å layer, the Ga:In ratio is gradually increased, introducing a ~ 0.03 eV bandgap gradient across the 400 Å layer. The base is then graded in 300 Å to the AlInAs emitter. The first 66 Å of the grade is Be-doped at $2\times10^{18}/\text{cm}^3$ and the remainder is Si-doped at $8\times10^{17}/\text{cm}^3$. The AlInAs emitter is about 1350 Å thick. The first 500 Å are Si-doped at $8\times10^{17}/\text{cm}^3$ and the remainder is Si-doped at $1\times10^{19}/\text{cm}^3$. This is graded in 66 Å to the InGaAs emitter cap. The emitter cap is n^+ doped with Si at $1\times10^{19}/\text{cm}^3$.

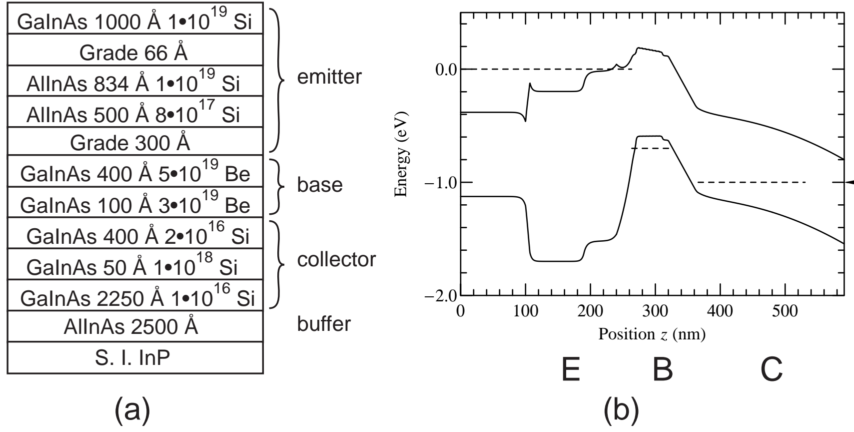
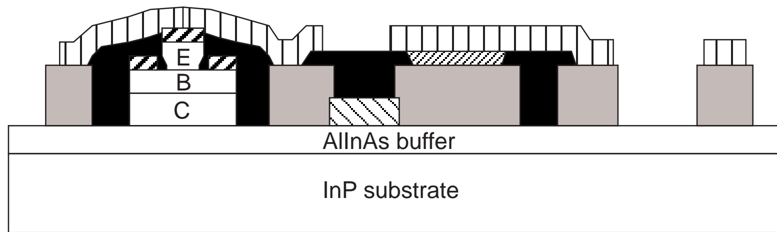


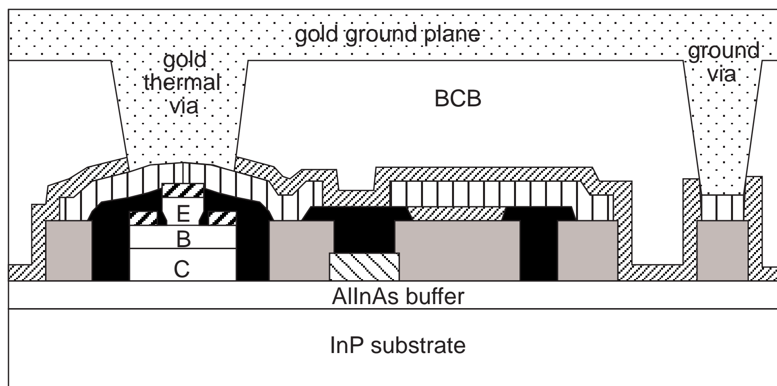
Figure 5: (a) MBE layer structure and (b) Band diagram under forward bias.

The band diagram corresponding to the layer structure of Fig. 5(a) under forward bias is shown in Fig. 5(b). The biasing conditions are as follows: base-emitter voltage $V_{BE} = 0.7$ V, collector-emitter voltage $V_{CE} = 1.0$ V, and a emitter current density of 1×10^5 A/cm^2. The collector current density is assumed to be the same as the emitter current density, as is the case of a narrow-collector HBT. The effect of the electrons in the collector space charge layer due to the collector current is included while calculating the electric field and the electrostatic potential in the collector space charge layer. An electron velocity of 3×10^5 m/s is assumed in these calculations.

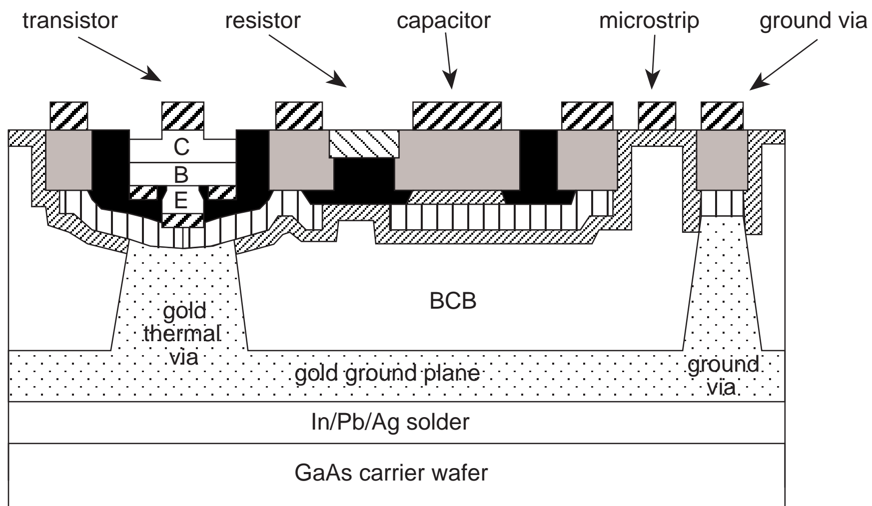
Fig. 6 shows sequentially, the steps involved in fabrication of transferred-substrate



(a)



(b)



(c)

Figure 6: Fabrication process for transferred-substrate HBTs.

HBTs. The fabrication process starts with the evaporation of Ti/Pt/Au emitter contacts. A combination of a dry etch, a selective wet etch, and a non-selective wet etch is then used to etch down to the base epitaxial layer. Fig. 7 shows a SEM photomicrograph of the device cross-section after this step. The non-selective wet etch causes a lateral undercut and reduces the emitter-base junction area to below the lithographically defined area as seen in this cross-section.

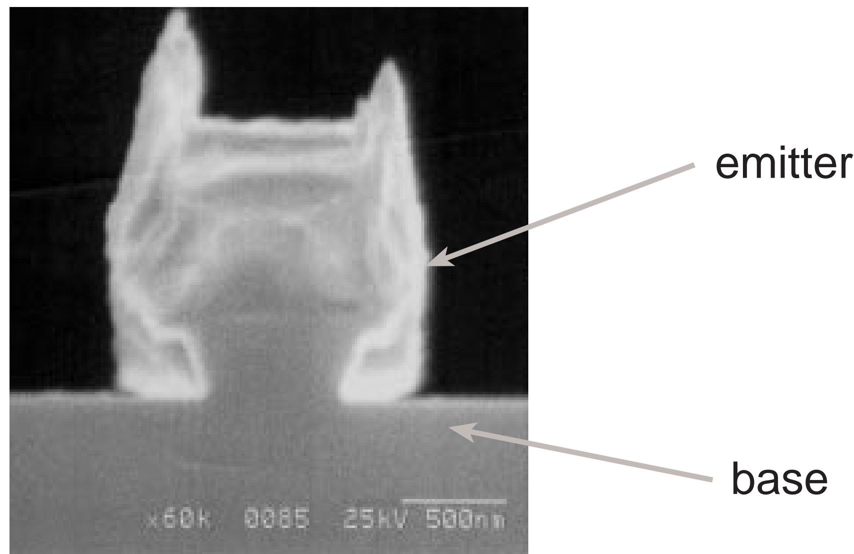


Figure 7: SEM cross-section of device after emitter-base etch.

Self-aligned Ti/Pt/Au base metal is evaporated and sintered at 300 °C for 1 minute. Transistors are then isolated by forming mesas using a dry etch, stopping on the AlInAs buffer layer. Thin film NiCr is evaporated on the wafer to form resistors with 50 $\Omega/\square$ sheet resistivity. The first level of metallization (metal1) is done at this point. This metal forms most of the transmission lines, interconnect wiring, probe pads, capacitor bottom plate and resistor contacts. The devices are passivated and planarized with polyimide. Polyimide also passivates the NiCr resistors and serves as interconnect crossovers for multiple wiring levels. The capacitor dielectric (1000 Å SiN) is then deposited and etched away in unwanted regions. Emitters and bases are contacted by electroplated Au. The electroplated Au also forms the second level of metallization (metal2) and the top plate for MIM capacitors. The process at this point is shown in Fig. 6(a). Fig. 8(a) shows a photomicrograph of a device after this step.

The substrate transfer process starts with the deposition of a 4000 Å SiN (insulator) layer by PECVD which serves to insulate the wafer. The wafer is then coated with a thick layer of Benzocyclobutene (BCB, $\epsilon_r = 2.7$). Thermal vias are formed on the emitters by dry etching openings in the BCB. This also etches the SiN insu-

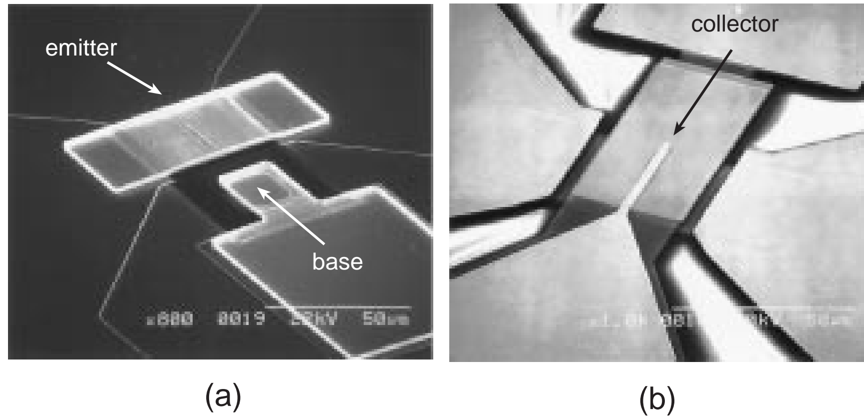


Figure 8: SEM photomicrograph of device after (a) partial fabrication and (b) complete fabrication.

lator layer in the vias. The vias are then filled with thick Au by electroplating. The electroplated Au also forms an electrically and thermally conducting ground plane, thus grounding all emitters. Ground vias are also formed in this step. Microstrip interconnect lines on BCB provide a low-capacitance environment wiring for dense circuits. Ground vias to the thick electroplated ground plane provide low ground return inductance. Thermal vias provide efficient heat-sinking for devices operating at very high current densities. Fig. 6(b) shows the process at this point.

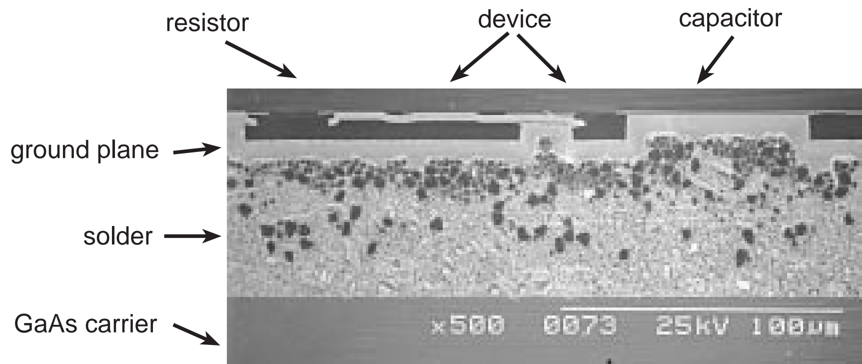


Figure 9: SEM photomicrograph of cross-section through an IC.

The wafer is then inverted and bonded to a GaAs transfer substrate. The InP substrate is removed in an aqueous solution of HCl. The AlInAs buffer layer is also removed by the same etch. This etch stops selectively on the InGaAs collector layer. Ti/Pt/Au Schottky collector contacts are then deposited. Outside the active

collector area, 1500 Å of the collector drift region are then removed by a self-aligned wet etch to reduce fringing capacitance. The process at this step is shown in Fig. 6(c). Fig. 8(b) shows a photomicrograph of a completed device. Fig. 9 shows a SEM photomicrograph of the cross-section of an integrated circuit with active and passive components.

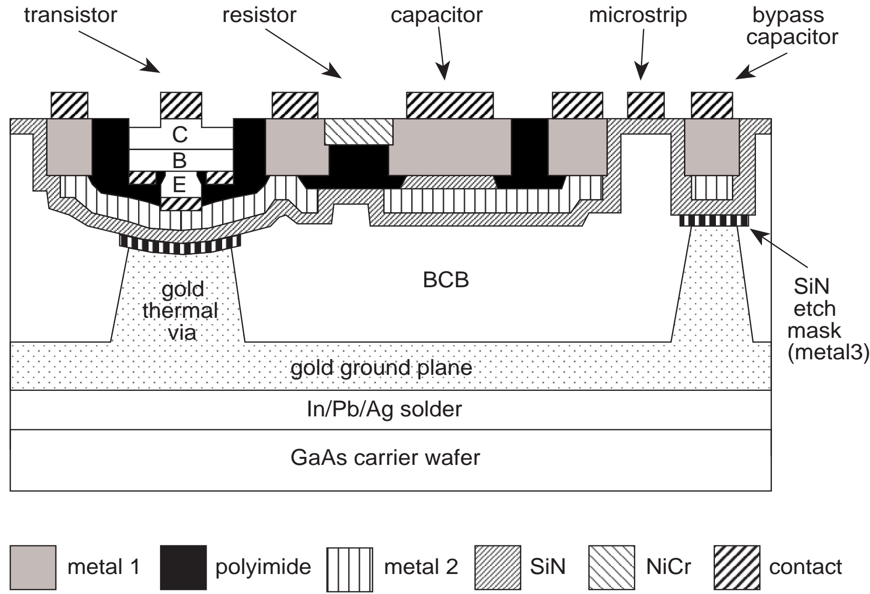


Figure 10: Fabrication process for devices with non-grounded emitters.

Transistors with non-grounded emitters (required in ICs) are fabricated by protecting the SiN insulator with a metal layer (Fig. 10) before applying BCB. Without this layer, the SiN insulator is removed during the via formation etch. This metal layer (metal3) also forms power supply bypass capacitors and forms a third level of metallization. Fig. 11 shows a SEM photomicrograph of the cross-section of a fully fabricated device with a non-grounded emitter.

Devices with non-grounded emitters should have similar performance and heat-sinking as the devices with grounded emitters. SiN has $\epsilon_r = 6$ and $\sim$ 10-30 W/m-K thermal conductivity. For an HBT with a 0.6×25 μm^2 emitter, the thermal via is 10×24 μm^2. For non-grounded emitter devices, the calculated capacitance from the emitter airbridge to the grounded substrate is 25 fF, which is much smaller than 730 fF base-emitter capacitance. The calculated 67-200 K/W thermal resistance of the SiN layer should result in less than 3.5 °C additional temperature rise for a device biased at 10^5 A/cm^2 and 1.0 V.

For integrated circuit applications, high device yield is required. The transferred-substrate HBT IC technology is being improved towards this goal. The technology is currently capable of yielding circuits with few transistors. Fig. 12 shows a pho-

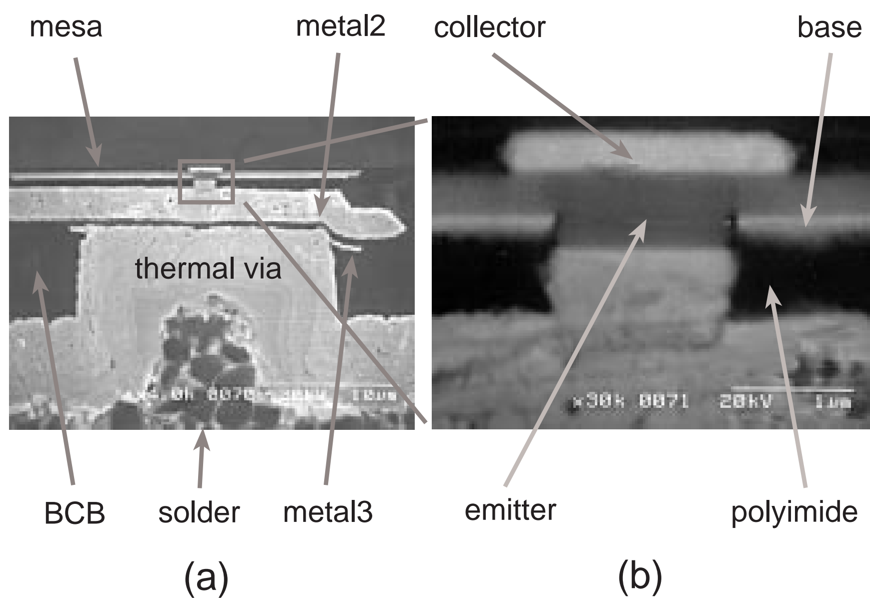


Figure 11: SEM photomicrograph of (a) cross-section through a device and (b) close-up of intrinsic device.

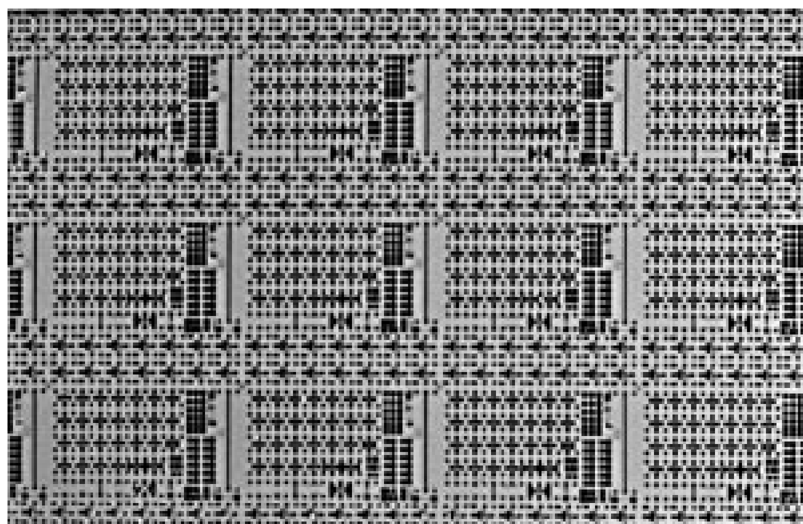


Figure 12: Photomicrograph of part of a wafer with ICs and discrete devices.

tograph of part of a wafer with discrete devices and small integrated circuits.

The device and circuit results reported here are from different wafers with small variations in the MBE layer structure and the fabrication process, and do not significantly affect the central theme of this work.

3. DC and RF Measurements

A variety of devices have been fabricated with different emitter and collector widths. It is important in characterization to determine the emitter-base and collector-base junction areas fairly accurately. Wet chemical etches with lateral undercuts are used to reduce both the emitter-base and collector-base junction areas to below their lithographically defined dimensions. Junction dimensions are determined by measuring (with a microwave network analyzer) the junction capacitances vs. the lithographically defined junction widths. Devices were fabricated with 0.6 μm $\times$ 25 μm emitters and with collector dimensions of 0.8 μm $\times$ 29 μm (narrow-collector) and 1.8 μm $\times$ 29 μm (wide-collector). Devices with very wide collectors ($\sim$ 5 μm), as is normally the case in double-mesa HBTs, were also fabricated. All devices have their emitter grounded by thermal vias, except where explicitly stated. While most of the data presented here is for the above devices, some data will also be presented from devices with different geometries and configurations.

3.1. *DC measurements*

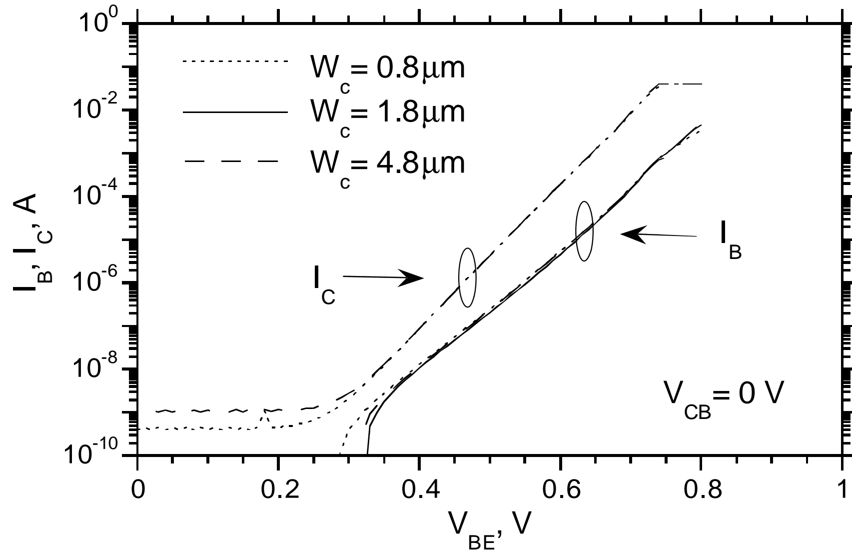


Figure 13: Gummel plots of transferred-substrate HBTs with 0.6 μm $\times$ 25 μm emitters and different collector widths.

Fig. 13 shows the Gummel plots for transferred-substrate HBTs with the three

different collector widths. The independence of these plots to collector width can be observed. The collector current ideality factor n_c is close to unity. The base current ideality factor n_b is 1.2.

DC common-emitter characteristics of the HBTs are shown in Fig. 14. The small signal current gain at DC, β, is 55. At high current densities, narrow-collector devices show significantly larger collector-emitter saturation voltages ($V_{CE,sat}$), arising from screening of the collector electrostatic field by the electron space charge. Screening occurs at a *collector* current density J_C satisfying the relationship $(V_{CB}+\phi) = T_C^2(J_C/v_{sat} - qN_d)/2\epsilon$, where T_C is the collector depletion layer thickness, N_d the collector doping, ϕ the junction built-in potential, and v_{sat} the electron velocity. In wide-collector HBTs, there is significant lateral spreading of the electron flux at high current densities[34], reducing the collector space-charge density. Lateral current confinement in narrow-collector HBTs results in both increased $V_{CE,sat}$ and decreased emitter current density at the onset of f_τ collapse (Kirk effect), resulting in increased emitter charging times and reduced f_τ.

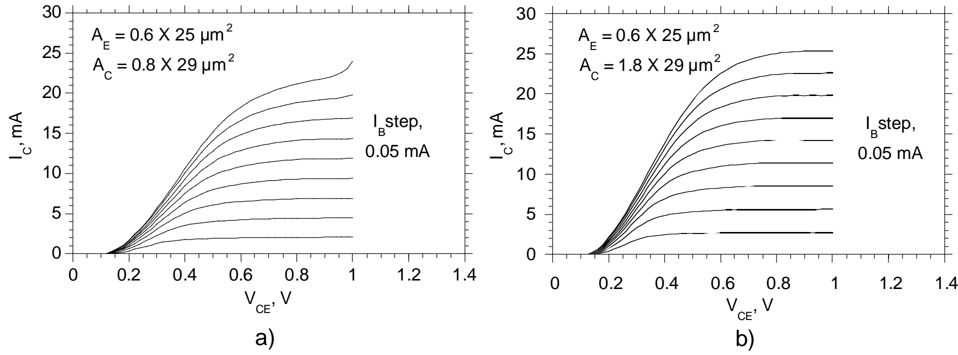


Figure 14: DC common-emitter characteristics of devices with (a) narrow collector and (b) wide collector.

The common-emitter breakdown voltage BV_{CEO} is ~3 V, decreasing to 1.5 V at 10^5 A/cm^2. The low breakdown voltage is due to the narrow-bandgap InGaAs collector material. InP collectors with a InGaAs/InAlAs linear grade would provide superior breakdown[35]. Our current facilities do not permit InP growth. Given that vertical scaling must accompany lateral scaling to obtain commensurate improvement in both f_τ and f_{max}, scaled 0.1 μm devices will demand very thin (1500-2000 Å) collectors, and InP must be employed.

DC characteristics of the devices with 0.6 μm $\times$ 25 μm emitters and 1.8 μm $\times$ 29 μm collectors were measured in the common-base configuration also. Fig. 15 shows these characteristics. The common base current gain α is 0.98. The common-base breakdown voltage BV_{CBO} is ~ 6 V, decreasing to 1.5 V at 10^5 A/cm^2.

We now compare the DC characteristics of devices with non-grounded emitters (with thermal vias) and devices without thermal vias. Three devices are compared.

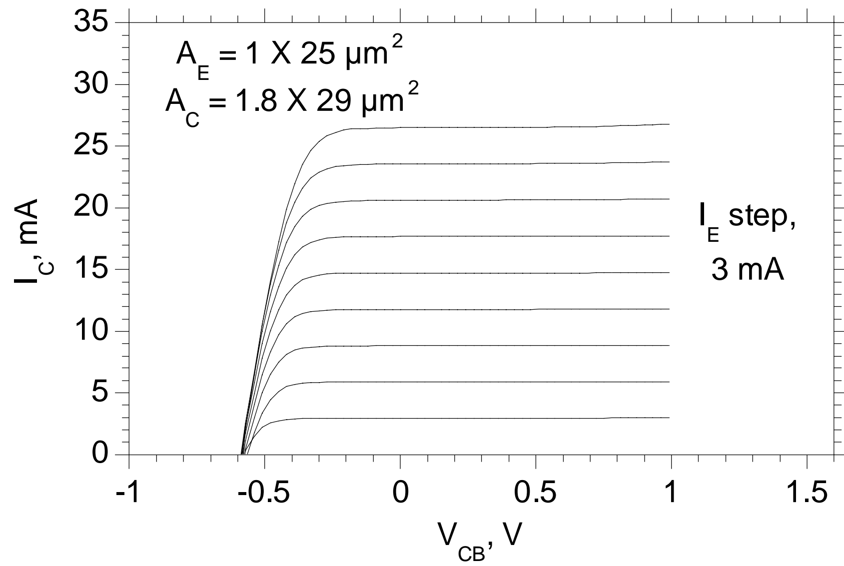


Figure 15: DC common-base characteristics of devices.

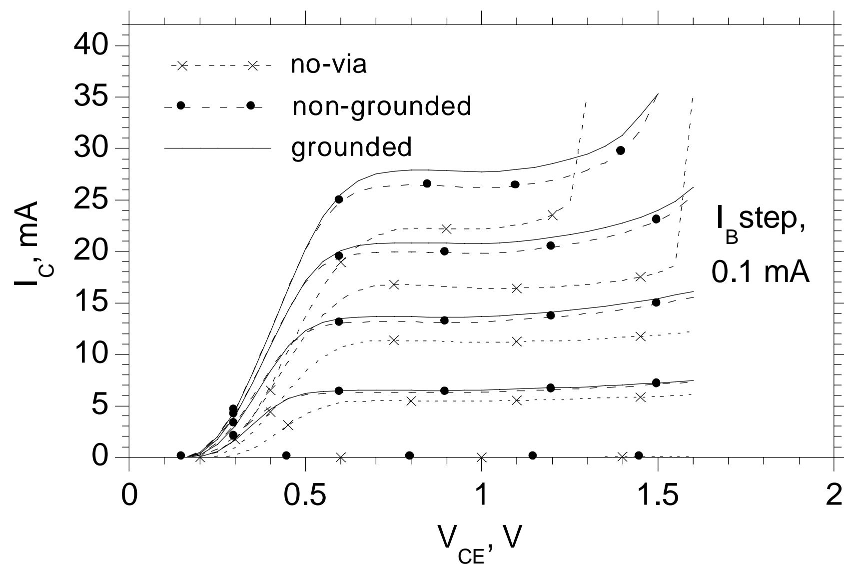


Figure 16: DC common-emitter characteristics of device with different heatsink structures; $A_E = 1\ \mu m \times 25\ \mu m,\ A_C = 4.8\ \mu m \times 29\ \mu m$.

All have 1 μm $\times$ 25 μm emitters and 4.8 μm $\times$ 29 μm collectors. The first device has its emitter grounded with a thermal via (grounded), the second device has metal 3 to protect the insulator layer (non-grounded), and, the third device does not have a thermal via (no-via). Fig. 16 shows their common-emitter characteristics. There is very little difference between the grounded and non-grounded devices, as was expected from the temperature calculations in the previous section. The no-via device has lower breakdown voltage and lower current gain due to self-heating effects. Hence, a thermal via is essential for high power operation.

3.2. *RF measurements*

The devices were characterized by on-wafer network analysis to 50 GHz. Fig. 17 shows the short-circuit current gain h_{21}, maximum stable gain (MSG), and Mason's[36] invariant (unilateral) power gain U. Pad parasitics have not been stripped. Bias conditions are as shown. Extrapolating at -20 dB/decade, f_{max} = 400 GHz and f_τ = 164 GHz for the wide-collector devices (Fig. 17(b)). The high f_{max} is due to the reduced $r_{bb}C_{cb}$ time constant due to low resistance base Ohmic contacts and the low intrinsic collector-base capacitance. We have used Mason's gain for extrapolating f_{max} because of its characteristic -20 dB/decade slope, its independence of the transistor configuration (common-base vs. common-emitter), and its independence of pad inductive and capacitive parasitics.

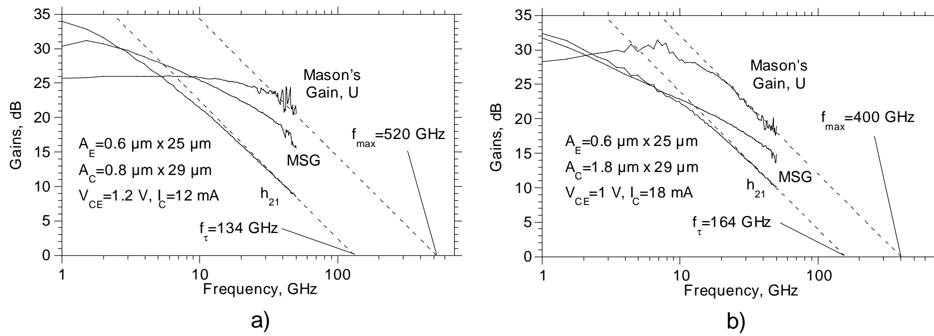


Figure 17: RF characteristics of devices with (a) narrow collector and (b) wide collector.

RF measurements (Fig. 17(a)) of the narrow-collector devices yield 134 GHz f_τ and 520 GHz extrapolated f_{max}. Such measurements are however at the limits of reliability for a 50 GHz instrument. We now estimate f_{max} by calculation from $f_{max} \simeq \sqrt{f_\tau / 8\pi r_{bb} C_{cbi}}$. Here C_{cbi} is the intrinsic base-collector capacitance, the fraction of C_{cb} charged through the base resistance r_{bb}. R_{bb} consists of sheet resistance and contact resistance (neglecting gap resistance). The measured base sheet resistance is 600 $\Omega/\square$. Because of poor test structure design, the specific base Ohmic contact resistivity falls below levels which can be reliably measured by

the (TLM) test structures employed on the present wafer, and we therefore take reported values of specific contact resistivity for test structures ($23\ \Omega - \mu m^2$)[37] having similar levels of Be-doping. With these parameters, we calculate a 2.4 Ω base spreading resistance and a 2.4 Ω base contact resistance. C_{cb} is extracted from s-parameter measurements by plotting the imaginary part of the reverse admittance parameter y_{12} vs. frequency. The C_{cbi}/C_{cb} ratio is not readily predicted from device geometry[38], but is often fitted by comparing measured and modeled s-parameters. Here, we roughly estimate the C_{cbi}/C_{cb} ratio as being equal to the ratio of the emitter-base and collector-base junction areas. For wide-collector devices, measured $f_\tau = 164$ GHz, $C_{cb} = 22.7$ fF, $C_{cbi} = 7.5$ fF and $f_{max} = 426$ GHz. For narrow-collector devices, $f_\tau = 134$ GHz, $C_{cb} = 8.2$ fF, $C_{cbi} = 6.2$ fF, and $f_{max} = 423$ GHz. Both the above calculations and the microwave measurements indicate that f_{max} is at least 400 GHz. The MSG is given by

$$MSG = \parallel s_{21}/s_{12} \parallel \simeq (\omega C_{cb})^{-1}(r_{ex} + (kT/qI_E))^{-1} \qquad (13)$$

and is higher for the narrow-collector devices because of the reduced C_{cb}.

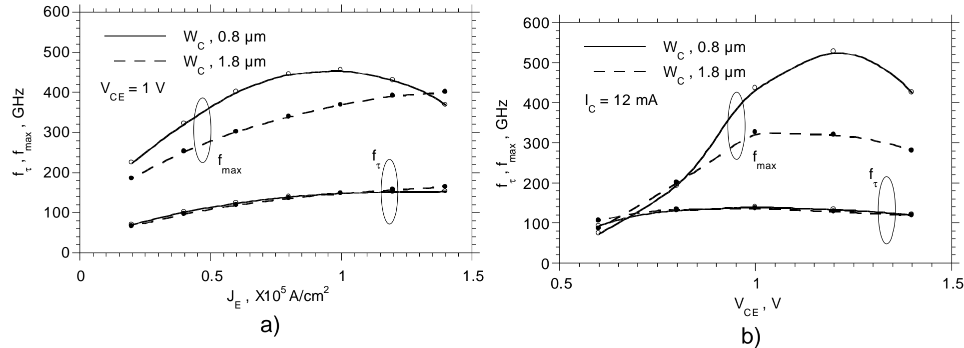


Figure 18: Variation of f_τ and f_{max} with (a) emitter current density and (b) collector-emitter voltage.

Fig. 18 shows the variation of f_τ and f_{max} with bias. F_τ is similar for both devices. The Kirk effect threshold is high due to the presence of the pulse-doped layer in the collector close to the base[33]. The narrow-collector devices exhibit the Kirk effect at lower current density than wide-collector devices. Fig. 18(b) shows a plot of f_τ and f_{max} vs. collector-emitter voltage, V_{CE}. At low V_{CE}, the collector is partially depleted leading to increased C_{cb} and reduced f_{max}. At high V_{CE}, f_τ and f_{max} decrease, suggesting a decrease in the collector electron velocity at high electric fields. By plotting $1/2\pi f_\tau$ vs. $1/J_E$, it is determined that the sum of the base and collector transit times ($\tau_b + \tau_c$) is 0.75 ps.

Fig. 19 shows how lateral scaling is achieved by transferred-substrate HBTs. Shown in the figure is the variation of f_τ and f_{max} with emitter current density for

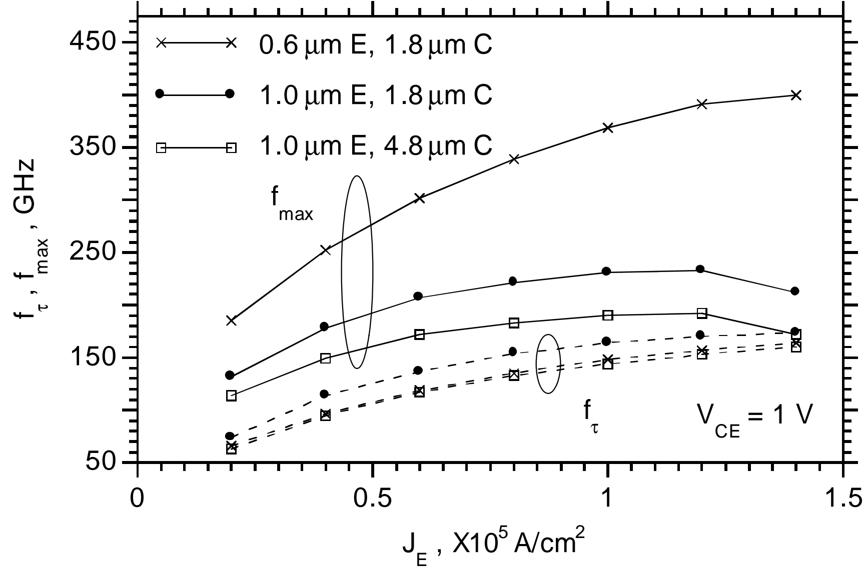


Figure 19: Variation of f_τ and f_{max} with J_E for devices with different geometry.

three different devices. The first one has a 1 μm $\times$ 25 μm emitter and 4.8 μm $\times$ 29 μm collector. The second one has the same emitter but a narrower 1.8 μm $\times$ 29 μm collector. The third one has the same collector as the second one but a narrower 0.6 μm $\times$ 25 μm emitter. From Fig. 19 we can see that f_τ is similar for all three devices. Some difference is present due to the $r_{ex}C_{cb}$ term in the expression for f_τ (Eq. (2)). Reducing the collector width alone does not significantly improve f_{max}, as the intrinsic part of the collector-base capacitance remains the same. Scaling both the emitter and the collector improves f_{max} by a large amount. These devices are from different wafers, and thus have slightly different parameters, but the general scaling trend can clearly be observed here. It is expected that with further submicron scaling of the emitter and collector dimensions, a f_{max} much higher than 400 GHz can be obtained.

A small-signal hybrid-π model of the transferred-substrate HBT was developed and is shown in Fig. 20. The device with 0.6 μm $\times$ 25 μm emitter and 1.8 μm $\times$ 29 μm collector was used as a representative device because of good RF and DC characteristics suitable for circuit design. All the parameters except r_{ce} were extracted from bias dependence of s-parameters rather than being fitted on a computer. The C_{cbi}/C_{cb} ratio is determined as described above. Pad parasitics are negligible. This model is simple enough to facilitate quick circuit design and analysis, and also provides a reasonable fit to the measured s-parameters. We note that it is difficult to fit measured HBT s-parameter data to a hybrid-π model for any HBT operating close to the Kirk threshold. Charge-control analysis of an HBT operating in the

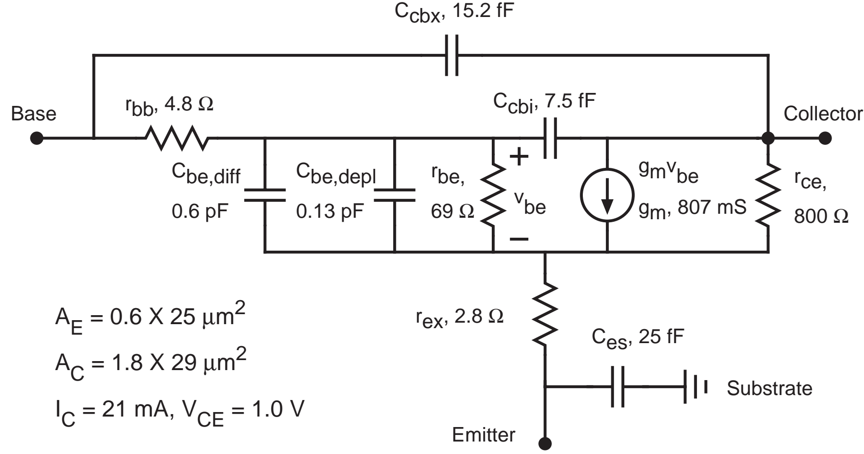


Figure 20: Small-signal hybrid-pi model of a transferred-substrate HBT.

region of collector field screening indicates that the base stored charge is modulated by the collector potential, an effect not modeled in the hybrid-π circuit.

4. Integrated Circuits

Transferred-substrate HBTs have been shown to have excellent high-frequency performance[39] and have great potential for future high frequency analog, digital, and mixed-signal integrated circuits. Analog circuits of interest include preamplifiers, variable-gain amplifiers, broadband traveling-wave amplifiers, voltage controlled oscillators and mixers. Digital circuits like D-flip-flops, frequency dividers, multiplexers/demultiplexers, selectors, digital phase-locked loops are being developed. In the mixed-signal category, analog-digital data converters are very important applications and are under development.

For integrated circuit applications, the process must have very high device yield and uniformity of DC and RF parameters. In addition to a high-performance device, there are other critical ingredients of a IC technology. Some of these are: passive components like resistors and capacitors, low-loss transmission lines, a low-capacitance multiple-level wiring environment, low ground return inductance vias and good heat-sinking. The transferred-substrate HBT technology has these key features as explained in the fabrication process. Device yield and uniformity is currently at levels suitable for fabricating circuits with few devices and is constantly being improved.

4.1. *Analog circuits*

The first demonstration integrated circuit to be fabricated in this technology was a feedback amplifier[40]. Feedback amplifiers are suitable for technology demonstra-

tion because of their simple design, low integration levels, few passive components and easy testability. A Darlington amplifier with series and shunt resistive feedback and 50Ω input/output impedance[41] was designed and fabricated.

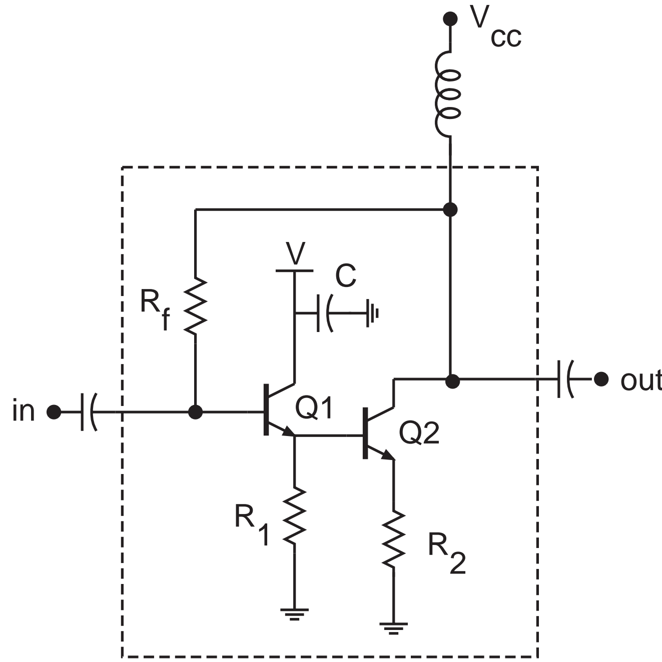


Figure 21: Circuit diagram of Darlington feedback amplifier.

Fig. 21 shows a schematic circuit diagram of the amplifier. The dotted line shows the chip boundary. Q1-Q2 form the Darlington pair. The emitter stripe lengths of Q1 and Q2 are selected to maximize bandwidth. If the emitter stripe length of Q1 is large, its input capacitance is large, degrading bandwidth; if it is too small, its base and emitter resistances are large, increasing the driving impedance for Q2 and degrading bandwidth. Large Q2 emitter stripe length increases its Miller-multiplied base-collector capacitance whereas a small emitter stripe length increases the base resistance, through which the (degenerated) device input capacitance must be charged. Hence, there are optimum emitter stripe lengths for Q1 and Q2. R_f, the shunt feedback resistor, is chosen to provide an input impedance of 50Ω. R_1 is the series feedback resistor in the emitter of Q1 and sets the Q1 emitter current density close to peak f_τ bias. R_2 sets the degenerate transconductance of Q2 (and hence of the circuit) to provide the desired gain and 50Ω output impedance. The circuit is biased with V_{CC} and an off-chip resistor connected through a bias-tee at the output. The collector of Q1 is not connected to the output, but is biased with and independent supply to eliminate Miller multiplication of its base-collector

capacitance. The IC consumes 46 mW DC power. Fig. 22 shows a photograph of the amplifier. The chip dimensions are 0.4 mm $\times$ 0.37 mm.

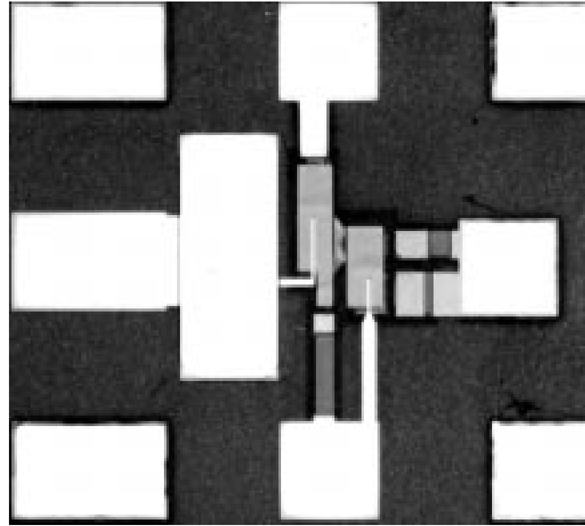


Figure 22: Photograph of the amplifier IC (0.4 mm $\times$ 0.37 mm).

The amplifier characteristics were measured with a network analyzer to 50 GHz. Fig. 23(a) shows the forward gain s_{21} of the amplifier. The low-frequency gain is about 13 dB and the 3-dB bandwidth (relative to the low-frequency gain) is 50 GHz. The gain peaking at high frequencies is due to the second (internal) pole in the feedback loop created by the emitter resistance of Q1 and the base resistance and input capacitance of Q2.

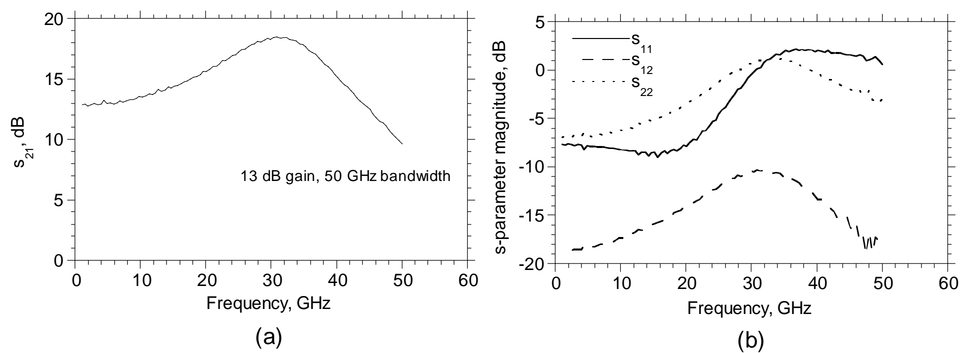


Figure 23: Measured amplifier characteristics: (a) forward gain, and (b) return losses and reverse isolation.

The bandwidth is below the potential of the HBT technology for several reasons. First, f_{max} is low on the current ICs due to high base Ohmic contact resistance. Secondly, the resistor current carrying capability was lower than expected, forcing us to bias the transistors at less than the intended design conditions. At the bias conditions at which the amplifier measurements were taken, the transistor f_τ and f_{max} are 120 and 175 GHz respectively. Fig. 23(b) shows the input and output return losses and the reverse isolation of the amplifier. Technology, device, and circuit design improvements are currently underway, and are expected to yield amplifiers with higher bandwidths.

Other circuits currently in development are broadband traveling-wave amplifiers, variable gain amplifiers, optical receiver preamplifiers and monolithic VCOs. Target applications include fiber-optic transmission systems for 40 and 100 Gbits/s and radar links.

4.2. *Digital circuits*

Digital circuits typically require higher levels of integration than analog circuits. Fig. 24 shows a SEM photomicrograph of a transferred-substrate HBT digital technology in development. Master-slave D-flip-flops, both in ECL and CML configurations, with projected clock rates of 80 GHz have been designed. D-flip-flops are building blocks for a variety of digital circuits. Target applications include direct digital frequency synthesizers, MUX/DEMUX and clock-data recovery circuits for wireless LANs and radar links.

5. Future Work

We have demonstrated *scalable* transferred-substrate HBTs with very high f_{max} in a IC technology. A demonstration IC in this technology has been shown. A variety of circuits have been designed and are currently in development. Current efforts seek to improve the process technology and device performance. Scaling of emitter and collector dimensions to deep submicron dimensions is being pursued to achieve f_{max} in the region of 700 GHz. Vertical scaling including reducing the base and collector layer thicknesses to improve f_τ is in progress. To improve the breakdown voltage, wide bandgap InP must be incorporated into the collector. Devices with Ohmic collectors instead of Schottky collectors are being developed to facilitate low V_{CE} operation for CML digital circuits. Improved heat spreading in resistors with high thermal conductivity encapsulation materials is being investigated. The substrate-transfer process involving In/Pb/Ag solder is a significant factor limiting yield, and the GaAs transfer substrate impairs heat-sinking. Substrate-transfer with a few hundred microns of electroplated high thermal conductivity copper, rather than solder, is being investigated. The thick electroplated Cu itself acts as the carrier wafer, eliminating the GaAs carrier wafer. Another major limitation to the yield is the critical alignment required between the emitter and collector on either side of the base epitaxial layer. The work presented here used a contact aligner

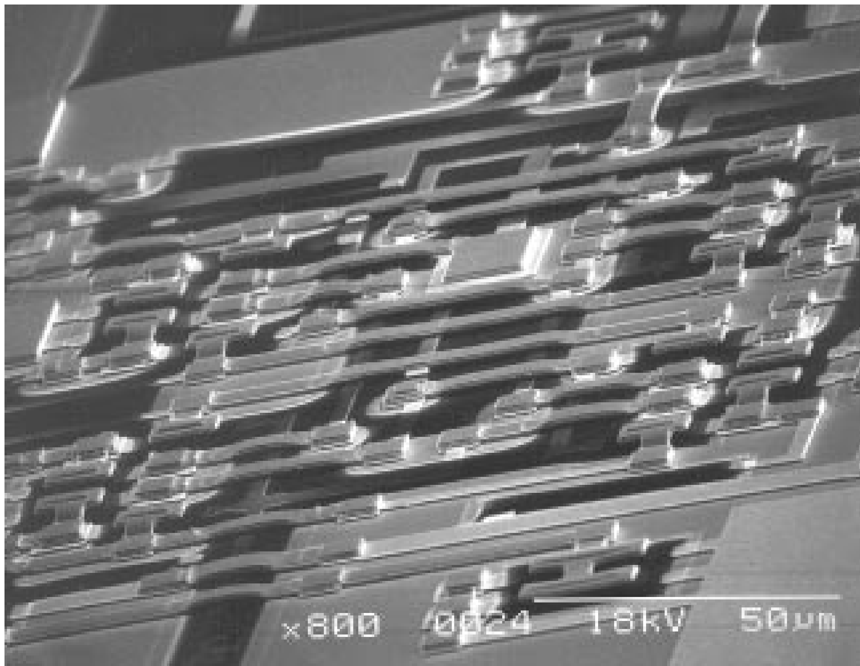


Figure 24: Transferred-substrate HBT digital IC in development.

with crude lithographic capabilities. Projection lithography systems should enable fine-line lithography and deep submicron alignment precision.

With the demonstrated high bandwidth of transferred-substrate HBTs, and with the process features delineated above, MSI-scale circuits at 100 GHz clock rates should be feasible.

Acknowledgments

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