48 GHz Static Frequency Divider in Ultrafast Transferred-Substrate Heterojunction Bipolar Transistor Technology

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Abstract

We report first digital integrated circuits in the transferred-substrate HBT technology. Emitter coupled logic (ECL) and current mode logic (CML) 2:1 static frequency dividers were fabricated. The circuits operated at a peak clock frequency of 48 GHz and 47 GHz respectively.

I Introduction

There is a growing need for high speed electronic circuits in a variety of applications including fiber-optics and multi-gigabit A/D converters. To meet this demand, a integrated circuit technology which incorporates high device bandwidth with low parasitic wiring and packaging is necessary. Transferred-substrate heterojunction bipolar transistors (HBTs) have obtained bandwidth (f_{max}) in excess of 400 GHz [1]. The transferred-substrate process offers the significant advantages of a low parasitic microstrip wiring environment with integral ground plane and a low thermal impedance environment for high power operation with increased packing density.

Analog integrated circuits in the transferred-substrate technology have obtained bandwidths of 50-80 GHz [2, 3]. The static frequency divider is the first demonstration of a high performance digital integrated circuit in the transferred-substrate technology. Static frequency dividers are critical functional elements in a variety of digital and microwave systems. These circuits are often used as benchmarks to evaluate the speed of a digital technology [4, 5].

To fabricate dense digital integrated circuits, the existing technology was modified to obtain higher device f_t and higher transistor packing density. Peak f_t and f_{max} of devices fabricated in the modified technology are 220 GHz and 470 GHz respectively. Contact lithography does not permit emitter and collector dimensions under $0.6\mu m$. The full potential of the transferred substrate process will be realized when emitters and collectors of the HBTs are scaled to deep submicron dimensions. The deep submicron devices will obtain f_{max} in excess of 600 GHz. Also, contact lithography limits current level of integration to 50-100 transistor circuits. With improvement in our existing lithographic capabilities, higher device bandwidth and higher levels of integration should be feasible.

II Device Design

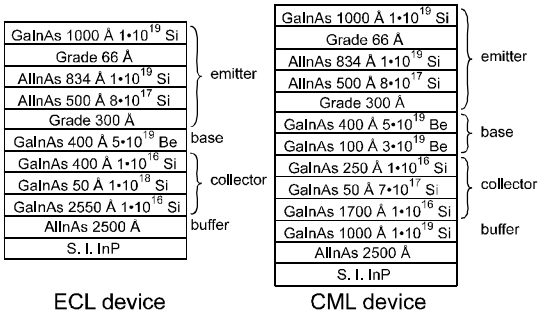

Figure 1: Epitaxial layer structures

Fig. 1 shows the epitaxial layer structures of two different devices, which are used for ECL and CML circuits respectively. In the ECL device, base thickness was reduced to $400\mathring{A}$ and base bandgap grading was increased to $2kT$. Extrinsic base-emitter capacitance was reduced by improving the process, which permits smaller extrinsic emitter contact metal and base mesa. With these changes, f_t improved from 180 GHz to 220 GHz. Fig. 2

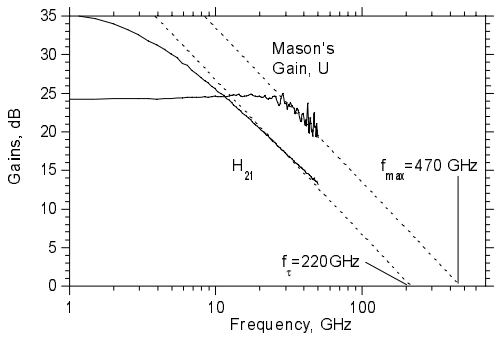

Figure 2: RF characteristics of ECL device $0.6\mu m \times 8\mu m$ emitter, $1.6\mu m \times 12\ \mu m$ collector biased at $V_{ce} = 1.1\ V$ and $I_c = 8\ mA$

shows measured RF characteristics of the ECL device. f_{max} obtained by 20 db/decade extrapolation of Masons gain is 470 GHz. This extrapolation from 50 GHz to 470 GHz is at the limit of measurement instrument bandwidth. f_{max} calculated from measured values of forward transit time, base-collector capacitance and base resistance is in excess of 400 GHz for this device. In ECL circuits the collector-emitter voltage varies between 0.7 V and 1.3 V in the switching pair and emitter followers. At $V_{ce} = 0.7\ V$ and $I_c = 8\ mA$, extrapolated f_{max} is only 140 GHz. The decrease in f_{max} from 470 GHz to 140 GHz (fig. 3) is due an increase in collector-base capacitance, caused by base pushout at low V_{cb}.

The ECL device is not suitable for CML circuits due to its poor f_t and f_{max} at V_{ce} less than 0.7 V. A variation of our original epitaxial layer structure incorporates an n+ collector contact, elimi-

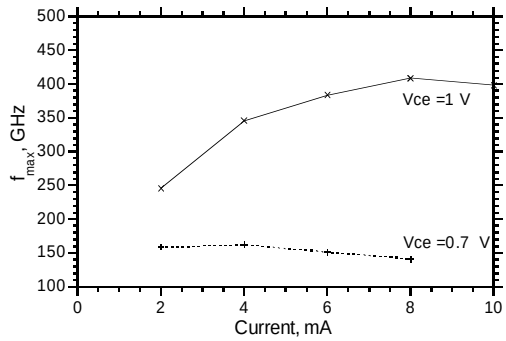

Figure 3: Variation of f_{max} with collector current for different V_{ce} in ECL device, $0.6\mu m \times 8\mu m$ emitter, $1.6\mu m \times 12\ \mu m$ collector

nating the 0.2 V drop across the Schottky collector contact. The collector thickness was reduced to $2000\mathring{A}$, reducing the voltage needed to fully deplete the collector. Also, the voltage drop induced by the launcher was reduced by decreasing the amount of n pulse doping and shifting the pulse closer to the base. Fig. 1 shows the layer structure of the CML device. Peak f_t for the CML device is 220 GHz. Reducing the collector thickness from $3000\mathring{A}$ to $2000\mathring{A}$ resulted in higher collector-base capacitance. Also, base resistance on this process run was higher. These two factors resulted in lower peak f_{max} for this device. However, f_{max} at $V_{ce} = 0.7\ V$ is higher for the CML than the ECL device(fig. 4).

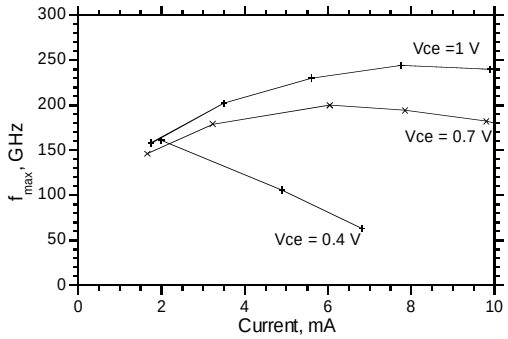

Figure 4: Variation of f_{max} with collector current for different V_{ce} in CML device $0.6\mu m \times 8\mu m$ emitter, $1.6\mu m \times 12\ \mu m$ collector

III Fabrication

To build integrated circuits, standard base-emitter processing, mesa isolation, polyimide passivation and planarization, and electroplated gold airbridge processes are followed by the transferred substrate process steps - benzocyclobutene (BCB) deposition, dry via etch and Au electroplating. Transistor epitaxial layers with thermal vias are then bonded to the transfer substrate using In/Pb/Ag solder. Collector contact metal is deposited after the InP host substrate is selectively etched away (fig. 5). In n+ subcollector HBTs, the n+ layer is etched away after collector metal deposition using collector metal as mask. The interconnects, microstrip on BCB, have a low dielectric constant for low capacitance and a ground plane for low ground-return inductance. The HBTs and passive components - NiCr resistors, SiN MIM capacitors

and two layers of gold metal wires are shown in fig. 5.

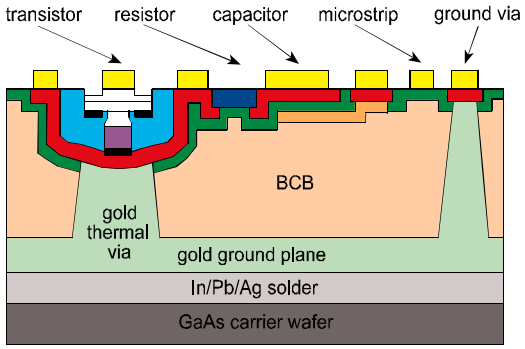

Figure 5: Cross section of integrated circuit after process

IV Circuit Design

The 2:1 static divider consists of a master-slave D-flipflop with the inverting output connected back to the data input. A standard series-gated approach with load resistance of 50 Ω is used. The circuit is fabricated with 0.6 $\mu m \times 8$ μm emitter and 1.6 $\mu m \times 12$ μm collector HBTs, operating at a current density of 0.8 $mA/\mu m^2$. The circuit is designed for a differential voltage swing of 600 mV. The slave stage directly drives a 50 Ω off-wafer load, eliminating the need for an output buffer.

In the ECL divider, emitter followers are added to buffer the upper level of switching transistors. On the lower level, the clock inputs were directly connected to switching transistors. Fig. 6 shows a photograph of the ECL static divider. The chip area of $0.6mm \times 0.6mm$ is limited by the size of the pads. The chip has single ended input and output. The second clock input was grounded on-wafer by a large capacitor.

A CML version of the static divider was also fabricated (fig. 7). CML circuits are used for their low power dissipation, relative design simplicity, and lower transistor count. The time constant involving load resistance R_L and C_{cb} limits switching speed in CML circuits designed with normal mesa HBTs. In the transferred substrate technology the extrinsic C_{cb} is small, permitting CML circuit operation at high clock rates. Peak clock speed of CML circuits fabricated in this technology is limited by the saturation characteristics of the device.

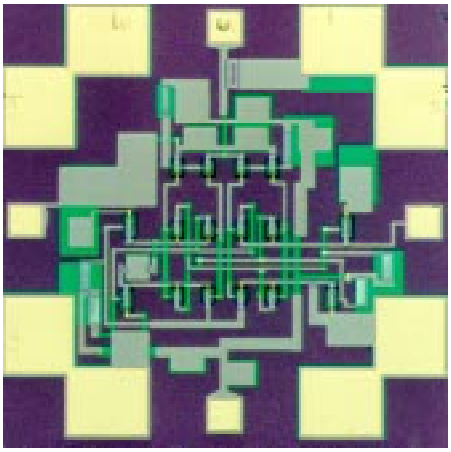

Figure 6: Chip photograph of ECL 2:1 static divider

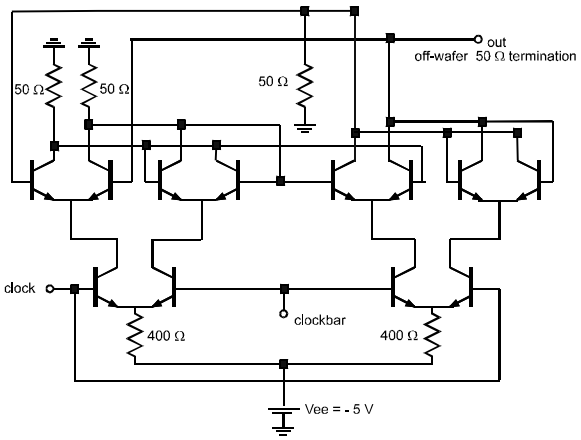

Figure 7: Circuit diagram of CML 2:1 static divider

V Results

The ECL static frequency divider operated at a maximum clock frequency of 48 GHz with a power dissipation of 380 mW from a -5 V supply. The output waveform at 24 GHz is shown in fig. 8. Fig. 9 shows the sensitivity plot of the ECL static divider. The peak operating clock speed of 70 GHz predicted from simulations in the ECL static dividers does not correlate with our measured clock speed of 48 GHz. To explain this discrepancy and improve circuit performance, instability due to gain peaking in emitter follower buffers and unmodeled parasitics in passive IC elements are being investigated.

Divide by 2 operation was seen in the CML static divider up to a peak clock frequency of

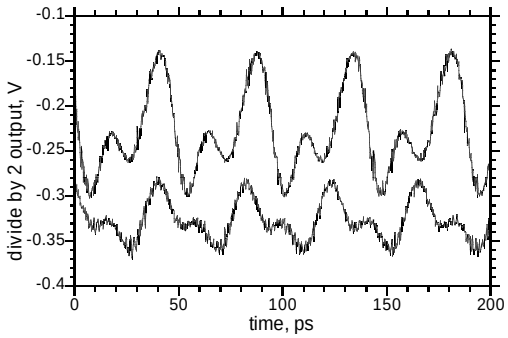

Figure 8: ECl static divider outputs for 48 GHz and 43 GHz clock inputs

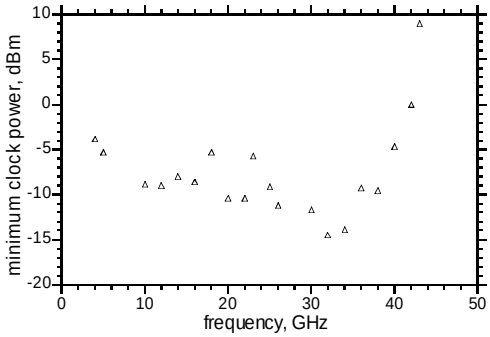

Figure 9: Clock input sensitivity of ECL static divider

47 GHz. This circuit dissipates only 75 mW of power. Fig. 10 shows the output waveform of this circuit. Good correlation is observed between simulated and measured highest frequency of operation in this circuit.

VI Conclusions

We have demonstrated digital integrated circuits in the transferred substrate technology. The technology yields HBTs with peak f_{max} of 470 GHz and f_t of 220 GHz. Static frequency dividers with peak operating frequency of 48 GHz were demonstrated. Optimization of HBT epitaxial layer structure and scaling of emitter and collector dimensions to 0.2 μm should yield devices with lower parasitics over the entire logic swing of the digital gate. These devices combined with more optimized circuit designs should yield digital ICs operating at clock rates >80 GHz.

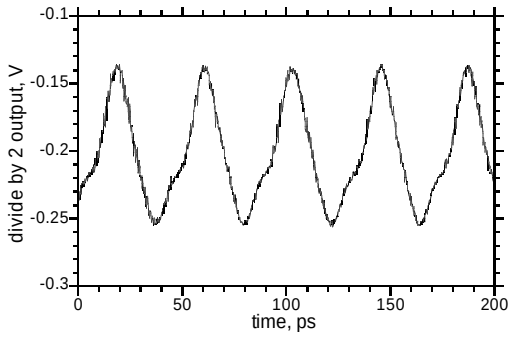

Figure 10: CML static divider output for 47 GHz clock input

References

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