InP Heterojunction Bipolar Transistor Decision Circuits

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Abstract

We have designed and built 30 Gb/s master-slave D-flip-flop circuits using InGaAs/InAlAs HBT's. The HBT devices have a β of 30, and f_{max} and f_t of 160 and 106 GHz, respectively. We discuss methods of testing decision circuits when bit error rate testing is not available at high data rates.

Summary

High speed fiber-optic links are driving the development of fast digital electronics. GaAs HBT's,[1,2,3] MESFET's[4] and HEMT's,[5] and InP HBT's[6,7,8] and HEMT's[9,10] have been used to develop 20-40 Gb/s flip-flops and fiber-optic communications chip sets. At such high data rates, most test and measurement equipment is severely limited. Unless transistor yield permits implementation of high data rate MUX's and DEMUX's on-chip, typical bit error rate test set-ups and pattern generators are limited to a bandwidth of 12 Gb/s. We report now on the development of 30 Gb/s InP HBT decision circuits, and discuss methods of characterization when the limits of available test equipment are exceeded and on-chip MUX's and DEMUX's are not available.

We have developed a process to fabricate high-speed InGaAs/InAlAs HBT's on an InP substrate. The process uses a double-mesa device design. A micrograph of a pair of single emitter HBT's (before airbridge contacts were made) is shown in Figure 1. The two devices share a common collector. The emitter area is 10 μm^2. The circuits use single-emitter devices as well as dual-emitter devices, which have two 1 x 10 μm^2 emitter stripes separated by a 2 μm gap.

A typical DC current-voltage characteristic for the dual-emitter transistors is shown in Figure 2. The transistors can operate at a collector current density in excess of 3 x 10^5 Amps/cm^2. Values for β are between 25 and 30. The flip-flop circuits discussed below have been designed conservatively, with an operating current density of 8 x 10^4 Amps/cm^2, where the breakdown voltage is nearly 2 Volts.

Small-signal *S*-parameter measurements have been performed on the transistors up to 50 GHz. Plots of Mason's unilateral gain (U) and the short circuit current gain (h_{21}) for one of the dual emitter transistors at a current density of 8 x 10^4 Amps/cm^2, are shown in

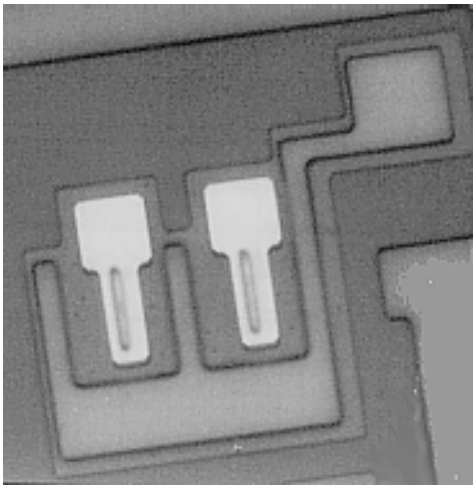

Figure 1. Micrograph showing a pair of InGaAs HBT's sharing a common collector. The single emitters are 1 x 10 μm^2 stripes.

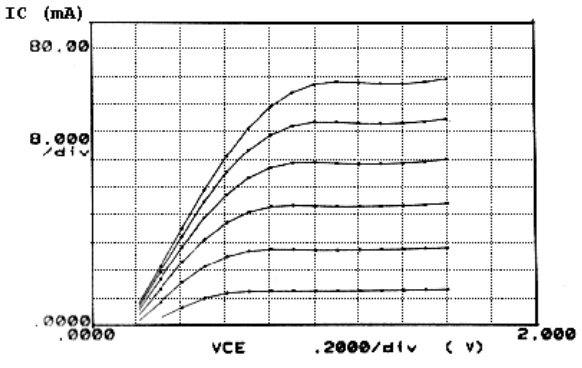

Figure 2. DC I-V characteristics of a dual-emitter HBT, having an emitter area of 20 μm^2. Base current, I_b, was applied in steps of 400 μA.

Figure 3. An extrapolated power gain cutoff frequency, f_{max}, of 160 GHz and current gain cutoff frequency, f_t, of 106 GHz have been obtained. At a current density of 2 x 10^5 Amps/cm^2, the f_{max} increases to 172 GHz while f_t increases to 118 GHz. The single-emitter devices have an f_{max} of 141 GHz and an f_t of 98 GHz at $J_c = 8\text{x}10^4$ Amps/cm.^{2}

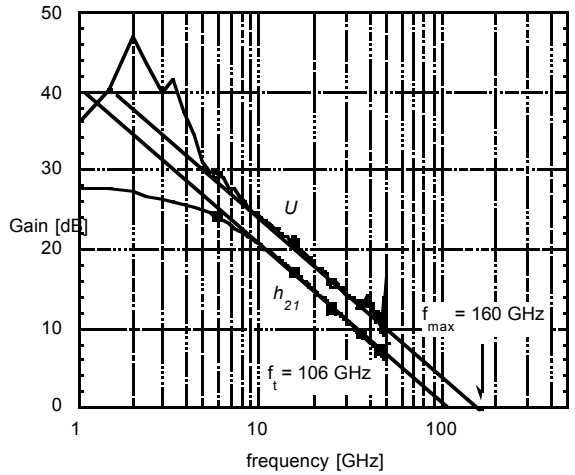

Figure 3. Plot of Mason's unilateral gain, *U*, and short circuit current gain, h_{21}, vs. frequency, showing the extrapolated f_{max} and f_t, for a dual emitter HBT at a current density of 8 x 10^4 Amps/cm^2.

2. Design and Testing of Flip-flops

Using the high-speed transistors discussed in the above section, we have designed and fabricated master-slave flip-flops using emitter-coupled logic. The circuit diagram for the flip-flops is shown in Figure 4. Clock and Data were driven single-ended, with Clockbar and Databar terminated in 50 ohm loads located on the probes. The circuits were designed for an output swing between 0 and -300 mV. The supply voltage was -5 V. The transistors were biased using nichrome resistors. A chip photograph is shown in Figure 5.

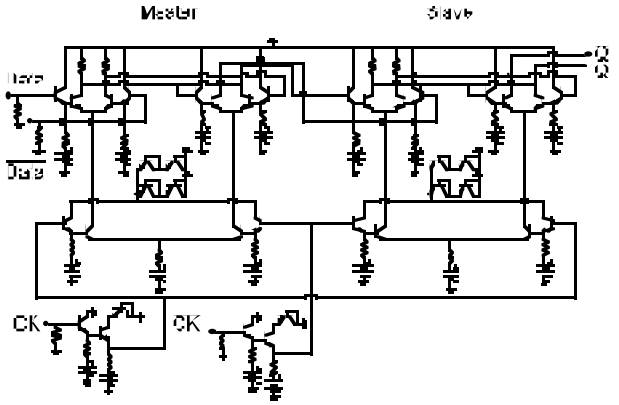

Figure 4. Schematic diagram of master-slave D-flip-flop circuit, showing all on-chip circuitry.

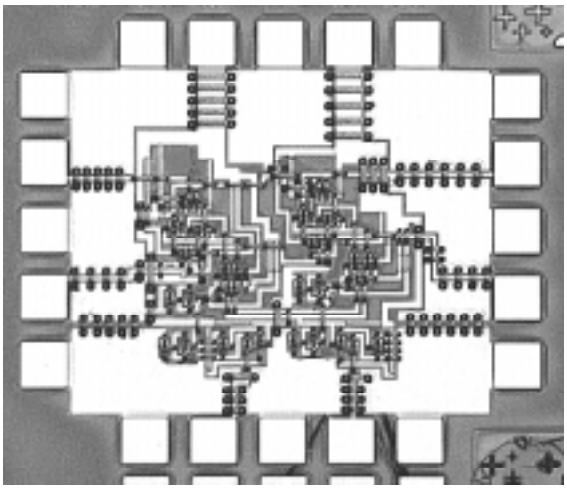

Figure 5. Micrograph of the fabricated master-slave flip-flop circuit is shown, having an approximate area of 1 mm^2 per circuit.

We have measured 30 Gb/s operation for the flip-flop. Figure 6 shows the measured flip-flop outputs, *Q* and *Qbar*, as a function of time, for a clock frequency f_{CK} of 30 GHz and a (sinusoidal) data input of frequency $f_{CK}/2$ =15 GHz, with 600 mVp-p clock and data voltage levels.

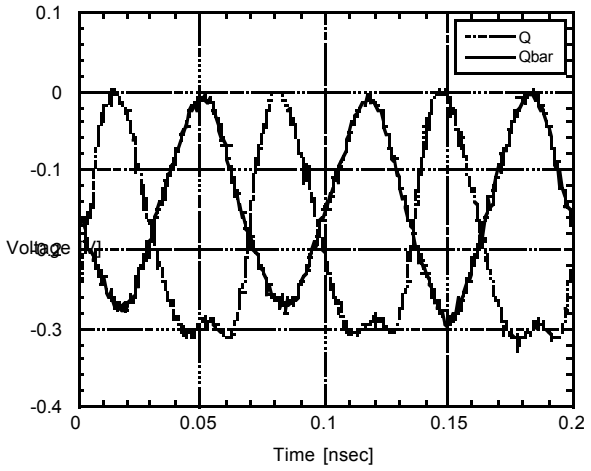

Figure 6. The graph shows a plot of the two flip-flop outputs, *Q* and *Qbar*, for a 30 GHz clock input frequency and a 30 Gb/sec input data rate, for an input data voltage of 600 mVp-p.

In Figure 6, we adjusted the phase between the clock and data with a mechanical phase shifter, in order to a.) allow for sufficient *setup* time for the data to be stable before the clock edge arrives; and b.) measure the phase margin. To measure the phase margin, the phase shifter was calibrated at a specific frequency, and then the range of phase angles over which the flip-flop functions correctly was determined. The phase margin is shown in Figure 7 for a variety of clock frequencies

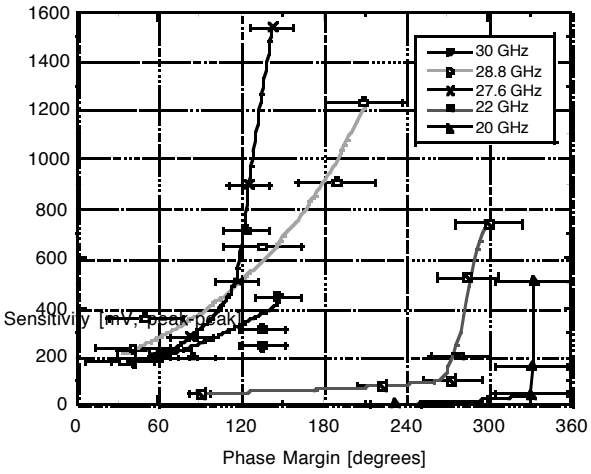

Figure 7. Above graph shows measured data input voltage vs. measured phase margin for the frequency range of 20-30 GHz.

between 20 and 30 GHz. For this plot, the clock input voltage was 635 ± 75 mVp-p for all the frequencies studied.

Because the mechanical phase shifter is imprecise and introduces spurious amplitude variations, we have also verified flip-flop operation and phase margins using *electronic phase-shifting*. In electronic phase shifting, the clock frequency is f_{CK} , and the data is set to a sine wave (analogous to a 101010 ... pattern) at frequency f_{CK} /2 + Δf, with Δf is small. As illustrated in Figure 8, by this means the relative phases (timing) of the clock and data transitions are continuously varied from 0 to 360° over the time period $1/(2\Delta f)$. When the data transition occurs within one setup time prior to the clock edge or one hold time subsequent to the clock edge, the decision circuit will fail to change states. The phase margin (ϕ_m)

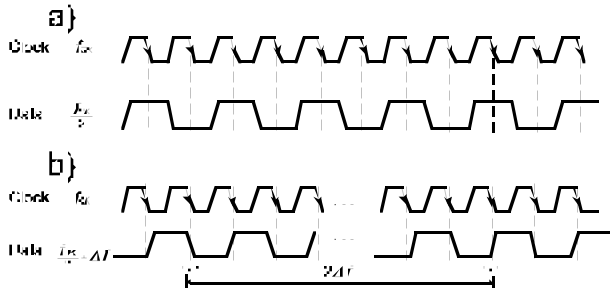

Figure 8. a) Timing diagram illustrating clock and data timing for divide-by-2 operation; b) Electronic phase-shifting timing diagram, where data rate is $f_{CK}/2 + \Delta f$, showing how the additional periodicity of the outputs will be $2\Delta f$.

at f_{CK} is then determined by measuring the period $\Delta\tau$ over which the output does not make correct transitions, and is given by $\phi_m = 360°(1-(2\Delta f)(\Delta\tau))$. The sum of the setup and hold times is given by $\tau_{setup} + \tau_{hold} = (1/f_{CK})(2\Delta f)(\Delta\tau)$.

As an example, the top portion of Figure 9 shows the circuit simulation for f_{CK} = 22 GHz, and a data frequency of f_{CK} /2 + Δf = 12 GHz, with Δf = 1 GHz. The simulated *Q* and *Qbar* are periodic at 11 GHz, with a modulation frequency

of $2\Delta f$, in this case, 2 GHz. From the simulation, it is apparent that the circuit fails to detect *at least* two bits of data, but no more than four, limiting $\Delta\tau$ between 90 and 180 ps. To confirm the simulation, the bottom part of Figure 9 shows experimental data from *Q* and *Qbar*, again for a 22 GHz clock and 12 GHz data, with 90 ps < $\Delta\tau$ < 190 ps. We have used these electronic phase shifting tests to confirm the phase margin data measured with the mechanical phase shifter. For the data in Figure 9, the average value for $\phi_m \approx 260° \pm 40°$, in good agreement with the data of Figure 7 for this input voltage.

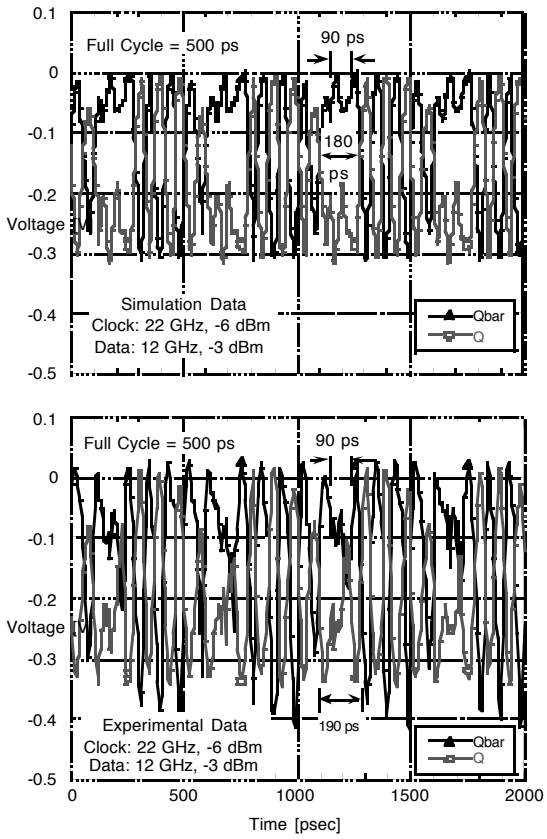

Figure 9. Top graph shows simulated flip-flop outputs; bottom graph shows measured flip-flop outputs, for a 22 GHz clock frequency.

We observe that electronic phase shifting measurements indicate flip-flop setup and hold times of approximately $\tau_{setup} + \tau_{hold} \approx 12 \pm 4$ ps, in the case of the data from Figure 9. In contrast, the observed (and simulated) rise times for *Q* and *Qbar* are ~ 50 ps, this being the factor which limits the circuit's maximum clock frequency.

Figure 10 shows a plot of input sensitivity vs. frequency for the flip-flop. The circuits respond to a wide range of input clock and data voltages. At a clock frequency of 30 GHz, the sensitivity of the data voltage levels for clock voltages between 250 and 700 mV is shown in the inset. For large data voltages, $V_{CE,sat}$ is reached in the input emitter followers, causing the circuit speed to decrease.

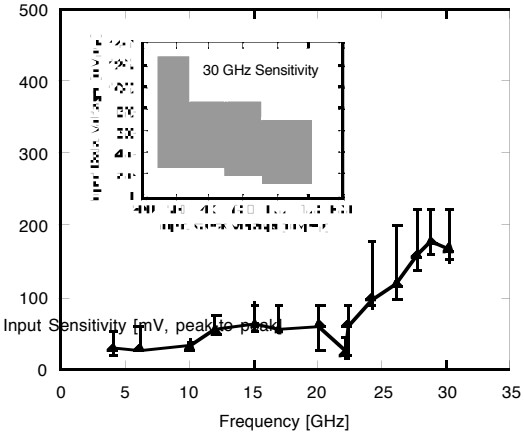

Figure 10. Input sensitivity vs. frequency for the MS flip-flop. Inset shows range input data voltages vs. clock voltage at 30 GHz clock frequency.

Because we do not have a 30 Gb/s bit error rate test system, we have measured the decision ambiguity width for this circuit using a fixed 101010. . .pattern (a sine wave), with a superimposed DC offset. For a 30 Gb/s clock rate and a 630 mVp-p data input, the decision circuit produces correct output levels for DC offsets between + 99 mV and -237 mV; the asymmetry may be a result of driving the flip-flop single-ended. From this, we determine a decision ambiguity width of (630 mV - 99 mV - 237 mV) = 294 mV.

3. Conclusions

In conclusion, we have developed an InP-based HBT process which was used to design and fabricate master-slave D flip-

flops. A method for characterizing decision circuits when 30 Gb/s bit error rate testing is not available was discussed. The phase margin was measured using both mechanical and electronic phase shifting, and revealed a maximum phase margin of 159° for a 30 GHz clock. Using both mechanical and electronic phase shifting measurements, we arrived at a measure of the sum of the flip-flop's setup and hold times, of $\tau_{setup} + \tau_{hold} \approx 12 \pm 4$ ps. These short setup and hold times are not the limiting factor which determines circuit speed, however. Instead, the maximum clock frequency is limited by long (~50 ps) rise times for the outputs *Q* and *Qbar*.

4. Acknowledgments

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