A 50 GHz Broadband Differential Amplifier with Transferred-Substrate HBTs

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Fiber-optic receivers require considerable amplification between the transimpedance preamplifier stage output and the decision circuit input [1,2]. The gain and group delay must be substantially flat over a bandwidth extending from a few KHz up to ~ 70 % of the data rate. AGC or *symmetric* limiting characteristics are also required. To meet these requirements, broadband multistage differential amplifiers are generally employed. This paper presents a broadband differential amplifier in the AlInAs/GaInAs transferred-substrate HBT IC technology. The transferred-substrate HBT IC technology has demonstrated devices with >400 GHz bandwidth (f_{max}) [3], and resistive feedback amplifiers with 50 GHz bandwidth [4]. Here, we present a two stage, DC-coupled differential amplifier. The low frequency gain is 11 dB and the 3-dB bandwidth is greater than 50 GHz. This is the highest bandwidth reported for a broadband differential amplifier.

The device technology used here is similar to our earlier work [3]. The MBE layer structure is similar but with a thinner base layer ($400\mathring{A}$). This improves f_τ at the cost of reduced f_{max}. Fig. 1 shows a schematic cross-section of the IC fabrication process. Resistors are made with thin-film NiCr and have $50\Omega/\square$ sheet resistivity. MIM capacitors with 2000 $\mathring{A}$ SiN as the insulator material are used. The transferred-substrate HBT IC process incorporates a low-capacitance ($\epsilon = 2.7$) microstrip wiring environment with a ground plane and three wiring planes. Efficient heat-sinking is provided through electroplated Au thermal vias. Devices with 0.75 μm wide emitters and 1.8 μm wide collectors were fabricated on this wafer. The common-emitter DC characteristics of the devices are similar to those reported in [3]. Fig. 2 shows the RF characteristics of the devices. The extrapolated f_{max} and f_τ are 370 GHz and 160 GHz respectively.

Fig. 3 shows a schematic circuit diagram of the amplifier. The first stage has a emitter-coupled pair with input emitter follower buffers and 50 Ω output impedance. The second stage employs transimpedance loading to obtain a $\sim$ 50 Ω interface impedance. Level-shifting diodes are used as shown. Active biasing with transistor current mirrors and a single negative supply is used. The IC consumes 250 mW DC power. Fig. 4 shows a photomicrograph of the amplifier. The chip dimensions are 0.75 mm $\times$ 0.44 mm.

The amplifier performance was measured with a network analyzer to 50 GHz. Only single-ended characteristics (two-port) were measured, with the other ports terminated in 50 Ω. Fig. 5 shows the forward gain s_{21} of the amplifier. The low-frequency gain is 11 dB and the 3-dB bandwidth is >50 GHz. The gain ripple at high frequencies is a result of using a 2-port calibration with off-chip terminations of the two unused ports. The in-band gain-flatness (particularly when under AGC) must be improved for application in fiber-optic receivers. Fig. 6 shows the input and output return losses and the reverse isolation of the amplifier.

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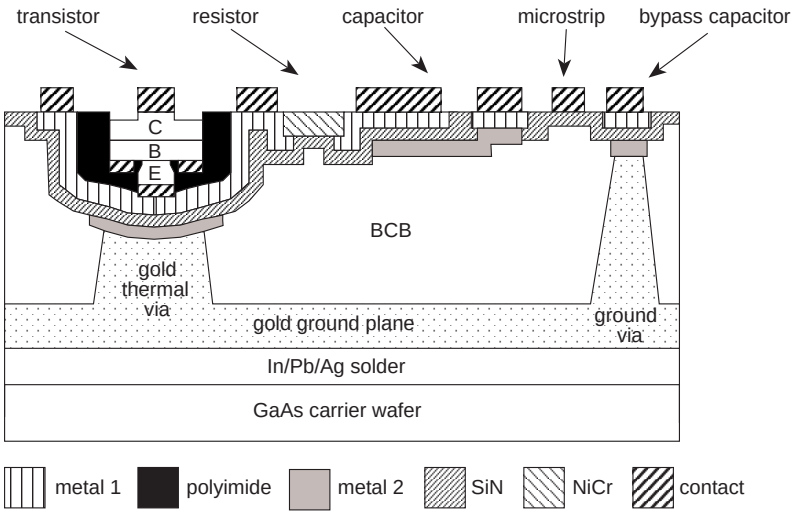

Fig. 1. Schematic cross-section of IC process

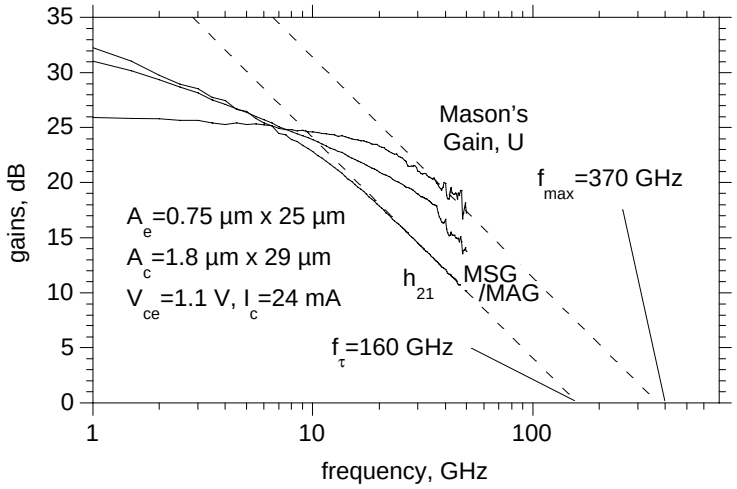

Fig. 2. RF characteristics of device

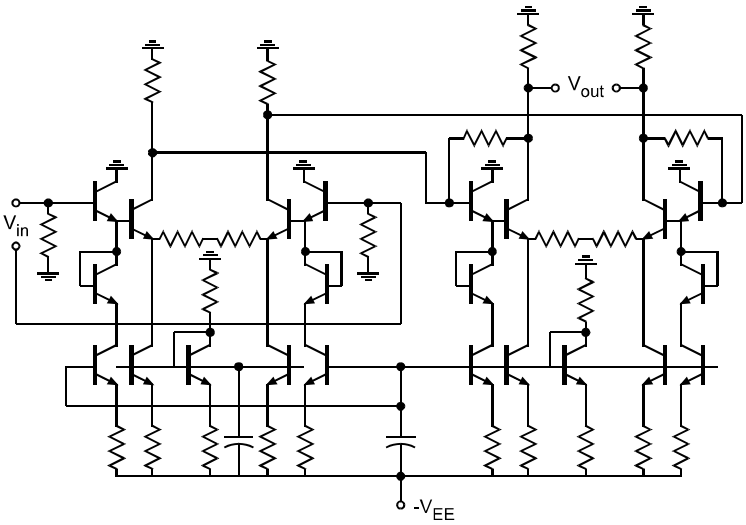

Fig. 3. Schematic circuit diagram of amplifier

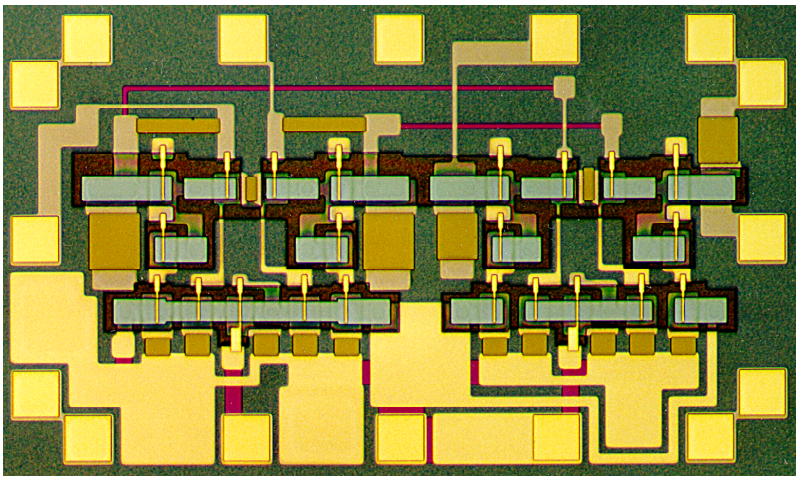

Fig. 4. Photomicrograph of amplifier IC

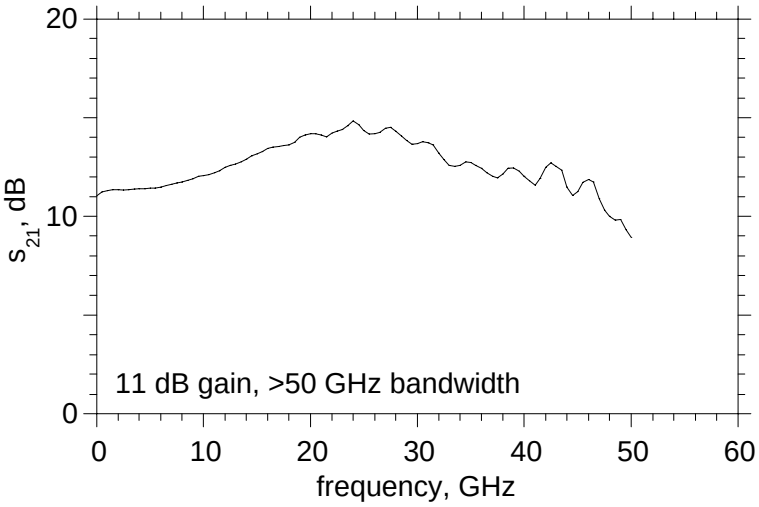

Fig. 5. Forward gain s_{21} of amplifier

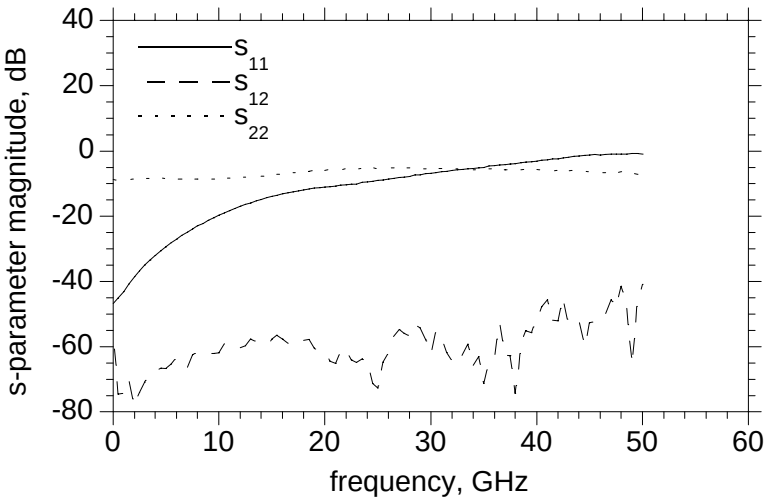

Fig. 6. Return losses and reverse isolation of amplifer