Baseband Amplifiers in Transferred-Substrate HBT Technology

D. Mensa, Q. Lee, J. Guthrie, S. Jaganathan, and M. J. W. Rodwell

Abstract— **Baseband amplifiers have been fabricated in the transferred-substrate HBT process. A Darlington amplifier achieved a DC gain of 15.6 dB with > 50 GHz bandwidth. A mirror doubler amplifier achieved a DC gain of 6.8 dB with 85 GHz bandwidth. These amplifiers will be useful for future work in ADCs, DACs, and fiber-optic receivers, and serve to benchmark the transferred-substrate technology.**

I. Introduction

WIDE bandwidth, DC coupled amplifiers are basic building blocks for larger analog systems[1], [2], [3]. Design and evaluation of simple (single-stage and single-ended) broadband amplifiers is a first step towards development of the more complex amplifiers. Amplifiers such as are reported here will be converted to differential form and AGC added to produce a gain stage for a fiber receiver[4]. Differential versions of these amplifiers with capacitive feedback will be used as Gm-C active filters and as the integrators in delta-sigma ADCs[5]. These resistive feedback amplifiers then serve as more accurate and useful figures of merit for system design than device bandwidth.

We have fabricated two resistive feedback amplifiers with single heterojunction InP based HBTs using the transferred-substrate process. These amplifiers demonstrate low power dissipation and record gain-bandwidth. The gain and bandwidth of these lumped amplifiers much reduces the need for travelling wave structures and their attendant difficulties.

II. Transferred-Substrate HBT Process

A brief review of the transferred-substrate HBT process follows[6], [7]. This process allows definition of HBTs with narrow emitter and collector stripes. Collector-base capacitance (C_{cb}) scales with the area of the collector contact instead of the area of the base mesa. The HBT then has an f_{max} which increases as the emitter-base and collector-base junction areas are reduced. This lithographic scaling of the device can be accompanied by thinning of the epitaxial layers to reduce transit time. The current process provides three levels of metallization plus a microstrip ground plane, MIM capacitors, NiCr resistors, and thermal vias for heat sinking. The amplifiers in this work are not the results of highly scaled devices, but utilize conservative 1 μm emitter stripe and 2 μm collector stripe geometries.

The layer structure of table 1 is grown by MBE. The HBTs reported here utilized a Schottky contact to the collector, eliminating the need for a subcollector layer. The base and emitter layers are grown under high As_2 flux and low growth temperature (380°) to minimize beryllium out-diffusion from the 5 × 10^{19} doped base. The base layer includes approximately 50 mV of compositional grading to reduce base transit time[8]. After MBE growth of the layer structure, processing begins with definition of the emitter contact. The self-aligned base contact etch follows, then deposition of the base contact metal. Isolation mesas are then etched. Polyimide is spun on the wafer to a thickness of 1.8 μm, then etched back to expose the emitter finger. Figure 1 shows a schematic of the process at this point.

Layer	Material	Doping (cm^{-3})	Thickness (nm)	InGaAlAs %Ga/%Al
Cap	n InGaAs	1×10^{19}	100	47/0
	n InGaAs	1×10^{19}	6.6	47/0→0/48
	n InAlAs	1×10^{19}	83.4	0/48
Emitter	n InAlAs	8×10^{17}	50	0/48
	n InGaAlAs	8×10^{17}	23.3	0/48→
	p InGaAlAs	2×10^{18}	6.6	→55/0
Base	p InGaAs	5×10^{19}	50	55/0→47/0
Collector	n InGaAs	1×10^{16}	25	47/0
	n InGaAs	5×10^{17}	5	47/0
	n InGaAs	1×10^{16}	170	47/0
Buffer	i InAlAs	UID	250	0/48

TABLE I
MBE Layer Structure

NiCr resistors are deposited for an intended sheet resistance of 50 Ω/square. After resistor deposition the first layer of metal (M1) is deposited, which contacts the exposed emitter finger and bridges over the polyimide to form either the ground pad (for devices) or an interconnect. A layer of SiN is deposited that forms capacitor dielectric and prevents grounding of device emitters. The second layer of interconnect (M2) is deposited over the SiN.

The microstrip dielectric is then spun onto the wafer. Benzocyclobutene (BCB) is used because of its low microwave loss and low dielectric constant (ϵ_r=2.7). For this work, the thickness of BCB used was 10 μm. Vias are dry-etched in the BCB down to M2. These vias are for heat sinking and/or electrical grounding. Where necessary, de-

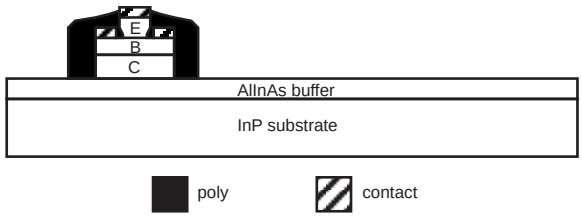

Fig. 1. Schematic after isolation etch

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vice emitters are grounded with a SiN etch before M2 deposition. Gold plating is then performed to fill the vias and form a ground plane (see figure 2).

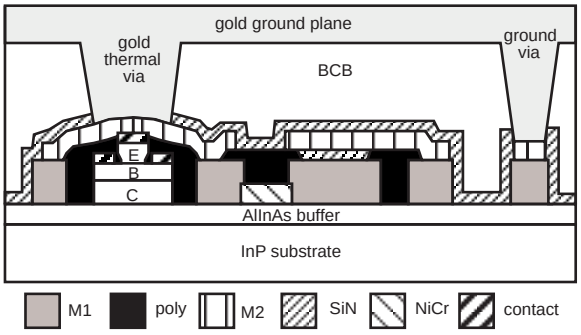

Fig. 2. Schematic after gold plating ground plane

The wafer is then solder bonded to a GaAs wafer of similar size and shape to provide mechanical support. An HCl etch removes the InP substrate completely, stopping on the InGaAs collector. Collector metal (M3) deposition follows, then a self-aligned recess etch of the collector semiconductor completes the process (see figure 3).

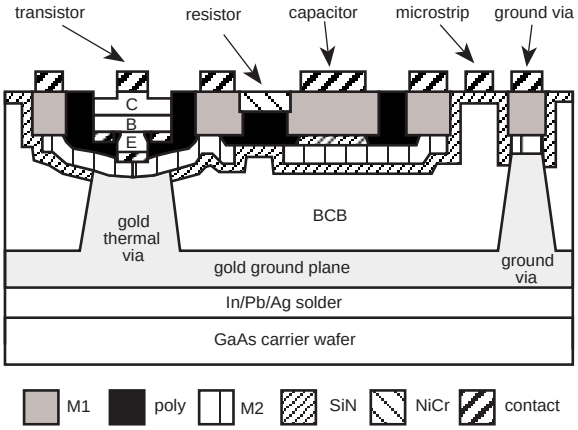

Fig. 3. Schematic after deposition of collector metal (M3)

III. Amplifier Design

A circuit diagram for the Darlington feedback amplifier is shown in figure 4. A chip photo is shown in figure 5. Provision is made for independent biasing of the collector of Q1, requiring a third pad. The area of the chip is then pad limited at 0.52 mm X 0.43 mm, or 0.224 mm^2. Simulated values of DC gain and 3 dB bandwidth are 15.2 dB and 52

Device	Emitter dimension	Collector dimension	Bias Current
Q1	$1 \times 8\ \mu m^2$	$2 \times 12\ \mu m^2$	5.8 mA
Q2	$1 \times 16\ \mu m^2$	$2 \times 20\ \mu m^2$	11.6 mA

TABLE II
Device specifications for Darlington amplifier.

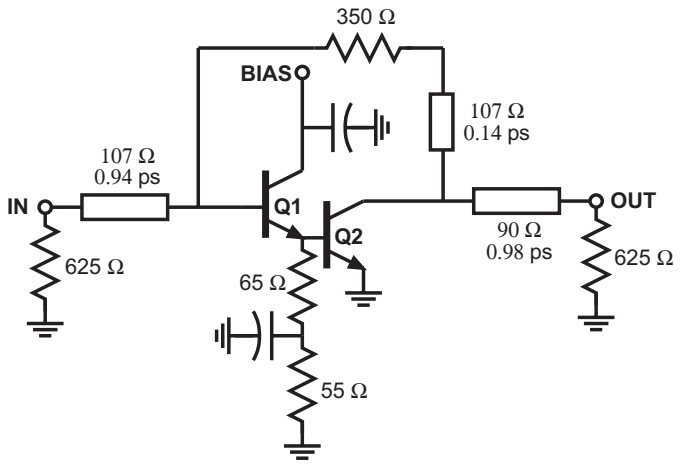

Fig. 4. Circuit diagram of Darlington Amplifier. Line section characteristic impedance and electrical length as indicated.

GHz, respectively. The radial stub bypass capacitors have a (simulated) capacitance of 300 fF. Tuning inductors and shunt resistors to ground are used on input and output to reduce reflection loss and increase bandwidth. No thermal via is provided on the degeneration resistors of Q1, as the parasitic capacitance from the via degrades the amplifier bandwidth. As the IC process is still under development, design rules do not yet exist pertaining to the current carrying capacity of resistors with and without heat sinks. The feedback path consists of a 350 Ω resistor in series with a small inductance. A thermal via is provided on each device, which on the input device represents a small but not negligible parasitic capacitance from the emitter to ground. This capacitance arises from the overlap of the M1 to the grounded M2 through the SiN dielectric.

Figures 6 and 7 show a circuit diagram and chip photo of the mirror doubler amplifier. This amplifier uses an emitter follower to drive a mirror doubler[9]. A third pad is also

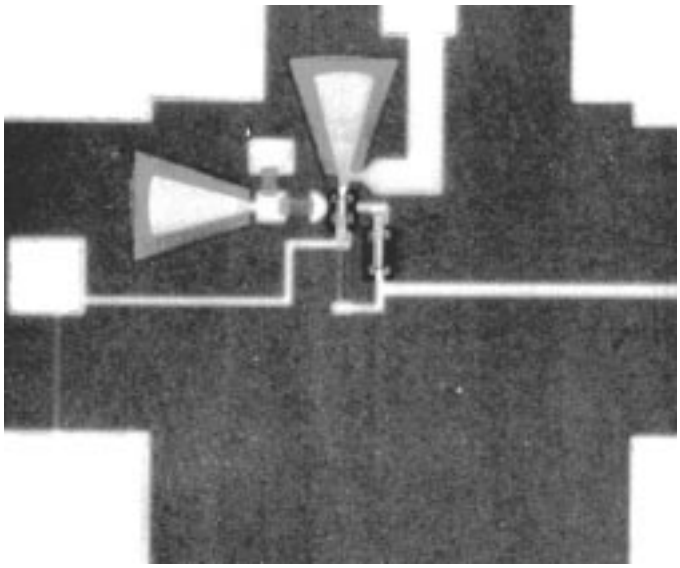

Fig. 5. Chip photo of Darlington Amplifier

Device	Emitter dimension	Collector dimension	Bias Current
Q1	$1 \times 16\ \mu m^2$	$2 \times 20\ \mu m^2$	11.6 mA
Q2	$1 \times 8\ \mu m^2$	$2 \times 12\ \mu m^2$	5.8 mA
Q3	$1 \times 8\ \mu m^2$	$2 \times 12\ \mu m^2$	5.8 mA
Q4	$1 \times 25\ \mu m^2$	$2 \times 29\ \mu m^2$	5.8 mA
Q5	$1 \times 8\ \mu m^2$	$2 \times 12\ \mu m^2$	5.8 mA

TABLE III
DEVICE SPECIFICATIONS FOR MIRROR DOUBLER AMPLIFIER.

used in this design to provide independent collector bias of the emitter follower, resulting in the same chip area of 0.224 mm^2. DC gain and 3 dB bandwidth simulate at 7.5 dB and 94 GHz. The radial stub bypass capacitor is designed to have 150 fF capacitance. Tuning inductors are also used in this design, as well as a shunt resistor to ground on the output. The diode Q4 is for DC level shifting, to maintain the Vce of Q5 near the region of peak RF performance. The feedback path consists of a 150 Ω resistor in series with a small inductance. Thermal vias are provided on each device except for the diode Q4. The diode Q4 is three times larger than Q2, Q3, and Q5 to minimize parasitic resistance at this node. The diode is biased at a low 2.3×10^4 A/cm^2 current density, reducing the need for a thermal via. A thermal via would present an imposing parasitic capacitance to ground for such a large device, and so it has been eliminated.

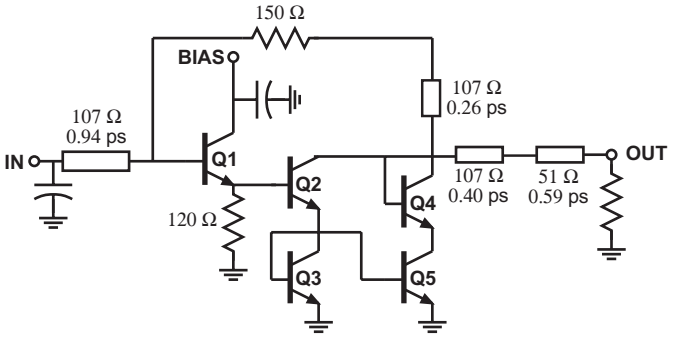

Fig. 6. Circuit diagram of Mirror Doubler

Power dissipation in the emitter degeneration resistor of Q1 is a difficulty. There is no thermal via on this resistor. This resistor demands the highest current carrying capacity of any resistor on the two amplifiers at 0.5 mA/μm under designed biasing conditions. The resistor fails if Q1 is biased at greater than about 15 mA emitter current. Depending upon their length, resistors without vias will fail at current densities in the range of 0.2 to 0.5 mA per micron of width. In the present design, addition of a thermal via to the resistor would prevent thermal failure, but the via capacitance would significantly degrade circuit bandwidth. Without the via, a resistor chosen for a safe current density would be at least 60 microns wide and 144 microns long, dominating the IC area.

In second generation designs now in fabrication, this resistor is replaced with a current mirror bias source, avoiding difficulties with dissipation. As the emitter degeneration resistance in the amplifiers reported here provides shunt stabilization of the emitter follower, in the redesigned amplifiers the current mirror bias source is bypassed at high frequencies by a series RC network.

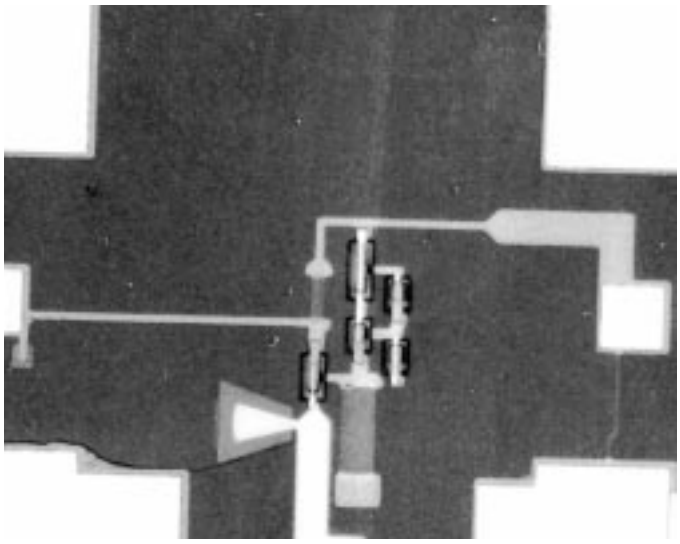

Fig. 7. Chip photo of Mirror Doubler Amplifier

IV. RESULTS

The amplifiers were measured on wafer from 0.5-50 GHz and from 75-110 GHz. S-parameters vs. frequency are plotted in figures 8 and 9 for the darlington amplifier and the mirror doubler amplifier, respectively. The DC gain of the Darlington amplifier is close to simulation at 15.6 dB, with a 3 dB bandwidth that is greater than 50 GHz. The gain peaks at 16.0 dB, and falls to 14.9 dB at 50 GHz. At 75 GHz, the gain has fallen to 8.8 dB, preventing precise determination of the 3 dB bandwidth. S_{22} remains below -13 dB from DC-50 GHz, but S_{11} rises to -4.5 dB at 50 GHz. Amplifier designs were based upon device models

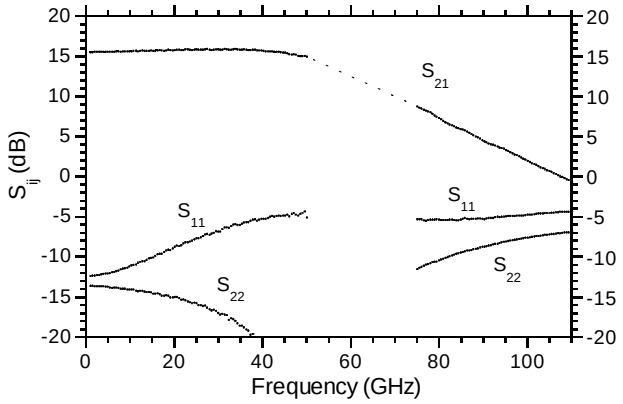

Fig. 8. Measured S parameters of the Darlington Amplifier

from previously-processed wafers. The device characteristics and layout design rules have evolved since that time. In this case, the input tuning network is not appropriate for the input impedance of the realized device. The power dissipation is 36.3 mW.

The DC gain of the mirror doubler amplifier is 6.8 dB. The gain steadily rises with frequency until at least 50 GHz where it reaches 9.5 dB. The frequency at which the gain has dropped to 3 dB below the DC gain is 85 GHz. S_{11} rises to -3.5 dB at W band, and S_{22} rises to -6 dB. This is again due to improper device modeling during circuit design. The power dissipation is 24.2 mW.

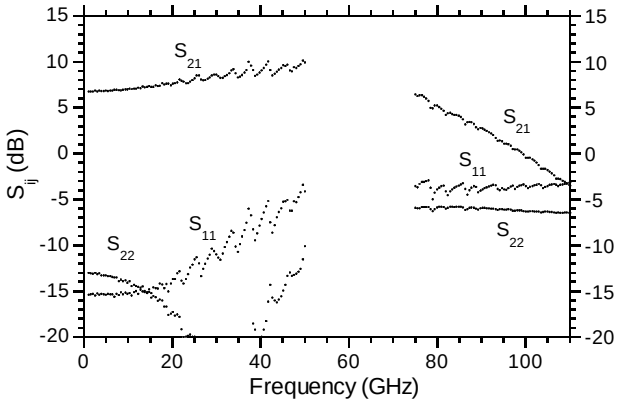

Fig. 9. Measured S parameters of the Mirror Doubler Amplifier

V. Conclusions

Baseband amplifiers have been fabricated in the InAlAs/InGaAs transferred-substrate technology. The mirror doubler amplifier exhibits very wide bandwidth of 85 GHz, while the Darlington amplifier demonstrates record gain-bandwidth product well over 300 GHz and flat gain-frequency characteristics. The amplifiers serve to benchmark this technology. Future work in this area will include improved versions of these amplifiers with higher gain-bandwidth (as the device itself is improved) and integration of amplifiers of this kind (the Darlington) with a photodetector as a fiber-optic receiver front end. These amplifiers will also be converted to differential form and used as building blocks for variable gain amplifiers (VGA).

Acknowledgments

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