80 GHz Distributed Amplifiers with Transferred-Substrate Heterojunction Bipolar Transistors

B. Agarwal, Q. Lee, D. Mensa, R. Pullela, J. Guthrie and M. J. W. Rodwell

Abstract— We report distributed amplifiers with 80 GHz bandwidth, 6.7 dB mid-band gain. These amplifiers were fabricated in the transferred-substrate heterojunction bipolar transistor integrated circuit technology. Transferred-substrate HBTs have very high f_{max} (>400 GHz) and have yielded distributed amplifiers with record gain-bandwidth product.

Keywords—HBT, distributed, InP, broadband, capacitive-division, transferred-substrate.

I. INTRODUCTION

TRAVELING -wave amplifiers (TWAs) are very broad-band circuits with applications in instrumentation and wide-band radar receivers. Broad bandwidth is achieved by absorbing the transistor parasitics into synthetic input and output 50 Ω transmission lines. Flat gain is achieved up to the Bragg frequency of the distributed line, and limited by the available gain from the device. Hence, the amplifier gain-bandwidth product depends critically on the transistor f_{max}. To date, TWAs based on HEMTs have demonstrated considerably higher bandwidths than those based on HBTs [1], [2], [3], [4], primarily due to the higher f_{max} of HEMTs. Transferred-substrate HBTs have high f_{max} [5], comparable to that of high-performance In-GaAs/InAlAs/InP HEMTs, and have demonstrated feed-back amplifiers with very high bandwidths [6]. Hence, TWAs with very high bandwidths should be possible in the transferred-substrate HBT IC technology. Here, we report first results with TWAs fabricated in this technology.

TWA design with HEMTs has been covered in detail in [1]. HBT TWA design differs considerably from that using HEMTs. The HBT transconductance - hence input capacitance ($C_{be} \simeq g_m/2\pi f_\tau$) - per unit HBT emitter area is large. To obtain the desired Bragg frequency, either very small HBTs must be used, or input capacitive-division [7] must be employed. The higher HBT input resistance compared to that of HEMTs (r_{bb} *vs.* r_{gate}) favors the use of very high capacitive-division ratios.

In addition to the input line losses due to the transistor input impedance, TWA gain-bandwidth also depends on the output impedance of the transistor. The frequency-dependent output impedance of HBTs introduces large output line losses. This is a second feature of HBT TWAs that differs substantially from HEMT TWAs. The output impedance of a HEMT is - to first order - R_{ds}. For a HBT driven by a resistive generator impedance, the frequency-

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Fig. 1. MBE epitaxial layer structure of transferred-substrate HBTs.

dependent output impedance arises from feedback through C_{cb}. Cascode connected transistors greatly increase the cell output impedance, decreasing collector line losses to the point where input line losses dominate.

TWA bandwidth is strongly influenced by the frequency-dependent transmission line losses, which become dominant at high frequencies. The transferred-substrate HBT IC process incorporates low-loss microstrip lines on a Benzocyclobutene (BCB, $\epsilon = 2.7$) substrate. These low-loss transmission lines make high bandwidths feasible. The process also incorporates thermal vias for transistor heat-sinking and ground vias for low ground-return inductance. With these design and technological improvements, we have fabricated TWAs with 6.7 dB gain and 80 GHz 0-dB bandwidth (where the gain goes below the mid-band gain). The 3-dB bandwidth is 85 GHz. This is the highest gain-bandwidth product reported for a HBT distributed amplifier.

The transferred-substrate HBT IC technology is described first. HBT TWA design is briefly discussed, followed by measurements and conclusions.

II. TRANSFERRED-SUBSTRATE HBT TECHNOLOGY

This section describes the transferred-substrate HBT technology in detail. The fabrication process is discussed first, followed by device DC and RF characteristics.

A. Fabrication

Fig. 1 shows the MBE epitaxial layer structure used in this work. The growth is done on a Fe-doped semi-insulating (100) InP substrate, starting with a 2500 Å AlInAs buffer layer. The GaInAs collector is 2700 Å thick, is Si-doped at $1 \times 10^{16}/\text{cm}^3$ and contains a $5 \times 10^{11}/\text{cm}^2$ Si pulse-doped layer 400 Å from the base. The 400 Å GaInAs base is graded in both doping and bandgap. The 100 Å of the $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ base immediately adjacent to the collector is Be-doped at $3 \times 10^{19}/\text{cm}^3$. The remaining 300 Å of the base is Be-doped at $5 \times 10^{19}/\text{cm}^3$. By increasing the Ga cell temperature progressively during growth of the 300 Å layer, the Ga:In ratio is gradually increased, introducing a ~ 0.03 eV bandgap gradient across the 300 Å layer. The base is then graded in 300 Å to the AlInAs emitter. The first 66 Å of the grade is Be-doped at $2 \times 10^{18}/\text{cm}^3$ and the remainder is Si-doped at $8 \times 10^{17}/\text{cm}^3$. The AlInAs emitter is about 1350 Å thick. The first 500 Å are Si-doped at $8 \times 10^{17}/\text{cm}^3$ and the remainder is Si-doped at $1 \times 10^{19}/\text{cm}^3$. This is graded in 66 Å to the InGaAs emitter cap. The emitter cap is n^+ doped with Si at $1 \times 10^{19}/\text{cm}^3$.

Fig. 2 shows a schematic cross-section of the transferred-substrate HBT integrated circuit process. The fabrication process starts with the evaporation of Ti/Pt/Au emitter contacts. A combination of a dry etch, a selective wet etch, and a non-selective wet etch is then used to etch down to the base epitaxial layer. Self-aligned Ti/Pt/Au base metal is evaporated and sintered. Transistors are then isolated by forming mesas, stopping on the AlInAs buffer layer. Thin-film NiCr is evaporated on the wafer to form resistors with 50 $\Omega/\square$ sheet resistivity. The devices are passivated and the emitters are planarized with polyimide. Polyimide also serves as interconnect crossovers for multiple wiring levels. The first level of metallization (M1), is evaporated at this point. This metal forms most of the transmission lines, interconnect wiring, probe pads, capacitor bottom plate and resistor contacts. Emitters and bases are also contacted by this metal. SiN dielectric is then deposited over the entire wafer by PECVD. This dielectric serves three purposes
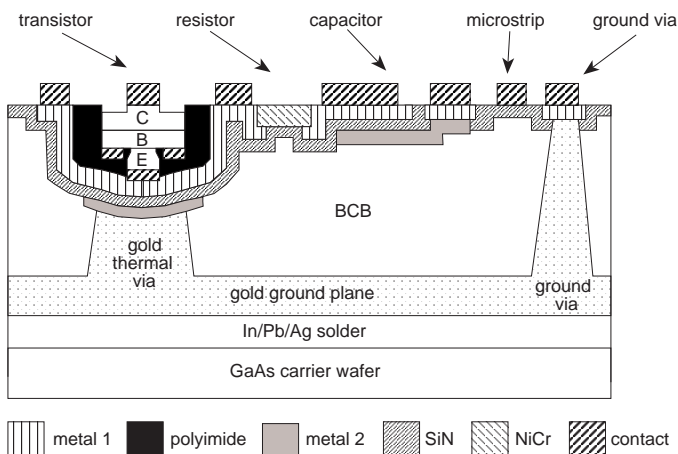
: it forms the dielectric for metal-insulator-metal capacitors; it forms the insulator for crossovers between M1 and the second level of metallization; and, it forms a insulating layer over the whole wafer prior to the process of substrate transfer. The SiN is selectively etched away followed by the second level of metallization (M2), similar to M1. M2 also forms the top plate for MIM capacitors.

The substrate transfer process starts by coating the wafer with a thick layer of Benzocyclobutene (BCB, $\epsilon_r = 2.7$) and curing. Thermal vias on the emitters and ground vias are formed by dry etching openings in the BCB. This etch also etches the SiN insulator layer in the vias. The vias are then filled with thick Au by electroplating. The electroplated Au also forms an electrically and thermally conducting ground plane, thus grounding all emitters. Transistors with non-grounded emitters (required in ICs) are fabricated by protecting the SiN insulator with M2 before applying BCB (fig. 2). Power supply bypass capacitors could be formed similarly. On transistors not having the layer of M2, the SiN insulator is removed during the via formation etch, thus grounding the emitter.

Microstrip interconnect lines on BCB provide a low-capacitance wiring environment for dense circuits. Ground vias to the thick electroplated ground plane provide low ground return inductance. Thermal vias provide efficient heat-sinking for devices operating at very high current densities.

The wafer is then inverted and bonded to a GaAs transfer substrate. The InP substrate and the AlInAs buffer layer are removed by a wet etch thus exposing all the buried elements of the wafer. Ti/Pt/Au Schottky collector contacts are then deposited. This metal layer could be used as a third level of metallization (M3), if needed, with polyimide as the insulator. Outside the active collector area, about 1500 Å of the collector drift region are then removed by a self-aligned wet etch to reduce collector-base fringing capacitance.

This completes the transferred-substrate HBT IC process. For integrated circuit applications, high device yield is required. The transferred-substrate HBT IC technology is constantly being improved towards this goal. The technology is currently capable of yielding circuits with few tens of transistors.

B. Device Characteristics

Common-emitter DC characteristics of the devices are shown in fig. 3. The devices have 0.75 μm $\times$ 25 μm emitters and 1.8 μm $\times$ 29 μm collectors. The small signal current gain at DC, β, is 50. The common-emitter breakdown voltage BV_{CEO} is ~ 3 V, decreasing to 1.5 V at 10^5 A/cm^2. The low breakdown voltage is due to the narrow-bandgap InGaAs collector material.

DC characteristics of the devices with 0.75 μm $\times$ 25 μm emitters and 1.8 μm $\times$ 29 μm collectors were measured in the common-base configuration also. Fig. 4 shows these characteristics. The common base current gain α is 0.98. The common-base breakdown voltage BV_{CBO} is $\sim$ 6 V, decreasing to 1.5 V at 10^5 A/cm^2.

Fig. 2. Schematic cross-section of transferred-substrate HBT IC process.

Fig. 3. DC common-emitter characteristics of transferred-substrate HBTs.
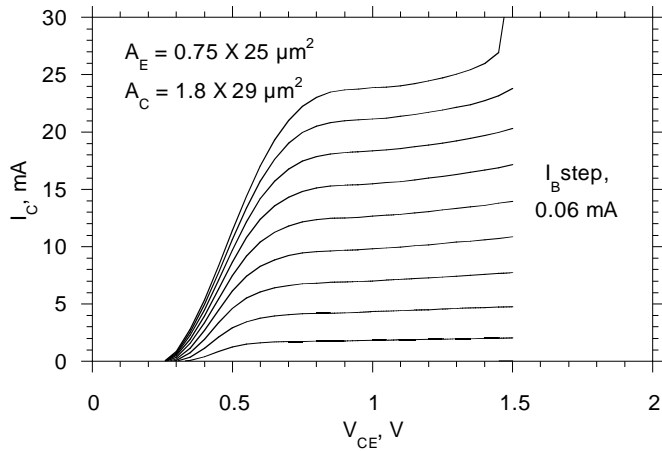

Fig. 5. RF characteristics of transferred-substrate HBTs.

The devices were characterized by on-wafer network analysis to 50 GHz. Fig. 5 shows the maximum available/maximum stable gain MAG/MSG, the short-circuit current gain h_{21}, and Mason's invariant (unilateral) power gain U of the transistor. Pad parasitics have not been stripped. Device dimensions and bias conditions are as shown. Extrapolating at -20 dB/decade, $f_{max} = 370$ GHz and $f_\tau = 160$ GHz.

Fig. 6 shows the variation of f_τ and f_{max} with emitter current density J_E. The peak f_τ is 175 GHz. F_τ increases with current density and saturates at high current densities due to Kirk effect. The Kirk effect threshold is high due to the presence of the pulse-doped layer in the collector, close to the base. Kirk effect influences f_{max} more strongly than f_τ as is seen from the reduced f_{max} at high current densities. This is because when the base width increases, the base transit time increases and the collector transit time reduces thus keeping the sum of the two relatively constant. But, the reduced collector thickness increases C_{cb} and degrades f_{max}. By plotting $1/2\pi f_\tau$ vs. $1/J_E$, it is determined that the sum of the base and collector transit
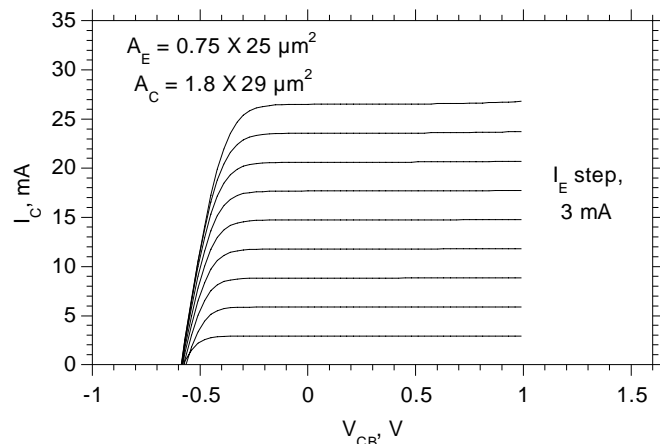
times $(\tau_b + \tau_c)$ is 0.67 ps. Fig. 7 shows the variation of f_τ and f_{max} with collector-emitter voltage, V_{CE}. At low V_{CE}, the collector thickness reduces due to base pushout leading to increased C_{cb} and reduced f_{max}. At high V_{CE}, f_τ and f_{max} decrease, suggesting a decrease in the collector electron velocity at high electric fields.

Small-signal hybrid-π models of transferred-substrate HBTs were developed from bias-dependent s-parameters. This simple model was used to design and simulate the traveling-wave amplifier which is presented in the next section.

III. Circuit Design and Fabrication

The theory of traveling-wave amplifiers has been presented in detail elsewhere in this journal [1]. It was shown that capacitive voltage division can be used on the input line to achieve gain-bandwidth products approaching the transistor f_{max} for any given design bandwidth. To obtain even higher gain-bandwidth products, a cascode transistor cell can be used instead of a single transistor. The theory developed in [1] applies equally well to HBTs. Here, we present only the final result. Using a simplified HBT hybrid-π model with the base resistance r_{bb}, the emitter-
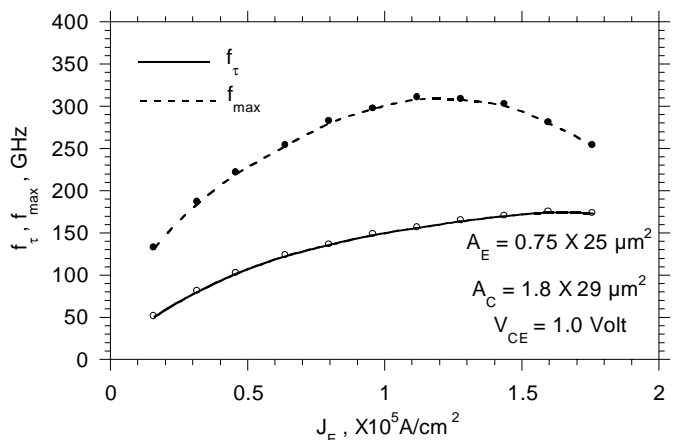

Fig. 4. DC common-base characteristics of transferred-substrate HBTs.

Fig. 6. Variation of f_τ and f_{max} with emitter current density J_E.

Fig. 7. Variation of f_τ and f_{max} with collector-emitter voltage V_{CE}.

Fig. 8. Schematic circuit diagram of the capacitive-division traveling-wave amplifier.
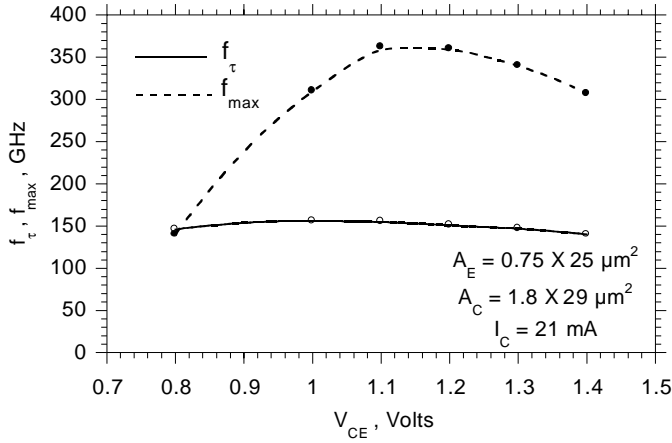
base capacitance C_{be}, transconductance g_m and the division capacitor C_{div}, we obtain for a cascode capacitive-division TWA,

$$A_v = -NMg_m Zo/2 \qquad (1)$$

where A_v is the voltage gain, N is the number of TWA cells, M is the capacitive-division ratio ($= C_{div}/(C_{div}+C_{be})$) and Z_o is the characteristic impdeance. The number of sections is limited by the input line losses (since output line losses are negligible). The input voltage to the Nth stage is attenuated by $e^{-(N-1/2)\alpha_b}$, where α_b is the base line attenuation per section. The maximum number of transistors N_{max} for a given desired bandwidth ω_{BW} is given by

$$N_{max}\omega_{BW}^2 M^2 C_{be}^2 r_{bb} Z_o \simeq 1 \qquad (2)$$

Using Eqs. 1 and 2, the gain-bandwidth product is given by

$$A_v \omega_{BW}^2 = g_m/MC_{be}^2 r_{bb} \qquad (3)$$

If aggressive capacitive-division (smaller M) is used, the number of sections used can be higher and gain-bandwidth improves, but is limited by the maximum available gain of the cascode cell. In the above derivation, the transmission line skin-effect and radiation losses have been neglected. These losses do impact the highest attainable gain-bandwidth in a given technology. If these losses are made negligible, the available power gain from the device can be achieved.

Fig. 8 shows the schematic circuit diagram of the capacitive-division TWA. Cascode-connected HBTs Q1-Q2 are used as explained before. The base and collector lines are composed of 75 Ω microstrip line sections. C_{div} is the division capacitor at the input of the common-emitter transistor Q1. A short length of microstrip is used at the output of the cascode cell to improve velocity matching between the input and output lines. The microstrip lines, together with the division capacitor and the cascode stage synthesize 50 Ω input and output lines. R_{bterm} is the 50 Ω base-line termination resistor. R_{cterm}, the collector-line termination resistor is off-chip to sustain the high collector bias current, and is connected through a microwave probe. R_{b1} is
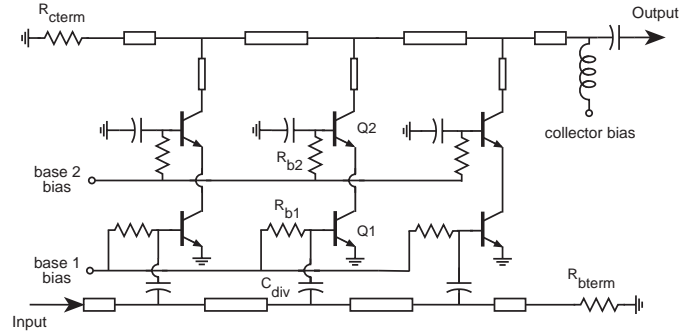
a large resistor to bias the input of Q1. The base of the common-base transistor Q2 is biased through an independent supply. AC ground at this node is provided by large bypass capacitors. R_{b2} provides decoupling between the multiple cells and prevents oscillations from resonance between the bias probe inductance and the bypass capacitors. The collector bias is through a bias tee at the output of the chip. Amplifiers with 3 cascode cells were fabricated. The simulated gain is about 7 dB and the designed bandwidth is 90 GHz. Fig. 9 shows a photomicrograph of the fabricated chip. The die size is about 1.4 mm $\times$ 0.6 mm.

IV. RESULTS

The amplifiers were tested on-wafer using commercial network analyzers from 0.045-50 GHz and 75-110 GHz. Fig. 10 shows the forward gain of the amplifier. The mid-band gain is about 6.7 dB. The 0-dB bandwidth (where the gain goes below the mid-band gain) is 80 GHz. The 3-dB bandwidth is 85 GHz.

From this curve, we can also observe gain peaking at high frequencies. The gain-frequency response of TWAs is strongly impacted by device f_{max} and the designed Bragg frequency. During design, a conservative HBT model with a 200 GHz f_{max} was assumed. HBTs on the current wafer have 370 GHz f_{max} which results in the observed gain peaking. Given the 370 GHz f_{max}, redesigning the amplifier would permit bandwidths greater than 80-90 GHz. The low frequency cut-off is about 2 GHz and is determined by the transistor f_τ/β. Fig. 11 shows the input and output return losses and the reverse isolation. The amplifier output return loss s_{22} is poor at high frequencies because of
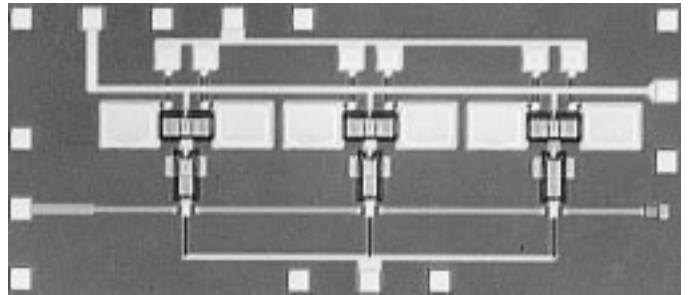

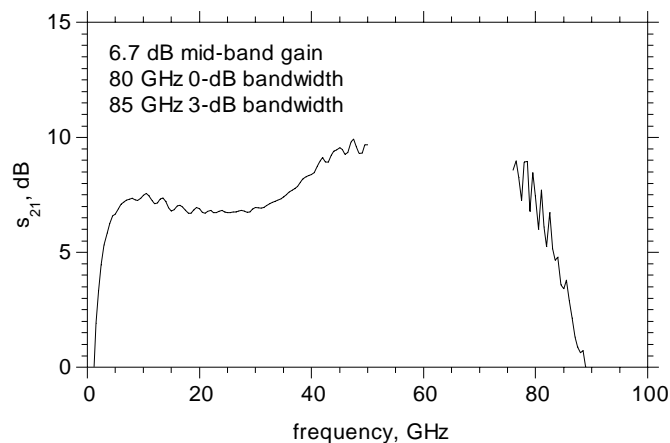Fig. 9. Photomicrograph of the amplifier IC.
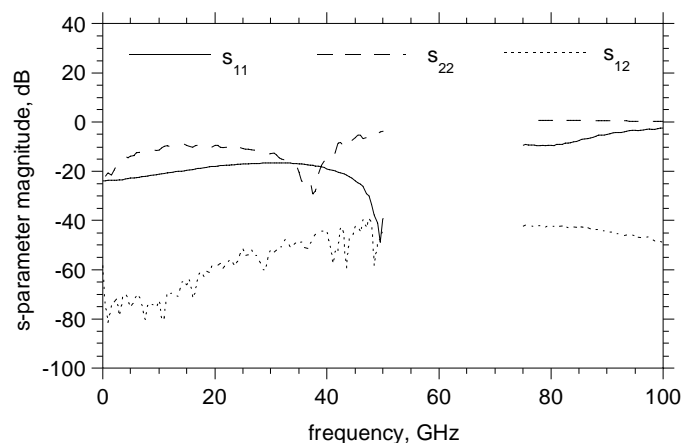
Fig. 10. Measured forward gain s_{21} of the amplifier.

Fig. 11. Measured input return loss s_{11}, output return loss s_{22}, and reverse isolation s_{12} of the amplifier.

the off-chip collector-line termination. The chip consumes about 250 mW of power.

V. Conclusions

We have designed and fabricated distributed amplifiers with 6.7 dB mid-band gain, 80 GHz 0-dB bandwidth and 85 GHz 3-dB bandwidth. These amplifiers have the highest gain-bandwidth product reported for a distributed HBT amplifier. The ICs demonstrate the potential of transferred-substrate HBTs for producing very high speed integrated circuits. Further improvements in the design of the amplifier, as well as in the intrinsic device technology will lead to wider bandwidth circuits.

Acknowledgments

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