66 GHz Static Frequency Divider in Transferred-substrate HBT Technology

Q. Lee, D. Mensa, J. Guthrie, S. Jaganathan, T. Mathew, Y. Betser
S. Krishnan, S. Ceran and M. J. W. Rodwell
Department of Electrical and Computer Engineering
University of California, Santa Barbara, CA 93106
805-893-8044, 805-893-3262 FAX
e-mail : rodwell@ece.ucsb.edu

Abstract

We report a 66 GHz emitter coupled logic (ECL) 2:1 static frequency divider using InAlAs/InGaAs transferred-substrate HBTs. To our knowledge this is the fastest static divider reported in any semiconductor technology.

I Introduction

Applications for HBTs include microwave frequency direct digital synthesis, fiber-optic transmission chip-sets and analog-digital converters. Master-slave flip-flops are critical functional elements in a variety of these digital and microwave systems. Maximum clock frequencies of master-slave flip-flops are readily determined by configuring the circuit as a 2:1 static frequency divider. These circuits are often used as benchmarks to evaluate the speed of a digital technology [1]. In this paper we demonstrate a static frequency divider with 76 transistors fabricated in the transferred-substrate HBT process. The circuit operated at 66 GHz clock rate. The maximum frequency is limited by the test set-up.

II Fabrication

The MBE layer structure used in this work is similar to [2]. The InGaAs base is 400 Å thick, and is Be-doped at $5{\cdot}10^{19}/\mathrm{cm}^3$. 50 meV base bandgap grading, introduced by varying the Ga:In ratio, reduces the base transit time. The collector is 3000 Å thick InGaAs.

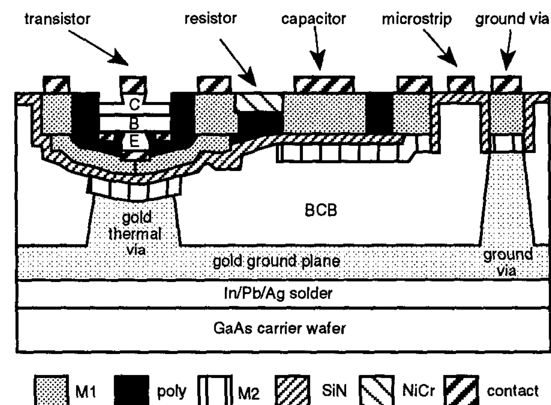

Figure 1: IC schematic cross-section.

ICs were fabricated in the transferred-substrate HBT process. This process provides very wideband transistors together with a low-parasitic microstrip wiring envi-

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ronment on a low-ϵ (2.7) substrate. Details of the process are described in [2]. Emitter contact metal is defined by optical projection lithography at 0.5 and 0.7 μm linewidths, followed by the standard base-emitter junction process, base mesa isolation, polyimide passivation and planarization, NiCr resistors deposition, interconnect metal 1 evaporation, SiN deposition for MIM capacitors and emitter insulation, and interconnect metal 2 evaporation. The substrate transfer process includes BCB deposition, etching and plating to form thermal vias and ground planes, bonding to a transfer substrate, and InP host substrate removal in HCl. The Schottky collector contacts are then deposited, completing the process. Figure 1 shows a IC schematic cross-section.

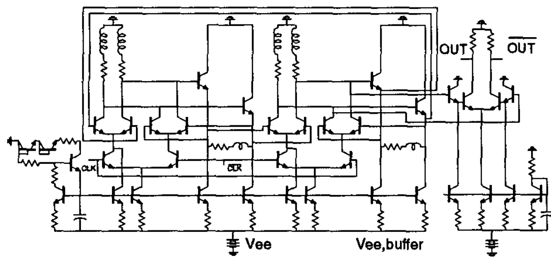

Figure 2: Simplified circuit diagram of ECL 2:1 static frequency divider.

ICs were fabricated using two standard transistor geometries. Wide-stripe devices have 0.7 μm emitter metal, 0.5 μm emitter-base junction width, and 1.5 μm collector widths. Narrow-stripe devices have 0.5 μm emitter metal, 0.3 μm emitter-base junction width, and 0.8-1.0 μm collector widths. On other processed wafers with identical MBE material (400 Å InGaAs base with 50 meV grading, 3000 Å collector thickness), the narrow-stripe devices exhibit f_τ=164 GHz and f_{max}=800 GHz [3].

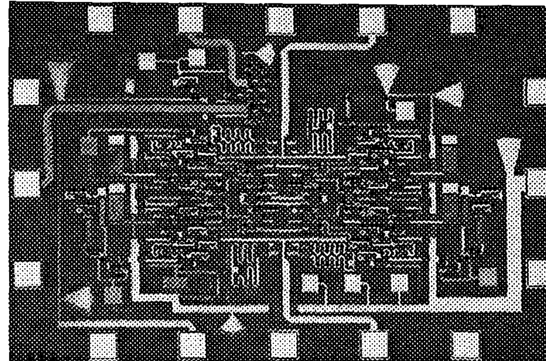

Figure 3: Divider photograph.

III Circuit Design

Figure 2 and 3 show a circuit diagram and chip photograph of the 2:1 static frequency divider. Figure 4 shows the key circuit design feature. The divider consists of an ECL master-slave D-flip-flop with inverting output connected back to the data input and an ECL output buffer stage. Current mirrors provide biasing. A "keep-alive" current (1/6 of the on-state current) is applied to the loading stage of each D-latch. This current keeps the loading switching pair weakly biased during the latching phase, reducing the latch-load transition time, and hence the propagation delay. Interconnect delay is a serious issue. The switching signal path is a short, doubly-terminated 90 Ω transmission-line bus, located at the center of the IC. The IC periphery is devoted to biasing current mirrors. The 90 Ω bus termination resistors use a small amount of series inductive peaking. The inductors are implemented with microstrip transmission lines. A series connected resistor and inductor combination between the emitter nodes of the emitter followers provides damping, thus preventing emitter follower ringing. The Tektronix 40 GHz sampling head provides one of the 50Ω load resistance terminations for the output

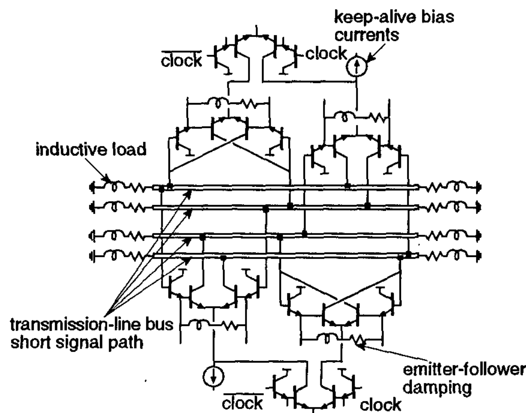

Figure 4: Key features of design and physical layout.

buffer stage. The second output pad is terminated in a 50Ω load through a 67 GHz wafer probe. The circuit is fabricated with 0.7 μm x 12 μm emitter and 1.5 μm x 14μm collector HBTs, operating at a current density of 2.0 mA/μm^2. The overall chip area is 1.0 x 0.4 mm, and contains 76 transistors.

Given the influence of wiring parasitics on high-speed logic operation, circuits were simulated with all significant interconnects modeled as microstrip transmission lines. Simulations (HP-EESOF) predict a maximum 95 GHz clock frequency.

IV Results

The 2:1 divider were tested on-wafer using commercial micro-coaxial probes. One of the two differential clock inputs is terminated in 50 Ω. A 67 GHz micro-coaxial wafer probe connects the second differential clock input pad to a sinusoidal clock signal source through an 18-50 GHz bias tee. The clock input is driven single-ended with a 2-20 GHz synthesizer followed by a 50-75 GHz frequency multiplier. Divide-by-2 operation is observed up to the frequency of 66 GHz using the current test setup. Figure 5 shows the output waveform of this circuit driven at 66 GHz. The flip-flop dissipates 812 mW from a -5V supply, and the output buffer dissipates 38 mW from a -2V supply. Given the peak clock frequency of 95 GHz predicted from SPICE simulation, which takes into account all significant device and interconnect parasitics, we believe the circuit performance is currently limited by the measurement setup. We are currently purchasing both 50-75 GHz and 75-110 GHz test equipment.

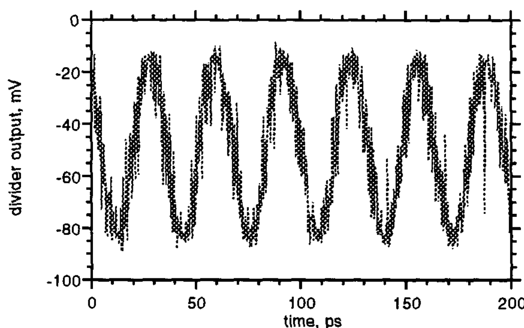

Figure 5: 33 GHz output waveform of ECL divider for 66 GHz clock input.

V Conclusions

In summary, we have designed and fabricated emitter coupled logic 2:1 static frequency dividers in the transferred-substrate HBT technology. 66 GHz divide by 2 operation is demonstrated. To our knowledge, this is the fastest divider reported in any semiconductor technology to date. The circuit performance is currently limited by the test setup. With higher frequency instrumentation, further device scaling and improved circuit design, clocked 100 GHz digital ICs should be feasible.

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