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A 50mm Copper/Polymer Substrate HBT IC Technology for >100GHz MMICs

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Abstract—**We report HBT integrated circuits fabricated by substrate transfer on 50mm diameter copper/polymer substrates. Layout and packaging of complex $\approx$ 100GHz circuits is facilitated by the microstrip wiring environment and the low ground lead inductance it affords. For ICs operating above 100GHz, the process allows radical scaling of the microstrip dielectric thickness without requiring handling of delicate thinned III-V wafers. The process can provide greatly improved heatsinking. Furthermore, full 50mm wafers can be processed incorporating transferred substrate HBTs, devices which have obtained > 500 GHz f_{max}.**

I. Introduction

Future communications and radar systems will require complex ICs operating significantly above 100GHz. In addition to transistors of greatly increased bandwidth, severe difficulties with interconnects, packaging and heatsinking must be addressed.

Ground return inductance, in particular the grounding inductance from die to package is critical to successful deployment. Problems of parasitic ground lead inductance in packaged ICs are greatly alleviated by the adoption of microstrip wiring, with its continuous backside ground plane. Delay sensitive circuits demand interconnects which are both physically short and characterized by high wave velocity (low ϵ_r). Minimizing interconnection delays forces integration densities up. Compounded with the high bias current density required for high speed HBTs, high power densities will arise and effective heatsinking is required.

We present a Copper/polymer substrate HBT IC process. ICs are fabricated on a 50mm diameter substrate. The initial, InP, substrate is replaced in the final ICs by an electroplated Cu surrogate substrate which forms the ground plane for polymer dielectric microstrip transmission lines. The Cu/polymer substrate provides a microstrip wiring environment with $5\mu m$ dielectric thickness for low via inductance. Copper thermal vias and the copper substrate provide effective heatsinking. The process includes transferred substrate HBTs, which have earlier obtained > 500GHz f_{max}[1].

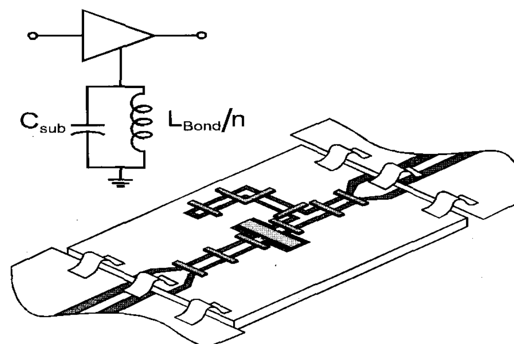

Fig. 1. Limiting package to die ground connections to the periphery of the die introduces parasitic ground return inductance. The inductance of the n ground bond ribbons, L_{bond}/n resonates with the parallel plate substrate capacitor, C_{sub} in the ground return circuit.

II. Substrate Engineering

The thickness of transmission line substrates must be scaled inversely with frequency. Microstrip transmission lines inherently support the TM_0 surface wave mode for all frequencies. However, energy transfer from the microstrip mode does not occur until such frequency as the phase matching condition is reached. This condition is approximately given by the cutoff of the TE_0 surface wave mode, $f_{TE_0} = c/\left(4h\sqrt{\epsilon_r - 1}\right)$[2]. Spurious surface wave modes in CPW are suppressed by the addition of a package ground plane under the substrate. The resulting structure supports a TEM parallel plate mode (between CPW and package grounds) at all frequencies which, *for ICs much smaller than* $\lambda/2$, is suppressed by peripheral grounding. For $f > c/\left(2h\sqrt{\epsilon_r}\right)$, or about 80GHz for a 0.5mm InP wafer, the spurious TE_1 parallel plate substrate mode is also supported by CPW on ground plane. CPW MMIC wafers not thinned according to operating frequency are subject to degradation by substrate mode effects. Although scaling CPW transmission lines to narrower ground plane separations can reduce the loss due to radiation, it cannot eliminate such loss where substrate modes are allowed. Thus, any energy coupled into

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substrate modes from one signal path on a CPW MMIC can potentially couple back to other signal paths. Such coupling can critically affect signal isolation within real systems implemented in CPW.

Shared parasitic ground return inductance is another source of crosstalk between subcircuits; this is the so-called "ground bounce" issue. Such shared ground inductance can be difficult to avoid when laying out circuits with multiple signal paths in CPW, and especially when packaging CPW MMICs[3]. As shown schematically in Fig. (1) inductance in the package grounding ribbon bonds can introduce resonances in the ground return circuit. The issue of ground return loops tends to favor the use of microstrip transmission lines for complex circuit designs. Though microstrip helps to isolate ground return paths, through wafer vias introduce a parasitic inductance which becomes significant at mm wave frequencies. A typical ground via through a $100\mu m$ thick GaAs wafer might represent a 10pH inductor.

HBTs typically reach their peak bandwidth at emitter current densities on the order of $10^5 \mathrm{A/cm^2}$. Given a minimum collector-emitter bias voltage of about 1V, this implies local dissipated power densities on the order of $10^5 \mathrm{W/cm^2}$. In a complex digital or mixed signal IC, the overall die power density could reach $1000\mathrm{W/cm^2}$. This power density would give rise to a temperature rise of $> 67°C$ across a 0.5mm thick wafer of InP with its thermal conductivity of 75W/mK. This figure of $67°C$ is an optimistic lower bound neglecting the concentration of heat sources. To achieve acceptable junction temperature rises in dense integrated circuits, the underlying semiconductor wafers must be thinned.

Recently reported MMIC amplifiers operating at 155GHz[4] and 94GHz[5] required substrate thinning to $75\mu m$ and $50\mu m$ respectively, where heatsinking and ground via inductance are the driving issues. Handling and lapping of such thinned wafers is difficult, and will become more so as frequencies are increased and the wafers thinned accordingly.

III. Fabrication

The InAlAs/InGaAs HBT epitaxial layer structure is as reported in[6]. Initial processing is as reported in[7], [6]. The microstrip transmission line substrate is formed after mesa isolated HBTs, passive elements and interconnections have been formed. Benzocyclobutene (BCB) polymer constitutes the dielectric substrate of the microstrip lines. The BCB resin is applied by spin casting and cured under N_2 ambient. Ground vias are formed by RIE etching of the BCB. The final thickness of the BCB film in the present work was $5\mu m$. As circuit operating frequencies increase, the substrate thickness can easily be scaled further. By virtue of the low permittivity ($\epsilon_r \approx 2.7$) dielectric used, the wiring offers $200\mu m$/psec

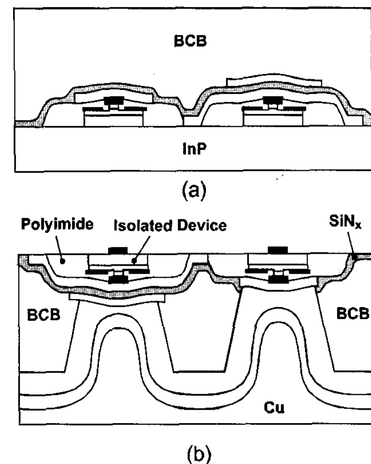

Fig. 2. Schematic cross-sections at two stages of process: a) prior to etching of vias in BCB b)after InP removal, patterning and deposition of collector contacts. The HBT labeled "isolated device" has its emitter electrically isolated from ground by the SiN_x layer.

propagation.

The ground plane and surrogate substrate is formed on the BCB by electroplating. A conductive seed layer is formed by sputtering of Ti and Au. Thin layers of plated Au and Ni are followed by a $30\mu m$ Cu layer, and a final protective Ni layer. While Ni and Au were plated from commercial solutions, the Cu was plated from a solution of H_2SO_4 and $CuSO_4$. The wafer is bonded to a Si carrier wafer with wax, in a mounting operation very similar to those used in typical wafer back-thinning processes[8]. The InP growth substrate is removed by a selective wet etch. Collector stripes and final interconnections are patterned while the MMIC wafer resides on the Si carrier. At this stage, the wafer includes NiCr thin film resistors, Si_3N_4 MIM capacitors, and three levels of interconnect metal. The entire MMIC wafer can then be liberated from the Si wafer in a normal demounting operation, or the MMICs could be diced directly. Schematic cross-sections of the wafer at key steps are shown in figure (1). A photo of a fully processed 50mm diameter wafer is shown in (fig. 3).

IV. Discrete Devices

RF characteristics of discrete devices were measured from 1-50GHz and 75-110GHz with a vector network analyzer. Calibration was by means of on-wafer LRL calibration standards. In the present work, HBTs were produced with relaxed geometries. Transistors with $2\mu m$ collector and $1\mu m$ emitter widths showed 175GHz f_t and 320GHz $f_{\max}$ (Fig. 4). The power gain cutoff frequency, $f_{\max}$, of the transferred substrate HBT has earlier been demonstrated to improve with lithographic scaling [9],

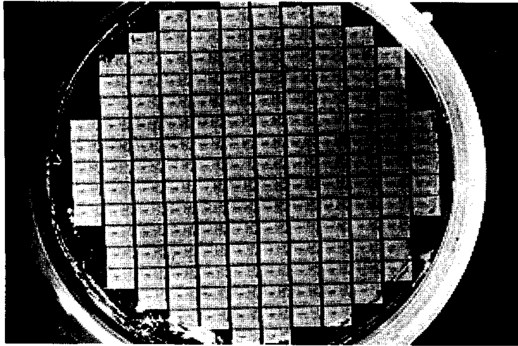

Fig. 3. Photo of completed 50mm wafer

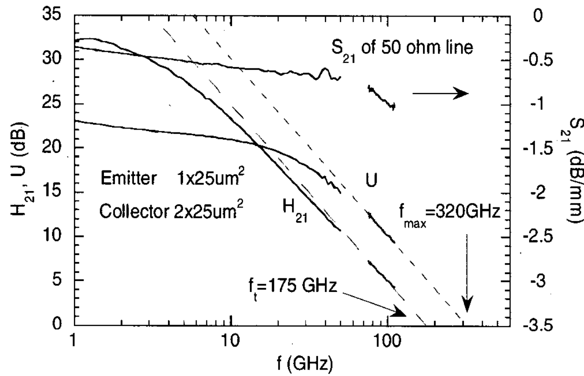

Fig. 4. Measured RF characteristic gains, H_{21}, U of discrete transistor, and normalized S_{21} of transmission line test structure

[1]Microstrip transmission lines of 50Ω nominal characteristic impedance showed less than 1.1dB/mm of loss at 110GHz (fig. 3).

V. Demonstration Circuits

As a demonstration of this technology, a variety of wideband MMICs have been fabricated on the present 50mm wafer. Darlington feedback amplifiers exhibit 9.5dB of gain from 0 to > 50 GHz (fig.4). Current mirror f_t doubler feedback amplifiers with common emitter input stage exhibited 5.3dB of gain from 0 to > 50GHz(fig.5). Reactively matched differential cascode f_t doubler amplifiers, designed to drive a 10Ω antenna were also tested on wafer in the 50Ω system. These amplifiers exhibited 8dB of gain from 75-80GHz with respect to 50Ω terminations(fig.6), and would have resulted in ≈ 10.5dB of gain into the 10Ω load.

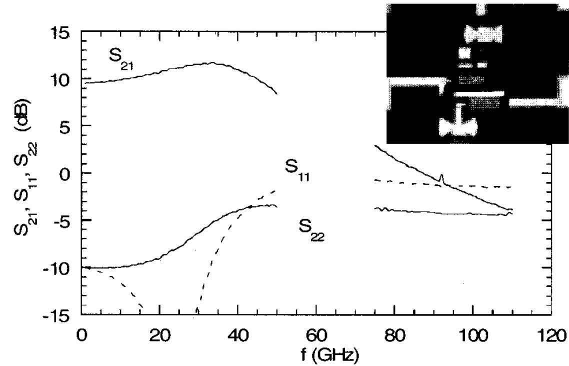

Fig. 5. Measured RF characteristics of Darlington feedback amplifier. Die photo inset.

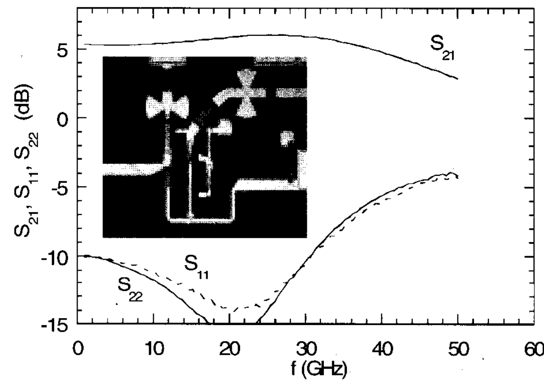

Fig. 6. Measured S parameters of mirror f_t doubler resistive feedback amplifier. Die photo inset.

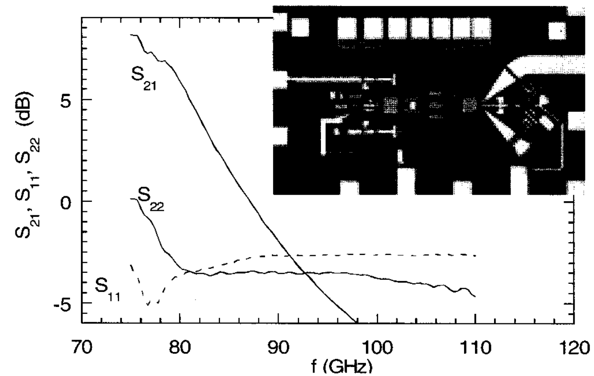

Fig. 7. Measured S parameters, with respect to 50ω characteristic impedance, of differential cascode tuned amplifier.

VI. Conclusion

The Copper/Polymer substrate process is similar to a conventional microstrip process, except that mechanical wafer thinning is replaced by a selective wet chemical etch. The process can provide very high $f_{\max}$ HBTs and a wiring and packaging environment suitable for ICs operating above 100GHz. Full 50mm wafers have been demonstrated.

VII. Acknowledgments

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