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SUBMICRON TRANSFERRED-SUBSTRATE HETEROJUNCTION BIPOLAR TRANSISTORS WITH GREATER THAN 800 GHz f_{max}

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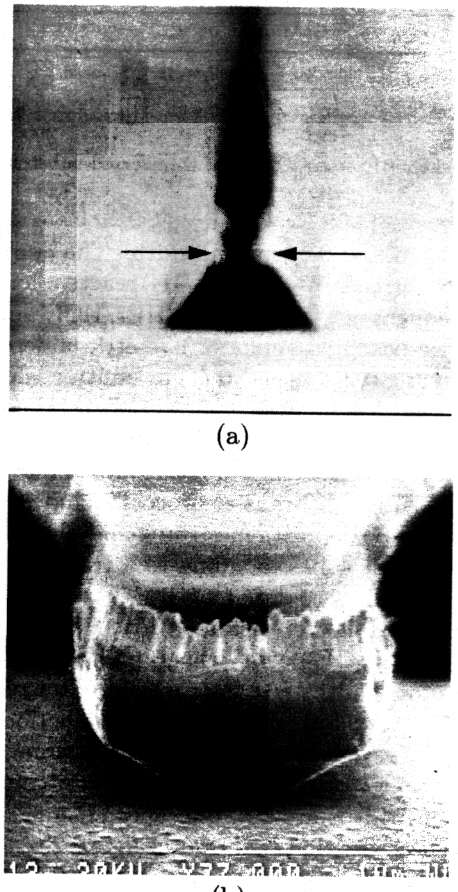
Abstract— **We report submicron transferred-substrate AlInAs/GaInAs heterojunction bipolar transistors. Devices with 0.4 μm emitter and 0.4 μm collector widths have 17.5 dB unilateral gain at 110 GHz. Extrapolating at -20 dB/decade, the power gain cut-off frequency f_{max} is 820 GHz.**

I. INTRODUCTION

VERY wide bandwidth heterojunction bipolar transistors (HBTs) [1], [2] will enable microwave analog-digital converters, microwave direct digital frequency synthesis, fiber-optic transmission at > 40 Gb/s, and wireless data networks at frequencies above 100 GHz.

Such ICs will demand very high transistor current gain cutoff frequency f_τ and power gain cutoff frequency f_{max}. Increases in f_τ are obtained by thinning the collector, and by thinning and grading the base. Unfortunately, thinning the base and collector epitaxial layers increases the base-collector capacitance C_{cb} and the base resistance R_{bb}, decreasing $f_{max} \sim \sqrt{f_\tau/8\pi R_{bb}C_{cbi}}$ where C_{cbi} is the fraction of C_{cb} charged through the base resistance R_{bb}. Using substrate-transfer processes [3], HBTs can be fabricated with narrow emitter/base and collector/base junctions on opposing sides of the base epitaxial layer. Reducing the emitter and collector widths progressively reduces $R_{bb}C_{cb}$, and hence f_{max} increase rapidly with scaling. Subsequently thinning the base and collector epitaxial films will increase f_τ at the expense of f_{max}, and high values of both f_τ and f_{max} are thus obtained.

We had earlier reported transferred-substrate heterojunction bipolar transistors with 0.8 μm collector junction width and > 400 GHz f_{max} [3]. Here we report submicron devices fabricated using electron-beam lithography and (for dimensional control) combined reactive-ion and wet-chemical etches. Devices with 0.4 μm emitter and 0.4 μm collector width obtained DC current gain $\beta = 50$ and 17.5 dB unilateral power gain at 110 GHz. Extrapolating at -20 dB/dec results in an estimated 820 GHz f_{max}, the highest reported for any transistor.


(a)

(b)

Fig. 1. Device electron micrographs. (a) Test structure with 0.15 μm emitter. (b) 0.4 μm Schottky collector stripe.

II. DEVICE DESIGN AND FABRICATION

The MBE epitaxial layer structure used in this work is similar to [3]. The base is 400 Å thick, and is Be-doped at $5{\cdot}10^{19}/\mathrm{cm}^3$. 50 meV base bandgap grading, introduced by varying the Ga:In ratio, reduces the base transit time. The collector is 3000 Å thick.

The fabrication process is similar to that described in [3]. Emitter contact metal is defined by E-beam lithogra-

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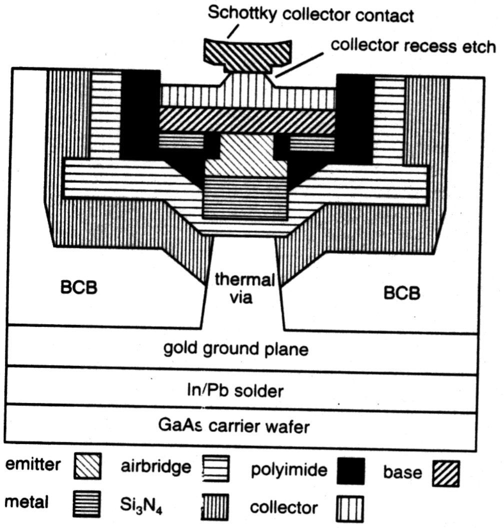

Fig. 2. Schematic cross-section of transferred-substrate HBT.

phy at 0.3 μm and 0.5 μm linewidth. The emitter-base junction is formed by $CH_4/Ar/H_2$ reactive-ion-etching with subsequent selective (acetic/HBr/HCl) and nonselective citric-based wet etches. The etch undercuts 0.05 μm, producing 0.2 μm and 0.4 μm emitter widths (figure 1). Subsequent steps include self-aligned base Ohmic contact deposition, base mesa isolation, polyimide passivation and planarization, and interconnect metal evaporation. The substrate transfer process includes Benzocyclobutene (BCB) deposition, etching and plating to form vias and ground planes, bonding to a transfer substrate with an $In_{0.4}Pb_{0.6}$ solder, and InP host substrate removal in HCl. Collector metal, with a "T" cross-section, is then defined by E-beam lithography at 0.5, 0.7, and 1.1 μm contact widths. An isotropic collector recess etch to 0.05 μm depth forms collector-base junctions with a tapered profile, reducing C_{cb} while maintaining latitude for emitter-collector misalignment. After etching collector junction widths are 0.4, 0.6, and 1.0 μm. A device schematic cross-section is shown in figure 2.

III. Results

Devices with 0.2 x 6 μm^2 emitter and 0.4 x 10 μm^2 collector exhibit DC current gain $\beta = 24$, while devices with 0.2 x 6 μm^2 emitter and 0.6 x 10 μm^2 collector exhibit $\beta = 42$.

The devices were characterized by HP8510 on-wafer network analysis from 0 to 50 GHz and 75-110 GHz using (GGB Inc.) waveguide-coupled microwave wafer probes. To avoid measurement errors (in S_{12}, hence U) arising from microwave probe-probe coupling, the HBTs are separated from the probe pads by 230-μm-length on-wafer microstrip lines. On wafer calibration standards were used to de-embed the transistor S-parameters. The standard Line-reflect-line (LRL) technique was used, with microstrip through line, extended lines for 20-50 GHz and 75-110 GHz calibration, and offset shorts and opens for the reflect standard and for verification. Biasing at $V_{ce} = 1.2$ volts and $I_c = 5.0$ mA, devices with 0.4 μm emitter and 0.4 μm collector widths obtained 3.2 dB current gain and 17.5 dB unilateral power gain at 110 GHz (figure 3). Extrapolating at -20 dB/decade, the current gain cut-off frequency f_τ is 162 GHz and the power gain cut-off frequency f_{max} is a record 820 GHz. We have used unilateral gain U for extrapolating the power gain cut-off frequency f_{max} because of its characteristic -20 dB/decade slope, its independence of the transistor configuration (common-base vs. common-emitter), and its independence of inductive and capacitive pad parasitics. The common-emitter (figure 3) and common-base (not shown) maximum stable gains are 12.2 dB and 16.0 dB at 110 GHz.

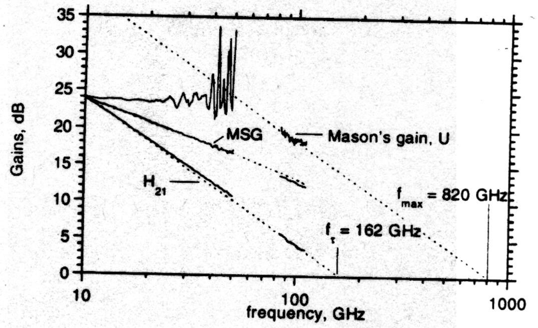

Fig. 3. Common-emitter RF characteristics of device with a 0.4 x 6 μm^2 emitter and a 0.4 x 10 μm^2 collector, biased at V_{ce} = 1.2 V and I_c = 5 mA.

Figure 4 shows a small-signal hybrid-π model for a device with a 0.4 x 6 μm^2 emitter and a 0.4 x 10 μm^2 collector biased at $I_c = 5$ mA and $V_{ce} = 1.2$ V. Base

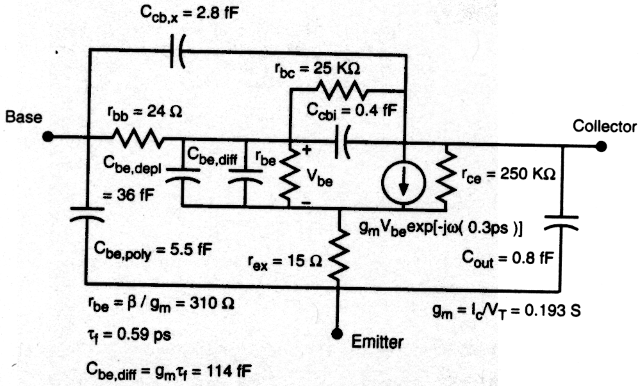

Fig. 4. Device equivalent circuit model at V_{ce} = 1.2 V and I_c = 5 mA.

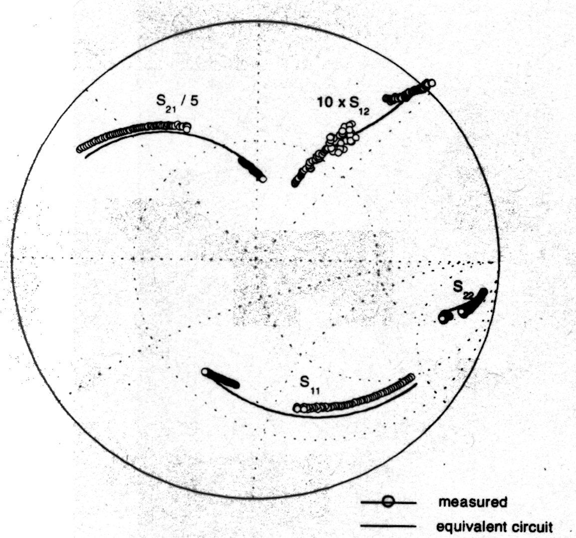

Fig. 5. Measured device S-parameters at $V_{ce} = 1.2$ V and $I_c = 5$ mA. The solid line represents S-parameters of the equivalent circuit model.

resistance R_{bb} consists of spreading resistance, contact resistance and base-emitter gap resistance. The measured base sheet resistance is $600\ \Omega/\square$ and the specific contact resistance is $50\ \Omega$-μm^2. With these parameters, we calculate a $24\ \Omega$ base resistance. $R_{ex} = 15\ \Omega$ is determined by plotting $\mathrm{Re}\{Y_{21}\}$ vs. $1/I_c$. By plotting $1/2\pi f_\tau$ versus $1/J_e$, it is determined that the sum of the base and collector transit times ($\tau_b + \tau_c$) is 0.59 ps, and the sum of the collector-base and base-emitter depletion capacitances ($C_{cb} + C_{be,depl}$) is 39 fF. R_{cb} and the total C_{cb} are extracted by plotting the real and imaginary part of the admittance parameter Y_{12} versus frequency. R_{cb} represents variation of collector-base leakage with bias, likely due to impact ionization. Base-width modulation in HBTs is negligible, hence R_{ce} is large. $C_{be,poly}$ is a calculated metal-polyimide-metal overlap capacitance between the emitter and base metalizations. The 3.2 fF sum of C_{cbi} and C_{cbx} is of the magnitude expected from the combination of ($\epsilon A_c/T_c$) 1.5 fF collector junction capacitance and ($\sim$ 10 μm x 150 fF/mm) metal-metal fringing capacitance between the base ohmic metal and the transmission line contacting the collector. Inclusive of the differential space-charge effect [4], [5], observed earlier in MESFETs [6], $C_{cbi} = \epsilon A_E/T_c - I_c \partial\tau_c/\partial V_{ce}$, where T_c is collector thickness and $\partial\tau_c/\partial V_{ce}$ is the variation in collector transit time with bias. The measured f_τ vs. V_{ce} (figure 6) indicates $\partial\tau_c/\partial V_{ce} \cong 0.05$ - 0.15 ps/Volt, predicting $C_{cbi} \cong 0.13$ fF - 0.63 fF at $I_c = 5$ mA. $C_{cbi} = 0.4$ fF is determined by fitting to the measured unilateral gain. This is 2.2:1 smaller than the expected zero-current capacitance ($\epsilon A_E/T_c = 0.88$ fF). The measured S-parameters (figure 5), h_{21} and U show good correlation to that of the hybrid-π model. Figure 6 and 7 show the variation of f_τ and f_{max} with bias. The drop of f_{max} at high current density and at low V_{ce} is due to the Kirk effect.

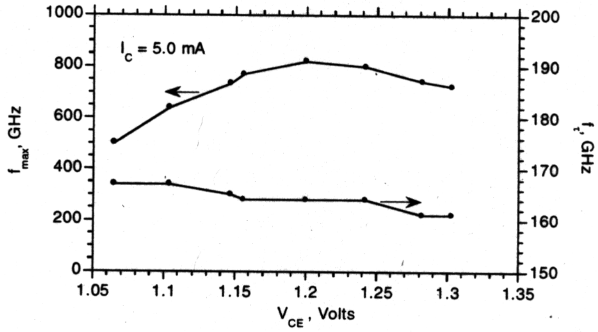

Fig. 6. Variation of f_τ and f_{max} with collector-emitter voltage V_{ce}.

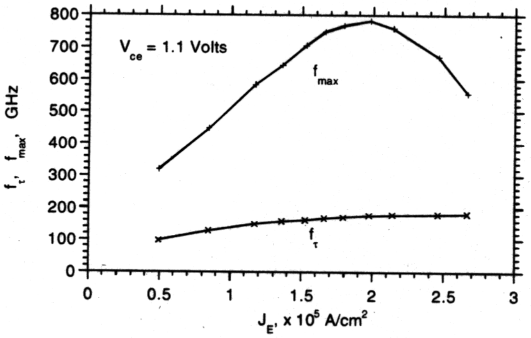

Fig. 7. Variation of f_τ and f_{max} with emitter current density J_e.

IV. CONCLUSIONS

We have demonstrated submicron transferred-substrate heterojunction bipolar transistors. Devices with 0.4 x 6 μm^2 emitters and 0.4 x 10 μm^2 collectors obtained an extapolated f_τ of 162 GHz and f_{max} of 820 GHz. With further scaling, HBTs with > 1000 GHz f_{max} should be feasible, pemitting ICs operating above 300 GHz [7].

ACKNOWLEDGMENTS

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