48-GHz Digital IC's and 85-GHz Baseband Amplifiers Using Transferred-Substrate HBT's

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***Abstract*— Using substrate transfer processes, we have fabricated heterojunction bipolar transistors with submicrometer emitter-base and collector-base junctions, minimizing RC parasitics and increasing $f_{\max}$ to 500 GHz. The process also provides a microstrip wiring environment on a low-ϵ_r dielectric substrate. First design iterations of emitter-coupled-logic master–slave flip-flops exhibit 48 GHz maximum clock frequency when connected as static frequency dividers. Baseband amplifiers have been demonstrated with bandwidths up to 85 GHz.**

***Index Terms*—Baseband amplifier, heterojunction bipolar transistor (HBT), static frequency divider, substrate transfer.**

I. Introduction

APPLICATIONS—present and potential—for heterojunction bipolar transistors (HBT's) include radio-frequency (RF)/microwave analog–digital conversion, microwave direct digital frequency synthesis, and fiber-optic transmission in the range of 40–120 Gbits/s.

The motivation for high circuit bandwidth varies with the application. In fiber-optic transmission, fast IC's will directly enable increased time-division-multiplexed transmission rates, complementing increases in channel capacity provided by wavelength-division multiplexing. For oversampled $(\Delta$–$\Sigma)$ analog–digital converters, in-band quantization noise power decreases in proportion to the fifth power of the oversampling ratio (second-order modulators). Very-high-speed IC technologies offer the potential of Δ–Σ analog-to-digital converters (ADC's) with clock frequencies in the tens of gigahertz, providing high dynamic range—and large instantaneous bandwidth—over radio frequencies and lower microwave frequencies. In direct digital frequency synthesis, increases in logic IC clock rates and digital-to-analog-converter bandwidths will result in increased synthesizer bandwidth. Used in radar transmitters, modulation bandwidths can then be increased and frequency agility improved.

A 100-GHz clock rate IC technology would permit significant advances in the performance of such signal conversion IC's. To permit clock rates exceeding 100 GHz, significant issues in transistor design, interconnects, packaging, and thermal design must be addressed. The transistor current gain (f_τ) and power gain $(f_{\max})$ cutoff frequencies must be several hundred gigahertz. Wiring parasitics must be minimized. The interconnects must have small inductance and capacitance per unit length, and the wire lengths, and hence transistor spacings, must be small. Given that fast HBT's operate at $\sim 10^5$ A/cm^2 current density, efficient heat sinking is then essential. To provide predictable performance, interconnects of more than a few ps length must have a controlled characteristic impedance. To prevent circuit–circuit interaction through ground-circuit common-lead inductance ("ground loops"), the IC technology must provide an integral ground plane for ground-return connection. Similarly, to prevent circuit–circuit interaction between the IC's input and output lines, common-lead inductance between the IC and package ground systems must be made vanishingly small.

Competing technologies for 100-GHz logic include submicrometer SiGe (and Si) bipolar transistors [1], InP/InGaAs [2] or InAlAs/InGaAs [4] HBT's, and InAlAs/InGaAs HEMT's. InAlAs/InGaAs high electron mobility transistors (HEMT's) have extremely high bandwidths (200–300 GHz f_τ, 300–500 GHz $f_{\max}$) and have been used in quasi-dynamic IC's operating above 50 GHz [3]. Yet, circuit design is more difficult with InGaAs/InAlAs HEMT's (level shifting due to the negative $V_{\rm gs}$, large logic swing due to the low $g_m/I_{\rm dss}$ ratio). Due to difficulties with 0.1-μm lithography and gate recess etch control, present scales of integration with InAlAs/InGaAs HEMT's are well below the $\sim$3000 demonstrated with InP-based HBT's [4]. Si/SiGe HBT's in standard planar processes offer $\sim$100 GHz f_τ and $f_{\max}$, very high yields, and 8-in wafers. Further, $\sim 10^6$ A/cm^2 current densities in Si bipolars minimize $C_{\rm je}$ and $C_{\rm cb}$ charging times, resulting in clock frequencies at a higher fraction of f_τ than now obtained with III–V devices [1]. To win this competition, III–V HBT IC's must offer transistor bandwidths equal to—or better than—HEMT's, and three to five times that of Si. The technology must offer low inductance and low capacitance interconnects. IC's of $\sim$1000–5000 devices must be feasible. Δ–Σ analog–digital converters are now being fabricated with 350 transistors; efforts to develop IC's with larger scales of integration are forthcoming.

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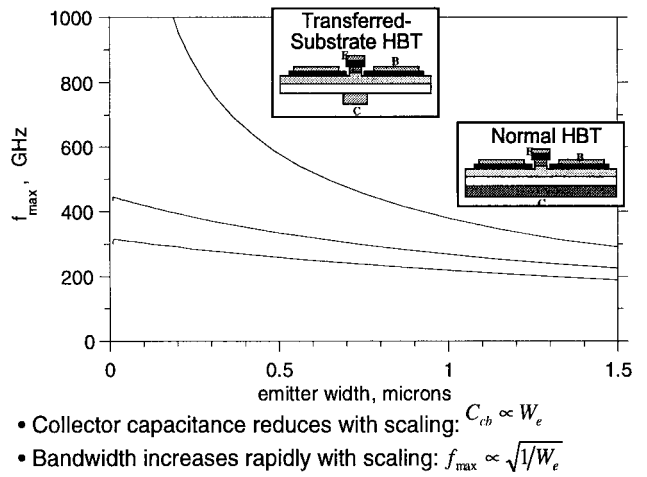


Fig. 1. Scaling of transferred-substrate and triple-mesa HBT's.

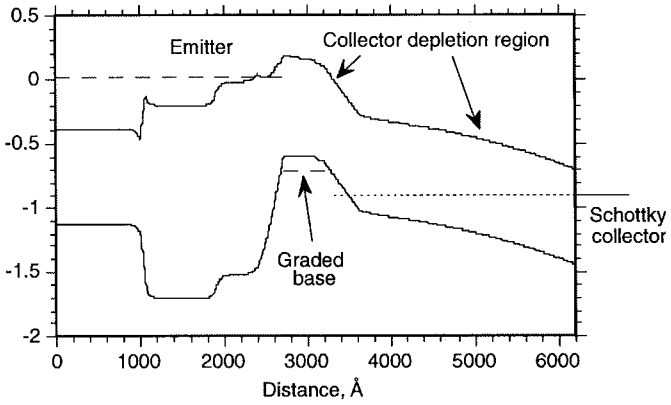


Fig. 2. Band diagram, under bias, of a typical device.

Wide-band HBT's are also needed in the gain blocks for these mixed-signal IC's and RF/microwave circuitry. We have also designed and tested simple broadband amplifiers as a first step in the development of these larger systems. These gain blocks will be converted to differential form and automatic gain control added to produce a gain stage for a fiber receiver, while differential versions of these amplifiers with capacitive feedback will be used as the integrators in delta–sigma ADC's.

II. Transferred-Substrate HBT's

Transferred-substrate HBT IC's [5] offer high transistor bandwidth, low wiring capacitance, and low wiring inductance. In this process, a substrate transfer step permits two-side processing of the device epitaxial layers, allowing definition of a transistor with narrow and aligned emitter-base and collector-base junctions.

In HBT's, f_τ is primarily determined by the base transit time τ_b, the collector transit time τ_c, and the emitter charging time $C_{\rm je}(kT/qI_e)$. Increases in f_τ are obtained by thinning the collector, by thinning and grading the base, and by increasing the emitter current density. Unfortunately, thinning the base and collector epitaxial layers increases the collector capacitance $C_{\rm cb}$ and the base resistance $R_{\rm bb}$, decreasing $f_{\max} = (f_\tau/8\pi R_{\rm bb}C_{\rm cbi})^{1/2}$. The base-collector junction is a distributed network and $R_{\rm bb}C_{\rm cbi}$ represents an effective, weighted time constant [6]. *For a fixed emitter stripe length,* decreasing the width W_e of the emitter-base junction decreases the base spreading resistance but does not decrease the base contact resistance. Scaling W_e reduces $R_{\rm bb}$ toward a minimum set by the contacts. Decreasing the width of the base-collector junction W_c decreases $C_{\rm cb}$.

In normal double-mesa HBT's (Fig. 1), the collector-base junction and base ohmic contact are defined in a single process step. The ohmic contacts must be at least one contact transfer length, setting a minimum collector junction width and a minimum collector capacitance. $R_{\rm bb}C_{\rm cb}$ has a minimum value, independent of lithographic limits, and $f_{\max}$ does not improve with scaling. In the transferred-substrate device, the collector width need only be larger than the emitter width. Reducing W_c and W_e progressively reduces $R_{\rm bb}C_{\rm cb}$, and $f_{\max}$ increases rapidly with scaling (Fig. 1). With lateral scaling alone, $f_{\max}$ should approach 1 THz as dimensions are scaled to $\sim$0.1 μm. Subsequently thinning the base and collector layers increases f_τ at the expense of $f_{\max}$. Simultaneous high values for both f_τ and $f_{\max}$ are thus obtained.

III. Growth and Fabrication

Fig. 2 shows the band diagram associated with a typical transferred-substrate HBT layer structure. The InGaAs base is nominally 400–500-Å thick, has kT–$2kT$ bandgap grading, and is Be-doped at $5 \cdot 10^{19}$/cm^3. The InGaAs collector has 2000–3000-Å thickness. A collector N^+ pulse-doped layer placed 400 Å from the base delays the onset of base pushout at high collector current densities. Devices typically use Schottky collector contacts [8], although HBT's with N+ subcollector layers (ohmic-collector devices) have also been fabricated. While ohmic-collector devices have nonzero collector series resistance, and hence lower $f_{\max}$ [6], the 0.2-V barrier present in the Schottky-collector device increases the $V_{\rm ce}$ required to suppress base pushout at high current densities. Ohmic-collector devices thus show higher $f_{\max}$ under the low-$V_{\rm ce}$ conditions associated with current-mode logic (CML). Schottky-collector devices are used for emitter-coupled logic (ECL), where the operating $V_{\rm ce}$ is higher.

Fig. 3 shows the process flow. Standard fabrication processes [4] define the emitter-base junction, the base mesa, polyimide planarization, and the emitter contacts. The substrate transfer process commences with deposition of the PECVD Si_3N_4 insulator layer and the benzocyclobutene (BCB) transmission-line dielectric (5 μm thickness). Thermal and electrical vias are etched in the BCB. The wafer is electroplated to metalize the vias and to form the ground plane. Subsequently, the wafer is indium-bonded to a GaAs carrier substrate and the InP substrate removed in HCl. Schottky collectors are then deposited, completing the process.

In the collector deposition step, collectors must be aligned to the HBT emitter stripe. Prior to substrate transfer, the alignment marks are metal features (formed during the emitter metal deposition) lying on the surface of the semiconductor substrate. During substrate transfer, these marks are first

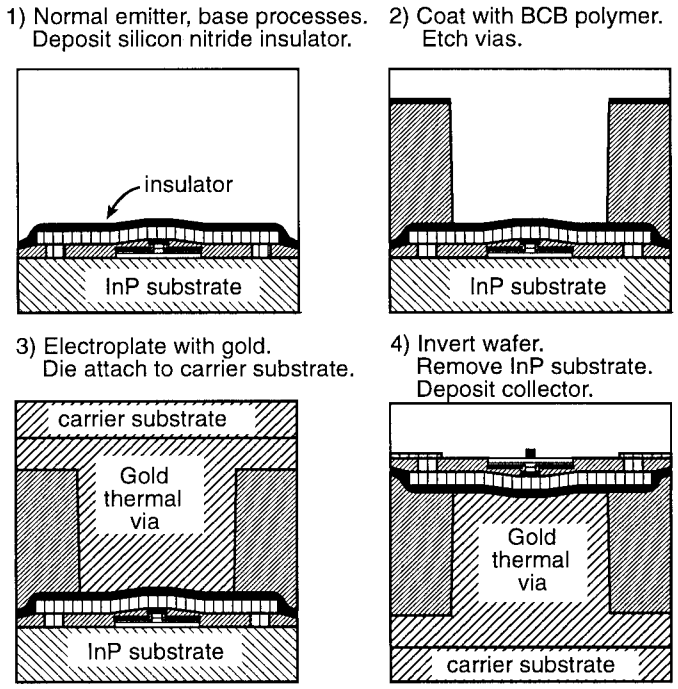


Fig. 3. Transferred-substrate HBT process flow.

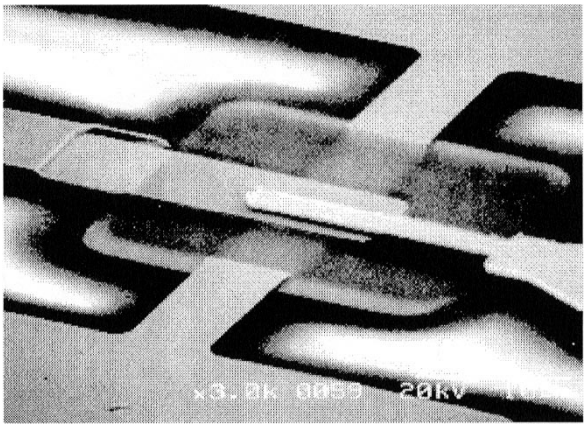


Fig. 4. Transferred-substrate HBT defined by contact lithography.

enveloped by the BCB and subsequently exposed during substrate removal. The alignment marks are thus visible on the wafer surface during collector lithography. The IC's reported here were fabricated on quarters of 2-in-diameter wafers. More recently, transferred-substrate IC's have been fabricated on full 2-in wafers.

In addition to HBT's with narrow emitter and collector stripes, the process provides thermal vias for HBT heatsinking, NiCr resistors, Si_3N_4 MIM capacitors, and microstrip wiring on a $\epsilon_r = 2.7$ dielectric with vias, ground plane, and three levels of interconnects. To tolerate high power densities, the NiCr resistors must have thermal vias, which results in significant parasitic capacitance. Pullup resistors in ECL do not require the thermal via.

A significant missing feature is in packaging. In the present process, the microstrip ground plane is isolated from the wafer back surface by the GaAs transfer substrate, increasing thermal resistance and preventing low-inductance connections between the IC and package ground. A modified process with a fully metallic electroplated copper substrate is in development [7]. This will provide highly effective heatsinking (395 W/M·K for Cu versus 74 for InP) and, with a package-IC ground interface over the full IC back surface, very low package-chip ground inductance.

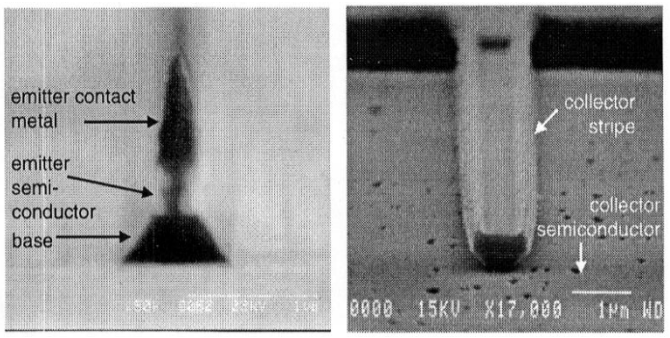
IV. Device Performance

Devices have been fabricated using contact lithography at 1–2-μm resolution, using a 0.5-μm stepper and electron-beam lithography. Fig. 4 shows a device with a 0.6 by 8 μm^2 emitter and a 1.6 by 12 μm^2 collector. In this device, the base ohmic contacts are 4 μm wide on either side of the emitter stripe. The device exhibits 215 GHz peak f_τ, and peak $f_{\max}$ above 400 GHz. Fig. 5 shows HBT emitter-base and collector-base junctions defined by electron-beam lithography. Submicrometer devices fabricated by E-beam lithography (Fig. 6) exhibit 500 GHz $f_{\max}$ [9]. Neither contact lithography nor electron-beam lithography is suitable for fabrication of large IC's. We have recently fabricated HBT IC's using a 0.5-μm projection lithography system and have obtained microwave gains (and $f_{\max}$) significantly higher than that shown in Fig. 6.

In determining the transistor power-gain cutoff frequency $f_{\max}$, we have extrapolated at -20 dB/decade using Mason's invariant (unilateral) power gain U [10]. U does not vary if the transistor is embedded in a lossless reciprocal network. For this reason, U, and hence $f_{\max}$ determined from extrapolation of U, is rigorously independent of the extraction of transistor pad parasitics. Further, U is independent of the transistor configuration (common base versus common emitter). Other commonly quoted power gains include the maximum available power gain (MAG), relevant for those frequencies where the device is unconditionally stable, and the maximum stable power gain (MSG), relevant for those frequencies where the device is potentially unstable. As only one of these two gains is relevant at any particular frequency, MAG and MSG are commonly plotted as a single function of frequency (MAG/MSG).

Using a hybrid-π equivalent-circuit model with typical HBT parameters [Fig. 7(a)], Fig. 7(b) plots MAG, MSG, and Mason's gain U in common-emitter, common-base, and common-collector configurations, as computed using a microwave circuit simulator. It is evident that MAG and MSG are strongly dependent upon the transistor configuration. Although not shown in Fig. 7, MAG and MSG are also dependent upon those transistor pad parasitics that create parasitic feedback (source/emitter inductance, parasitic capacitance between input and output pads). As required by circuit theory, MAG, MSG, and U, independent of transistor configuration, all reach 0 dB at a single and unique power-gain cutoff frequency $f_{\max}$. For a transistor well characterized by a hybrid-π model, the variation of U with frequency conforms very closely to a -20 dB/decade slope, while MAG and MSG show no particular fixed variation with frequency.

In characterizing a transistor whose $f_{\max}$ exceeds that of the available instrumentation, extrapolation of MAG or MSG



(a) (b)

Fig. 5. E-beam HBT: (a) test structure with 0.15-μm emitter-base junction and (b) 0.4-μm Schottky collector stripe.

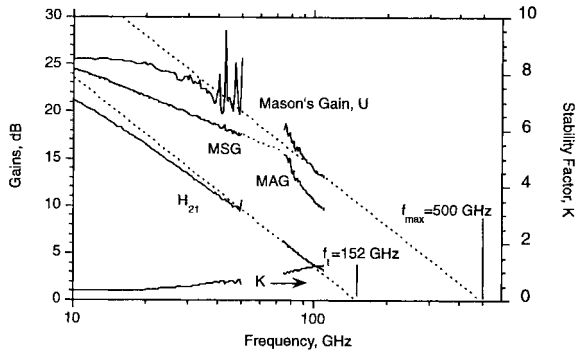


Fig. 6. W-band gains of device with a 0.4 $\times$ 25 μm^2 emitter and a 1.0 $\times$ 29 μm^2 collector.

at -20 dB/decade will result in an extrapolated $f_{\max}$ whose value depends upon the highest frequency of measurement. U does not suffer from this difficulty. In microwave circuit design, a circuit power gain equal to the transistor's unilateral gain U is obtained by the combination of impedance matching and unilateralization through the addition of lossless reactive feedback. Without unilateralization, the maximum gain is constrained by the MAG/MSG. With HBT's, this is generally highest in common-base mode.

Device scaling also reduces dc current gain and breakdown voltage. Base current in narrow-emitter InAlAs/InGaAs HBT's is predominantly due to conduction on the exposed InGaAs base surface between the emitter mesa and the base ohmic contact. β decreases with emitter width but increases as the base is thinned, as base bandgap grading is increased, and (at the expense of $f_{\max}$) as the emitter-base spacing is increased. $\beta > 50$ has been obtained with 0.2-μm emitters. The 2500-Å InGaAs collectors have very low breakdown, 1.5 V BV_{ceo}, 2 V BV_{cbo} *at* 1–2 $\cdot$ 10^5 A/cm^2 *current density*. Clearly, InP collectors should be used for highly scaled devices.

V. Digital IC Demonstration

As first digital IC's demonstrations, we fabricated ECL and CML master–slave D flip-flops, configured as 2 : 1 static frequency dividers [11]. Circuits were fabricated using contact lithography, producing devices with 0.6 $\times$ 8 μm^2 emitters and 1.6 $\times$ 12 μm^2 collectors. The devices operate at 1.25 mA/μm^2. Devices in the ECL dividers were of 3000 Å collector thickness and had Schottky collector contacts. Devices in the CML dividers were of 2000 Å collector thickness and had ohmic contacts to a 1000-Å-thick, $1 \cdot 10^{19}$/cm^3 Si-doped subcollector for improved performance at low V_{ce} bias. The differential logic swing is 600 mV. The collector pullup resistors are 50 Ω; hence the divider outputs directly drive 50-Ω output lines without buffering. Circuit design is entirely standard. The CML divider uses series-gated master and slave latches. Emitter-follower buffers are added to the CML clock and data ports to form the ECL divider. The IC's are shown in Fig. 8.

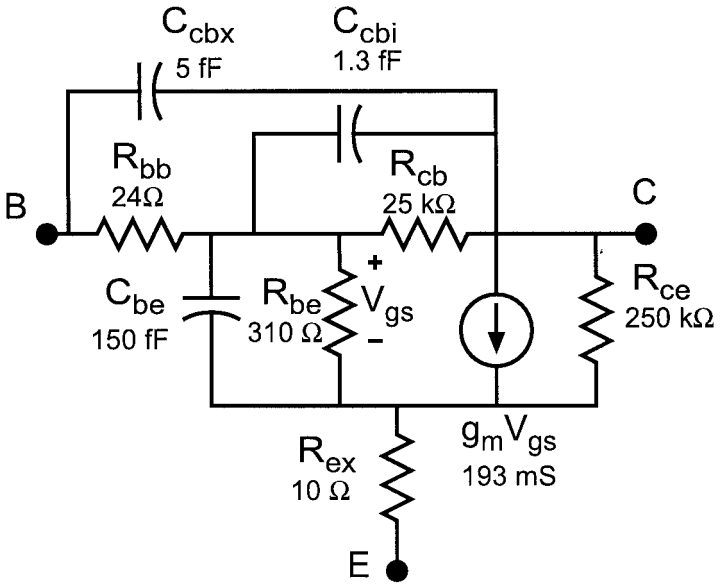
Measurement results are shown in Figs. 9 and 10. The CML and ECL static frequency dividers operated at maximum clock frequencies of 47 and 48 GHz. The circuits dissipate 380 mW (ECL) or 75 mW (CML) from a -5-V supply and have pad-limited 0.6 $\times$ 0.6 mm^2 die areas. The peak ECL clock speed of 70 GHz predicted from SPICE simulation (in which efforts were made to model all significant device and interconnect parasitics) does not correlate with the measured 48 GHz. We suspect that this discrepancy arises from strong emitter-follower gain peaking at 50 GHz. We have observed very strong $\sim$50-GHz gain peaking—inconsistent with SPICE simulation—in resistive feedback amplifiers [12], [13] and have suppressed it with shunt resistive loading at the emitter-follower output, as shown in the next section. Design studies now in progress suggest the feasibility of 100-GHz clock rates with the present HBT's, but the device models—and the circuits—remain to be validated.

VI. Amplifier Design and Results

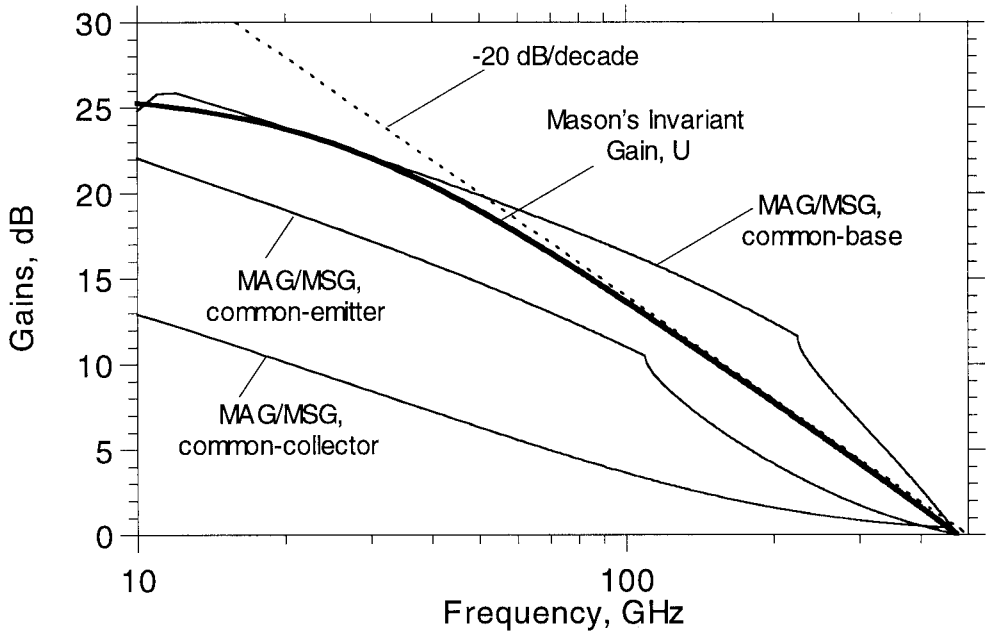
Two resistive feedback amplifiers have been fabricated. The first is a simple Darlington feedback amplifier. The second is a mirror doubler amplifier [15] driven by an emitter follower. Both amplifiers were fabricated on material with a 2000-Å-thick, Schottky contacted collector for high f_τ (250 GHz).

A circuit diagram for the Darlington feedback amplifier is shown in Fig. 11. A chip photo is shown in Fig. 12. Provision is made for independent biasing of the collector of Q1, requiring a third pad. The area of the chip is then pad limited at 0.52 $\times$ 0.43 mm^2, or 0.224 mm^2. Simulated values of dc gain and 3-dB bandwidth are 15.2 dB and 52 GHz, respectively. The radial stub bypass capacitors have a (simulated) capacitance of 300 fF. Tuning inductors and shunt resistors to ground are used on input and output to reduce reflection loss and increase bandwidth. The feedback path consists of a 350-Ω resistor in series with a small inductance. A thermal via is provided on each device, which on the input device represents a small but not negligible parasitic capacitance from the emitter to ground. This capacitance arises from the overlap of the M1 to the grounded M2 through the SiN dielectric.

Figs. 13 and 14 show a circuit diagram and chip photo of the mirror doubler amplifier. A third pad is also used in this design to provide independent collector bias of the emitter follower, resulting in the chip area of 0.224 mm^2. Simulated dc gain and 3-dB bandwidth are 7.5 dB and 94 GHz. Tuning inductors are also used in this design, as well as a shunt resistor to ground on the output. The diode Q4 is for dc-level shifting, to maintain

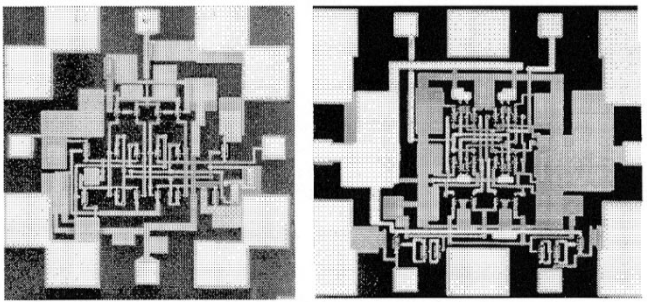


(a)



(b)

Fig. 7. Variation of transistor power gains versus frequency: (a) Hybrid-π model of a high-performance HBT. (b) Computed values from this model for Mason's gain U, and the common-emitter, common-base, and common-collector maximum available/maximum stable power gains.



(a) (b)

Fig. 8. (a) CML and (b) ECL master–slave D-flip-flops.

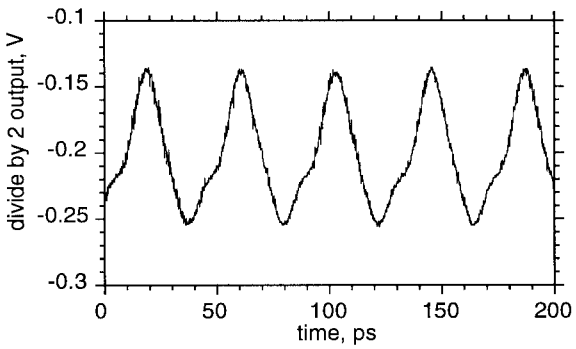


Fig. 9. CML static frequency divider output for 47-GHz input.

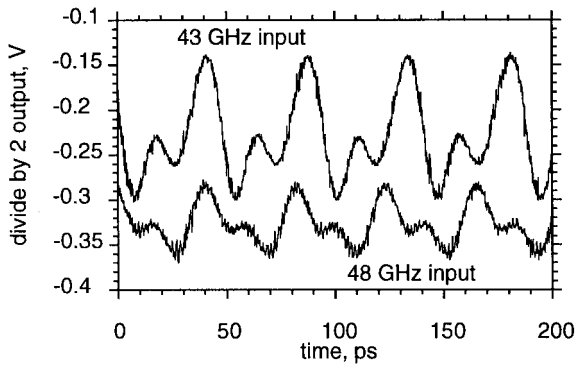


Fig. 10. ECL static divider output for 48- and 43-GHz inputs.

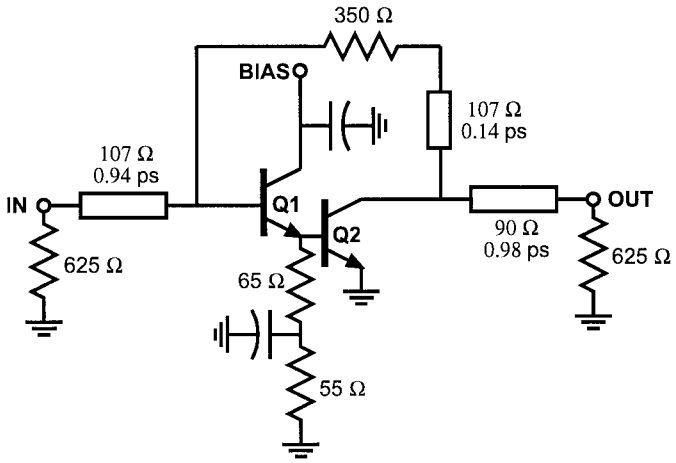


Fig. 11. Circuit diagram of Darlington amplifier. Line section characteristic impedance and electrical length as indicated.

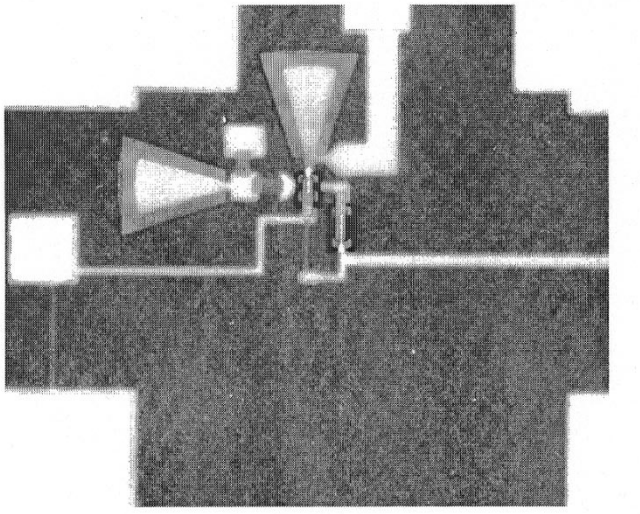


Fig. 12. Chip photo of Darlington amplifier.

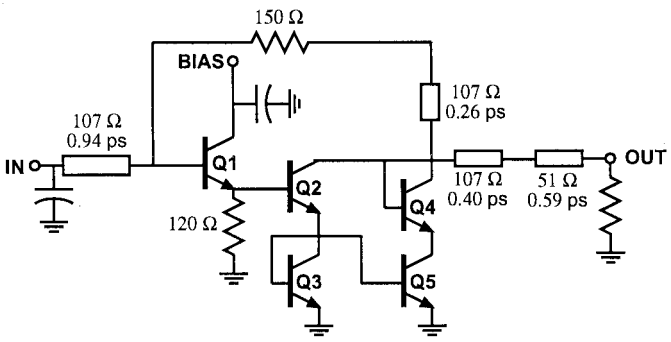


Fig. 13. Circuit diagram of mirror doubler.

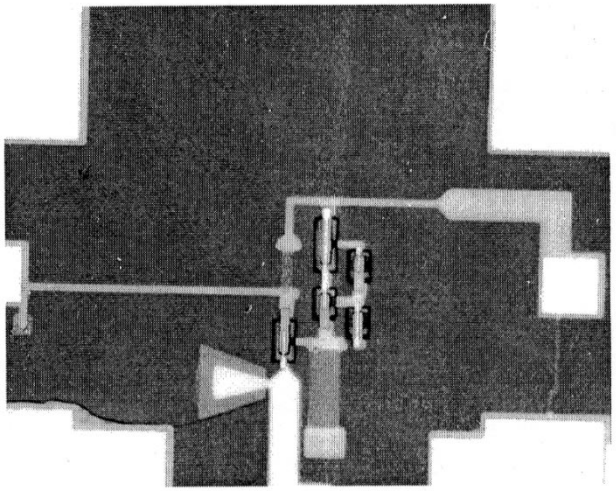


Fig. 14. Chip photo of mirror doubler amplifier.

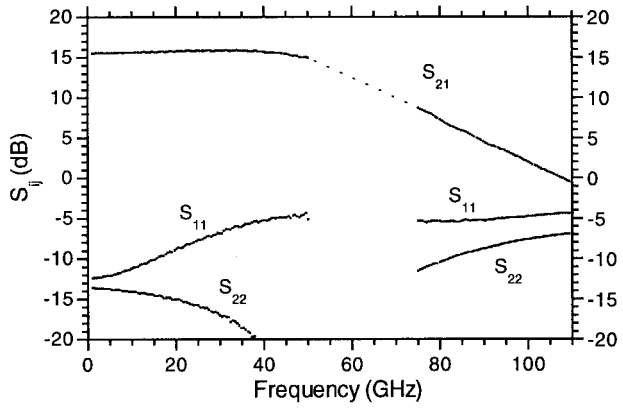


Fig. 15. Measured S parameters of the Darlington amplifier.

the V_{ce} of Q5 near the region of peak RF performance. The feedback path consists of a 150-Ω resistor in series with a small inductance.

In second-generation designs now in fabrication, the emitter degeneration resistance of the emitter follower is replaced by a current mirror bias source. As this resistance in the amplifiers reported here provides shunt stabilization of the emitter follower, in the redesigned amplifiers the current mirror bias source is bypassed at high frequencies by a series RC network.

The amplifiers were measured on wafer from 0.5 to 50 GHz and from 75 to 110 GHz. S-parameters versus frequency are plotted in Figs. 15 and 16 for the Darlington amplifier and

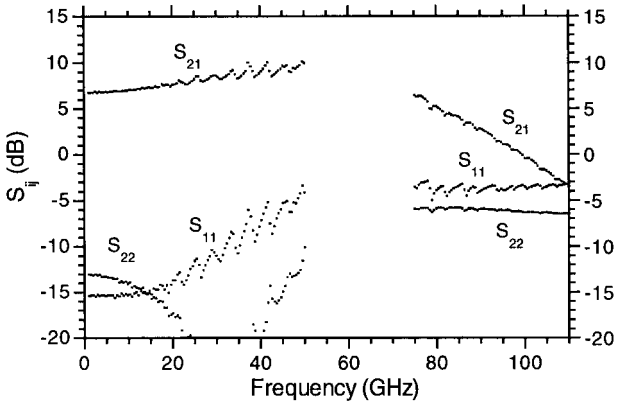


Fig. 16. Measured S parameters of the mirror doubler amplifier.

the mirror doubler amplifier, respectively. The dc gain of the Darlington amplifier is close to simulation at 15.6 dB, with a 3-dB bandwidth that is greater than 50 GHz. The gain peaks at 16.0 dB and falls to 14.9 dB at 50 GHz. At 75 GHz, the gain has fallen to 8.8 dB, preventing precise determination of the 3-dB bandwidth. S_{22} remains below -13 dB from dc–50 GHz, but S_{11} rises to -4.5 dB at 50 GHz. Amplifier designs were based upon device models from previously processed wafers. The device characteristics and the BCB dielectric thickness have evolved since that time. In this case, the input tuning network is not appropriate for the input impedance of the realized device. The power dissipation is 36.3 mW.

The dc gain of the mirror doubler amplifier is 6.8 dB. The gain steadily rises with frequency until at least 50 GHz, where it reaches 9.5 dB. The frequency at which the gain has dropped to 3 dB below the dc gain is 85 GHz. S_{11} rises to -3.5 dB at W-band, and S_{22} rises to -6 dB. This is again due to improper device modeling during circuit design. The power dissipation is 24.2 mW.

VII. Conclusion

Digital IC's of 100 GHz require a high-bandwidth transistor, low-parasitic interconnects, and effective heatsinking. Using substrate-transfer processes, HBT's can be fabricated with highly scaled lithographic and epitaxial dimensions, giving both high f_τ and high $f_{\max}$. Initial designs yielded 48-GHz digital IC's [11] and 50–85-GHz amplifiers [12]–[14]. With further scaling and improved circuit design, 100-GHz digital IC's will be feasible. Improvements have been made in transistor performance as well as in the design of master–slave flip-flops and baseband amplifiers, promising significant performance improvements over the results reported here. This is due to improvements in the circuit design as well as reduced transistor critical dimensions resulting from the incorporation of a projection lithography system into the process. These IC's are still undergoing testing, and results will be reported subsequently.

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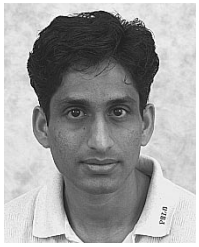

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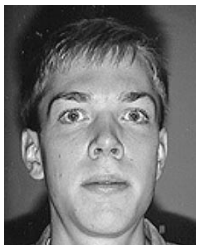

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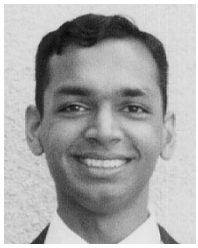

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