Submicron Transferred-Substrate Heterojunction Bipolar Transistors

Q. Lee, S. C. Martin, D. Mensa, R. P. Smith, J. Guthrie, and M. J. W. Rodwell

***Abstract*— We report submicron transferred-substrate AlInAs/GaInAs heterojunction bipolar transistors (HBT's). Devices with 0.4-μm emitter and 0.4-μm collector widths have 17.5 dB unilateral gain at 110 GHz. Extrapolating at −20 dB/decade, the power gain cutoff frequency $f_{\max}$ is 820 GHz. The high $f_{\max}$ results from the scaling of HBT's junction widths, from elimination of collector series resistance through the use of a Schottky collector contact, and from partial screening of the collector-base capacitance by the collector space charge.**

***Index Terms*— Heterojunction bipolar transistors, substrate transfer.**

I. Introduction

VERY wide bandwith heterojunction bipolar transistors (HBT's) [1], [2] will enable microwave analog-digital converters, microwave direct digital frequency synthesis, fiber-optic transmission at >40 Gb/s, and wireless data networks at frequencies above 100 GHz.

Such IC's will demand very high transistor current gain cutoff frequency f_τ, and power gain cutoff frequency $f_{\max}$. Increases in f_τ are obtained by thinning the collector, and by thinning and grading the base. Unfortunately, thinning the base and collector epitaxial layers increases the base-collector capacitance C_{cb} and the base resistance R_{bb}, decreasing $f_{\max} \sim \sqrt{f_\tau/8\pi R_{bb}C_{cbi}}$ where C_{cbi} is the fraction of C_{cb} charged through the base resistance R_{bb}. Using substrate-transfer processes [3], HBT's can be fabricated with narrow emitter/base and collector/base junctions on opposing sides of the base epitaxial layer. Reducing the emitter and collector widths progressively reduces $R_{bb}C_{cb}$, and hence $f_{\max}$ increases rapidly with scaling. Subsequently thinning the base and collector epitaxial films will increase f_τ at the expense of $f_{\max}$, and high values of both f_τ and $f_{\max}$ are thus obtained.

We had earlier reported transferred-substrate heterojunction bipolar transistors with 0.8-μm collector junction width and >400 GHz $f_{\max}$ [3]. Here, we report submicron devices fabricated using electron-beam lithography and (for dimensional control) combined reactivation and wet-chemical etches. Devices with 0.4-μm emitter and 0.4-μm collector width obtained dc current gain $\beta = 50$ and 17.5 dB unilateral power gain at 110 GHz. Extrapolating at −20 dB/dec results in an estimated 820 GHz $f_{\max}$, the highest reported for any transistor.

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II. Device Design and Fabrication

The MBE epitaxial layer structure used in this work is identical to [3], except that the base is 400 Å thick, is Be-doped at $5 \cdot 10^{19}/\text{cm}^3$, and uses 50 meV base bandgap grading, introduced by varying the Ga : In ratio. As in [3], the collector is 3000 Å thick, and uses an N^+ pulse doped layer [4] 400 Å from the base to delay base push-out and to act as an electron launcher.

The fabrication process is similar to that described in [3]. Emitter contact metal is defined by E-beam lithography at 0.5 μm linewidth. The emitter-base junction is formed by $CH_4/Ar/H_2$ reactive-ion-etching with subsequent selective (acetic/HBr/HCl) and nonselective citric-based wet etches. The etch undercuts 0.05 μm, producing 0.4-μm emitter width. Subsequent steps include self-aligned base Ohmic contact deposition, base mesa isolation, polyimide passivation and planarization, and interconnect metal evaporation. The substrate transfer process includes Benzocyclobutene (BCB) deposition, etching and plating to form vias and ground planes, bonding to a transfer substrate with an $In_{0.4}Pb_{0.6}$ solder, and InP host substrate removal in HCL. Collector metal, with a "T" cross section, is then defined by E-beam lithography at 0.5 μm contact width [Fig. 1(a)]. An isotropic collector recess etch to 0.05 μm depth forms collector-base junctions with a tapered profile, reducing C_{cb} while maintaining latitude for emitter-collector misalignment. After etching collector junction width is 0.4 μm. A device schematic cross section is shown in Fig. 1(b).

III. Results

The devices were characterized by HP8510 on-wafer network analysis from 0 to 50 GHz and 75 to 110 GHz using (GGB, Inc.) waveguide-coupled microwave wafer probes. To avoid measurement errors (in S_{12}, hence U) arising from microwave probe-probe coupling, the HBT's are separated from the probe pads by 230-μm length on-wafer microstrip lines. On wafer calibration standards were used to de-embed the transistor S-parameters. The standard line-reflect-line (LRL) technique was used, with microstrip through line, extended lines for 20–50 GHz and 75–110 GHz calibration, and offset shorts and opens for the reflect standard and for verification.

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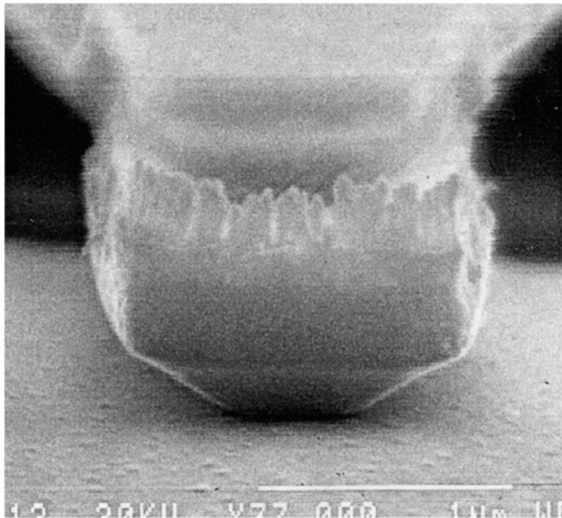
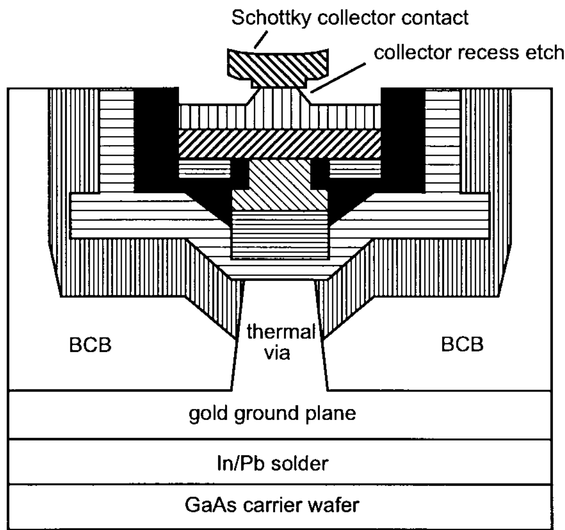


(a)



(b)

Fig. 1. (a) A 0.4-μm Schottky collector stripe and (b) schematic cross section of transferred substrate HBT.

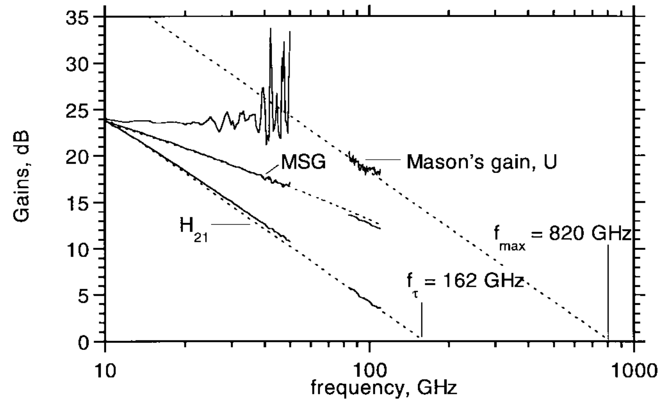


Fig. 2. Common-emitter RF characteristics of device with a 0.4×6 μm^2 emitter and a 0.4×10 μm^2 collector, biased at $V_{ce} = 1.2$ V and $I_c = 5$ mA.

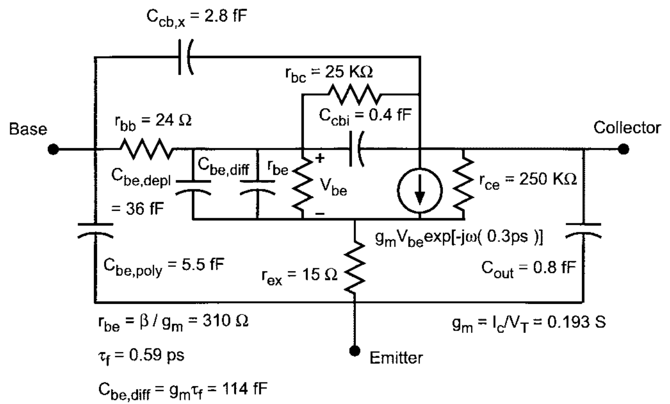


Fig. 3. Device equivalent circuit model at $V_{ce} = 1.2$ V and $I_c = 5$ mA.

Biasing at $V_{ce} = 1.2$ V and $I_c = 5.0$ mA, devices with 0.4-μm emitter and 0.4-μm collector widths obtained 3.2 dB current gain and 17.5 dB unilateral power gain at 110 GHz (Fig. 2). Extrapolating at -20 dB/decade, the current gain cutoff frequency f_τ is 162 GHz and the power gain cutoff frequency $f_{\max}$ is a record 820 GHz. The common-emitter (Fig. 2) and common-base (not shown) maximum stable gains are 12.2 and 16.0 dB at 110 GHz.

Fig. 3 shows a small-signal hybrid-π model for a device with a 0.4×6 μm^2 emitter and a 0.4×10 μm^2 collector biased at $I_c = 5$ mA and $V_{ce} = 1.2$ V. Base resistance R_{bb} consists of spreading resistance, contact resistance, and base-emitter gap resistance. The measured base sheet resistance is 600 $\Omega/\Box$ and the specific contact resistance is 50 Ω-μm^2. With these parameters, we calculate a 24 Ω base resistance. $R_{ex} = 15$ Ω is determined by plotting Re$\{Y_{21}\}$ versus $1/I_c$. By plotting $1/2\pi f_\tau$ versus $1/J_e$, it is determined that the sum of the base and collector transit times $(\tau_b + \tau_c)$ is 0.59 ps, and the sum of the collector-base and base-emitter depletion capacitances $(C_{cb} + C_{be,\,depl})$ is 39 fF. R_{cb} and the total C_{cb} are extracted by plotting the real and imaginary part of the admittance parameter Y_{12} versus frequency. R_{cb} represents variation of collector-base leakage with bias, likely due to impact ionization. Base-width modulation in HBT's is negligible, hence R_{ce} is large. $C_{be,\,poly}$ is a calculated metal-polyimide-metal overlap capacitance between the emitter and base metallizations. The 3.2 fF sum of C_{cbi} and C_{cbx} is of the magnitude expected from the combination of $(\epsilon A_c/T_c)$ 1.5 fF collector junction capacitance and ($\sim$10 μm $\times$ 150 fF/mm) metal-metal fringing capacitance between the base ohmic metal and the transmission line contacting the collector. Inclusive of the differential space-charge effect [5], [6], observed earlier in MESFET's [7], $C_{cbi} = \epsilon A_E/T_c - I_c \partial\tau_c/\partial V_{ce}$, where T_c is collector thickness and $\partial\tau_c/\partial V_{ce}$ is the variation in collector transit time with bias. The measured f_τ versus V_{ce} (Fig. 4) indicates $\partial\tau_c/\partial V_{ce} \cong$ 0.05–0.15 ps/V, predicting $C_{cbi} \cong$ 0.13–0.63 fF at $I_c = 5$ mA. $C_{cbi} = 0.4$ fF is determined by fitting to the measured unilateral gain. This is 2.2 : 1 smaller than the expected zero-current capacitance ($\epsilon A_E/T_c = 0.88$ fF). The measured S-parameters (Fig. 5), h_{21} and U show good correlation to that of the hybrid-π model.

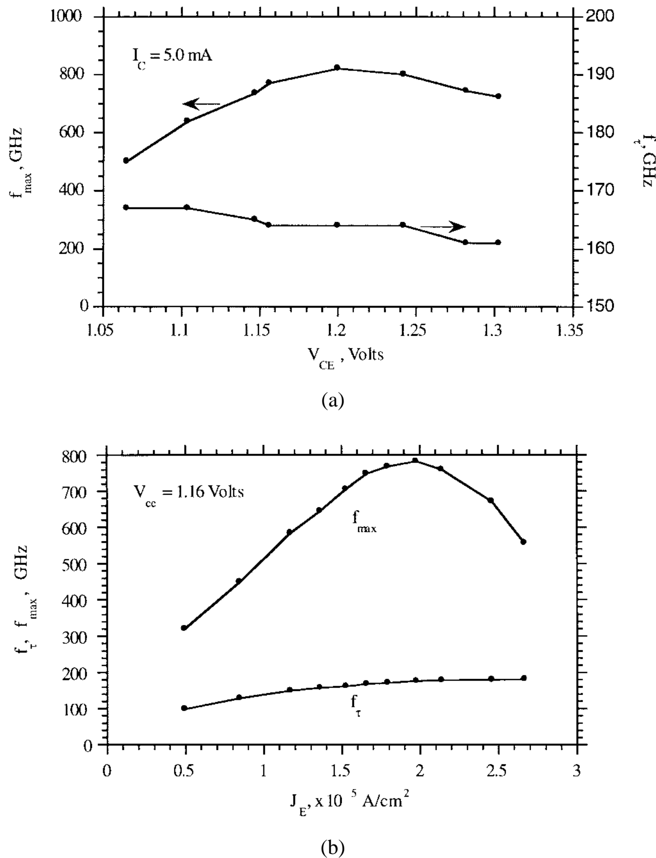


Fig. 4. (a) Variation of f_τ and $f_{\max}$ with collector-emitter voltage V_{ce} and (b) variation of f_τ and $f_{\max}$ with emitter current density J_e.

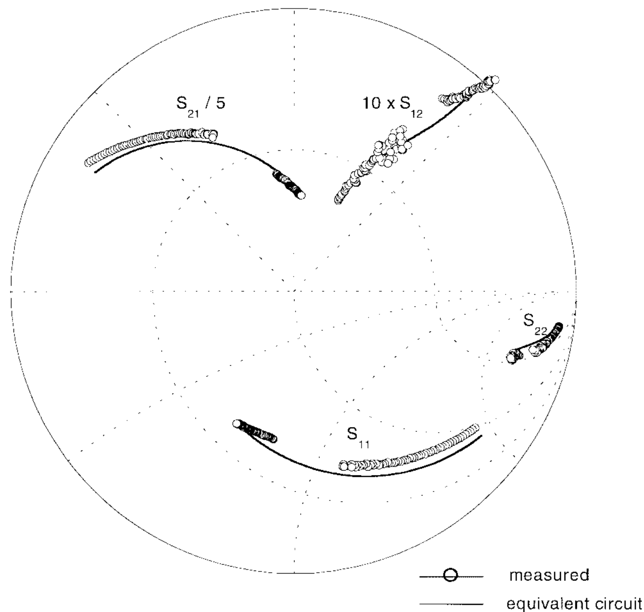


Fig. 5. Measured device S-parameters at $V_{ce} = 1.2$ V and $I_c = 5$ mA. The solid line represents S-parameters of the equivalent circuit model.

Due to difficulties with electron exposure during collector lithography on the present wafer, device yields were in the range of 50%. In other process runs using optical projection lithography, yields above 70% are obtained for 76-transistor IC's [8].

In comparing the present results with those reported in [3], the high $f_{\max}$ results from scaling of HBT junction widths and from partial screening of the collector-base capacitance by the collector space charge. Normalizing to the emitter junction area A_E to correct for differing device sizes, devices reported in [3] exhibited $R_{bb}A_E = 72$ Ω-μm^2 and $C_{cbi}/A_E = 0.42$ fF/μm^2 versus $R_{bb}A_E = 58$ Ω-μm^2 and $C_{cbi}/A_E = 0.17$ fF/μm^2 for those reported here. The reduction in $R_{bb}A_E$ results from scaling, while the reduction in C_{cbi}/A_E results from the reduction of C_{cbi} through the differential space-charge effect [5]–[7] under the combined conditions of high current density and high collector-emitter bias voltage. At 0.4 μm, the collector-base junction width is $\sim$10 : 1 smaller than in typical HBT's reported in the literature.

IV. Conclusions

We have demonstrated submicron transferred-substrate heterojunction bipolar transistors. Devices with 0.4×6 μm^2 emitters and 0.4×10 μm^2 collectors obtained an extrapolated f_τ, of 162 GHz and $f_{\max}$ of 820 GHz. With further scaling, HBT's with >1000 GHz $f_{\max}$ should be feasible, permitting IC's operating above 300 GHz [8].

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