1999 IEEE Workshop
Interconnections within High-Speed Digital Systems

Device and Interconnect Technologies for ~100 GHz mixed-signal ICs

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Device and Interconnect Technologies for ~100 GHz mixed-signal ICs

Two topics:

*ICs *__for__* high-frequency interconnects*

RF/wireless, optical fiber

*ICs *__needing__* high-frequency interconnects*

100 GHz digital logic, GHz ADCs/DACs

The organization:

what are the future applications ?

what are the requirements ?

what is the state of the art ?

challenges for future high speed ICs

…and how my group is attacking them

Applications:

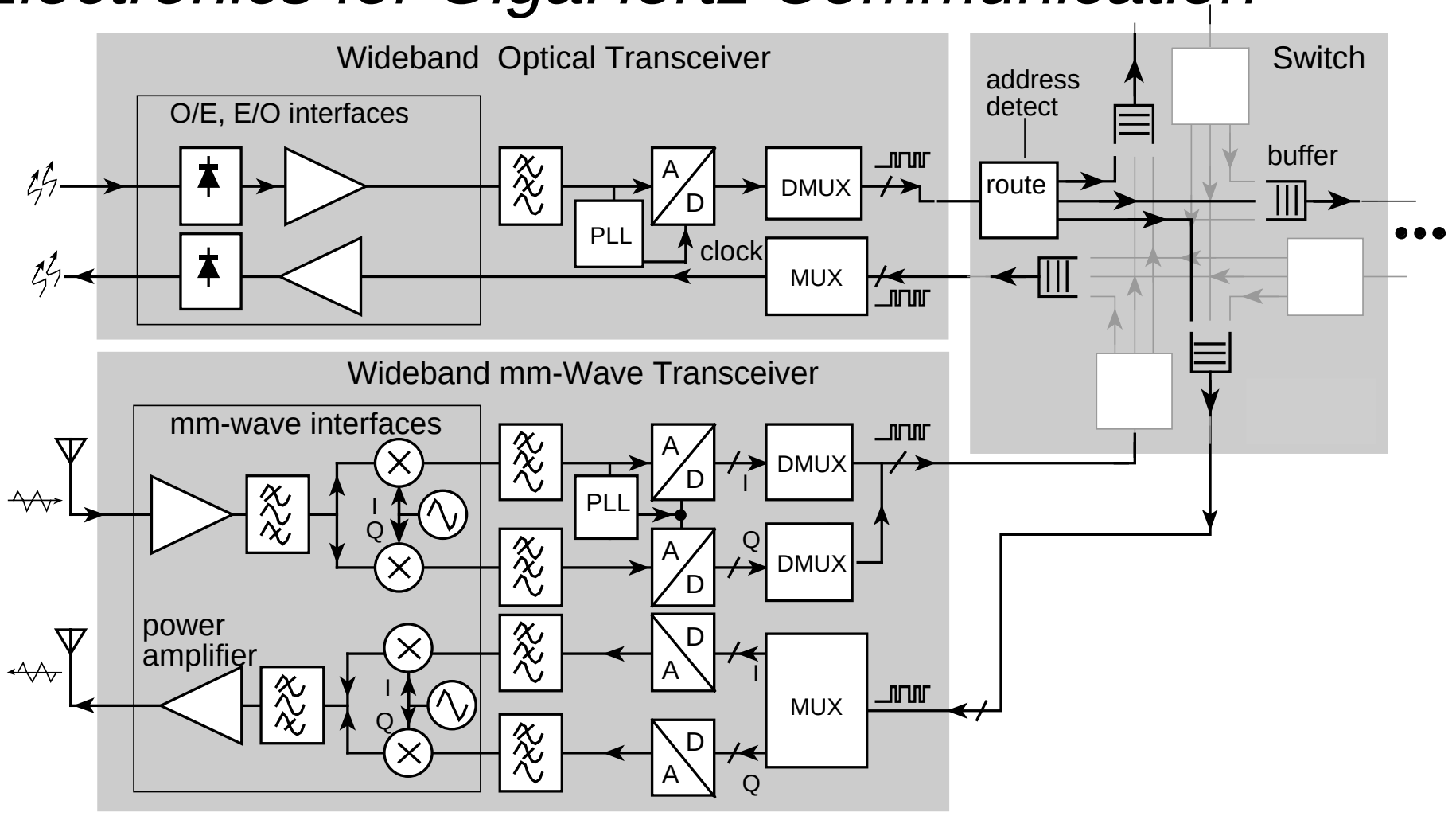
*ICs *__for__**

high-frequency interconnects

*ICs *__needing__**

high-frequency interconnects

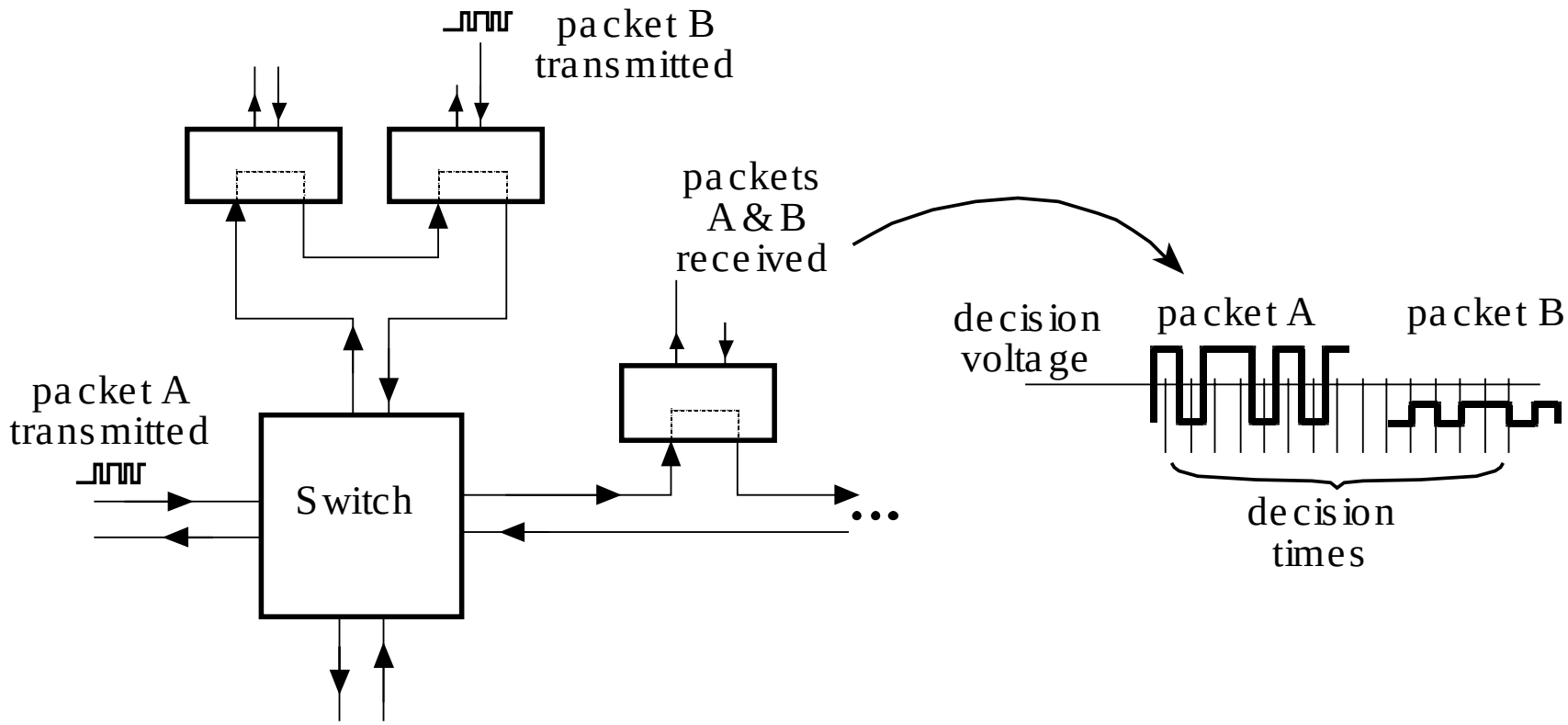
Electronics for GigaHertz Communication



***Transceivers**: very fast digital & mixed-signal ICs*
***Interfaces**: very wideband analog circuits, optoelectronics, mm-wave power*
***Switches**: ~10 GHz fast complex digital ICs*

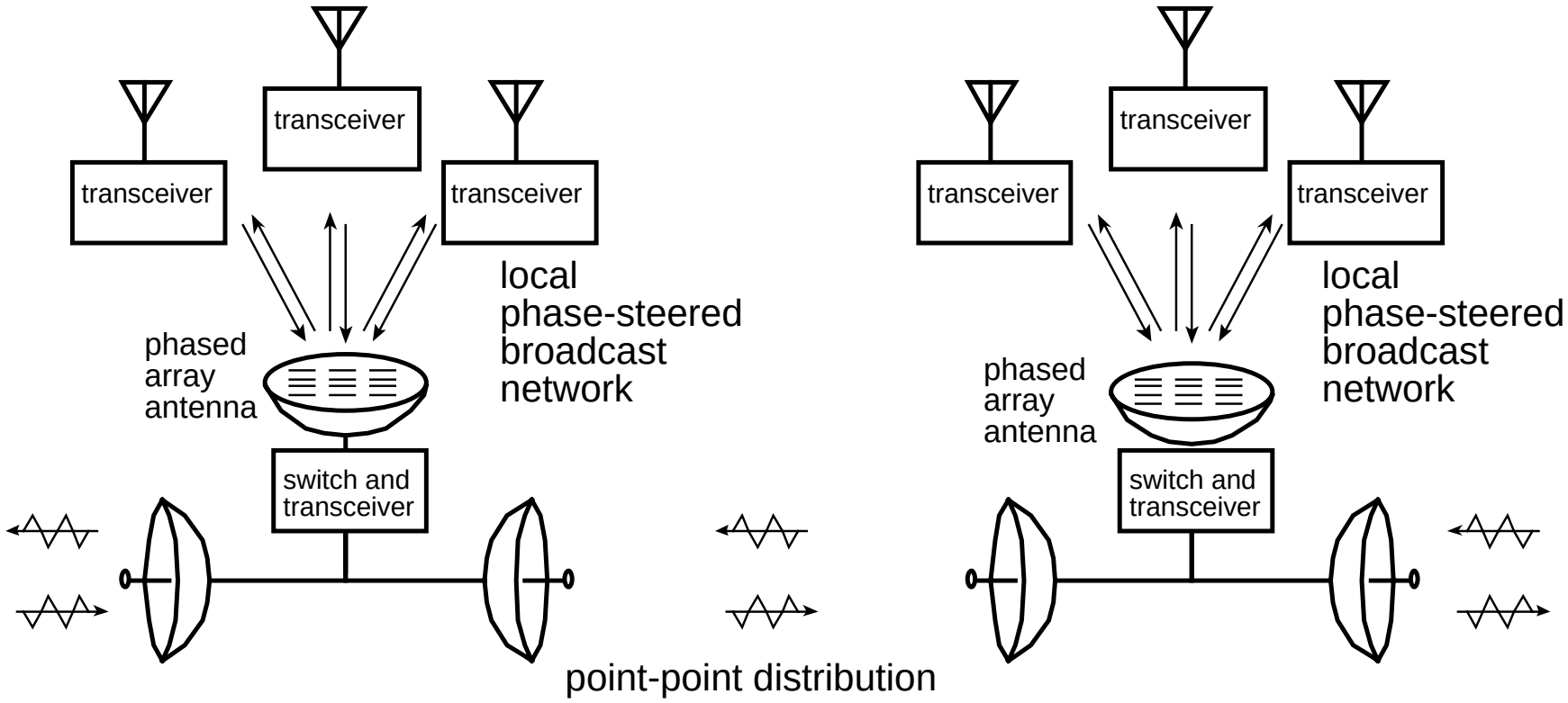
Why electronic switching remains important

Packet switching in a transparent (optical) switch



Burst errors will arise due to timing and amplitude glitches
Fix with digital (electronic) regeneration at switch -> all digital network

Wireless Digital Transmission: Networks & Distribution



Point-point links: 80 GHz, ~200 GHz line-of-sight

capacities of 10s of Gb/s

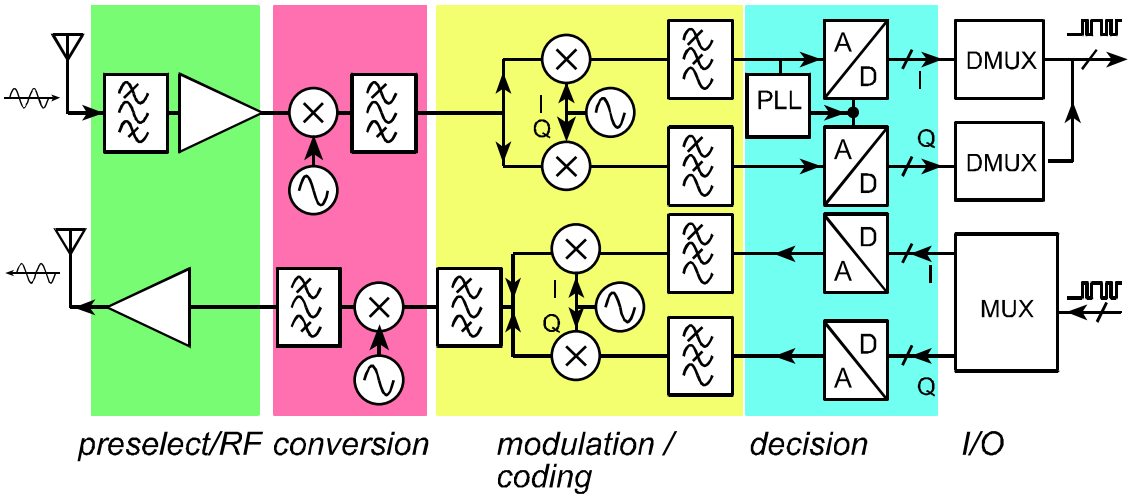
Broadcast links: 60 GHz, 120 GHz, ….

phased-array beamsteering

CDMA spread-spectrum coding for multipath

RF/Microwave ADCs/DACs/DDS: Towards the "Software Radio"

Transceiver: Today



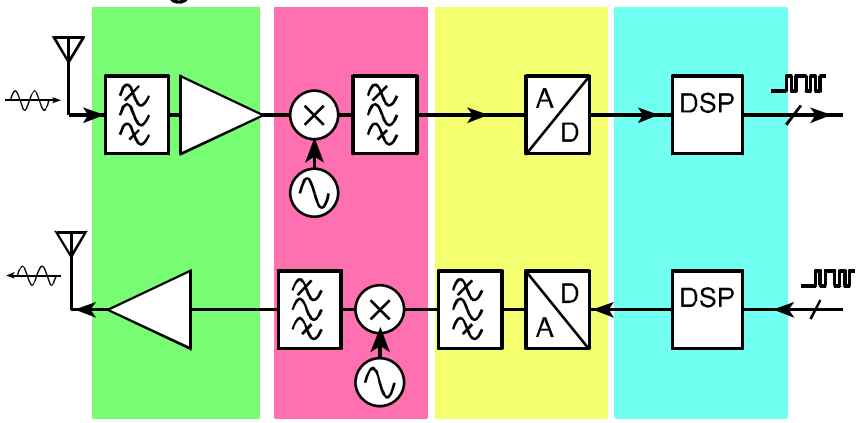
Advantages

digital robustness, frequency agility
complex modulation (spread spectrum...),
simultaneous operation on many bands

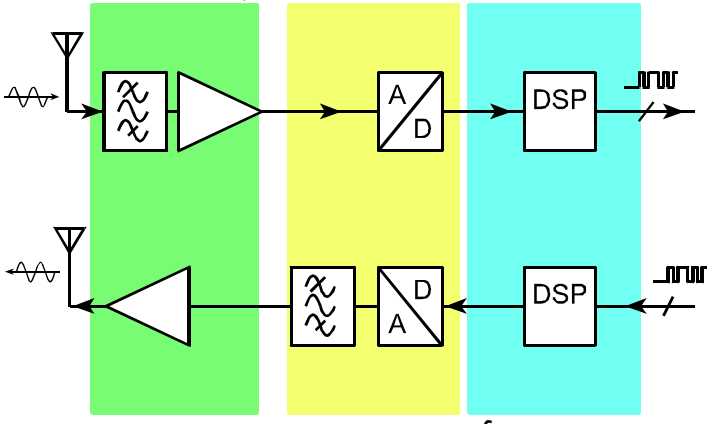
Challenges

*ADC needs **enormous** dynamic range*
DAC also must have very high SNR
Enormous data reduction in DSP:
very complex, very fast logic

Digital Modulation Transceiver

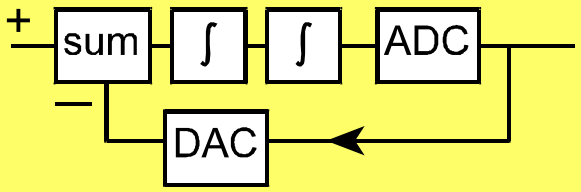


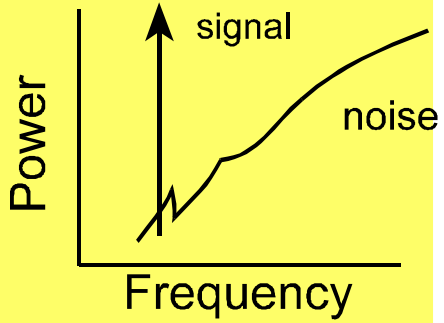
All Digital Transceiver



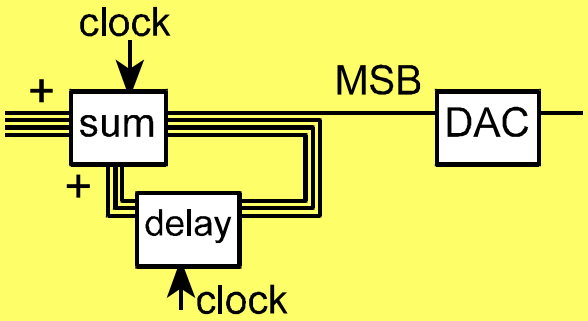
High resolution ADCs/DACs need high IC speed

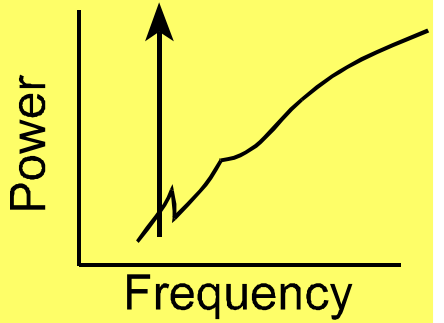
Delta-Sigma (noise shaping) ADC





Interpolating (noise shaping) DAC





ADCs/DACs for radio:

high dynamic range required (10-18 bits)

Oversampling ADCs/DACs:

high resolution obtained through high oversampling

Microwave ADCs need very fast logic, very fast transistors

Requirements: 100 GHz clock-rate logic

Fast transistors:

ADCs etc need very high ratio of transistor to signal bandwidth

High performance wiring :

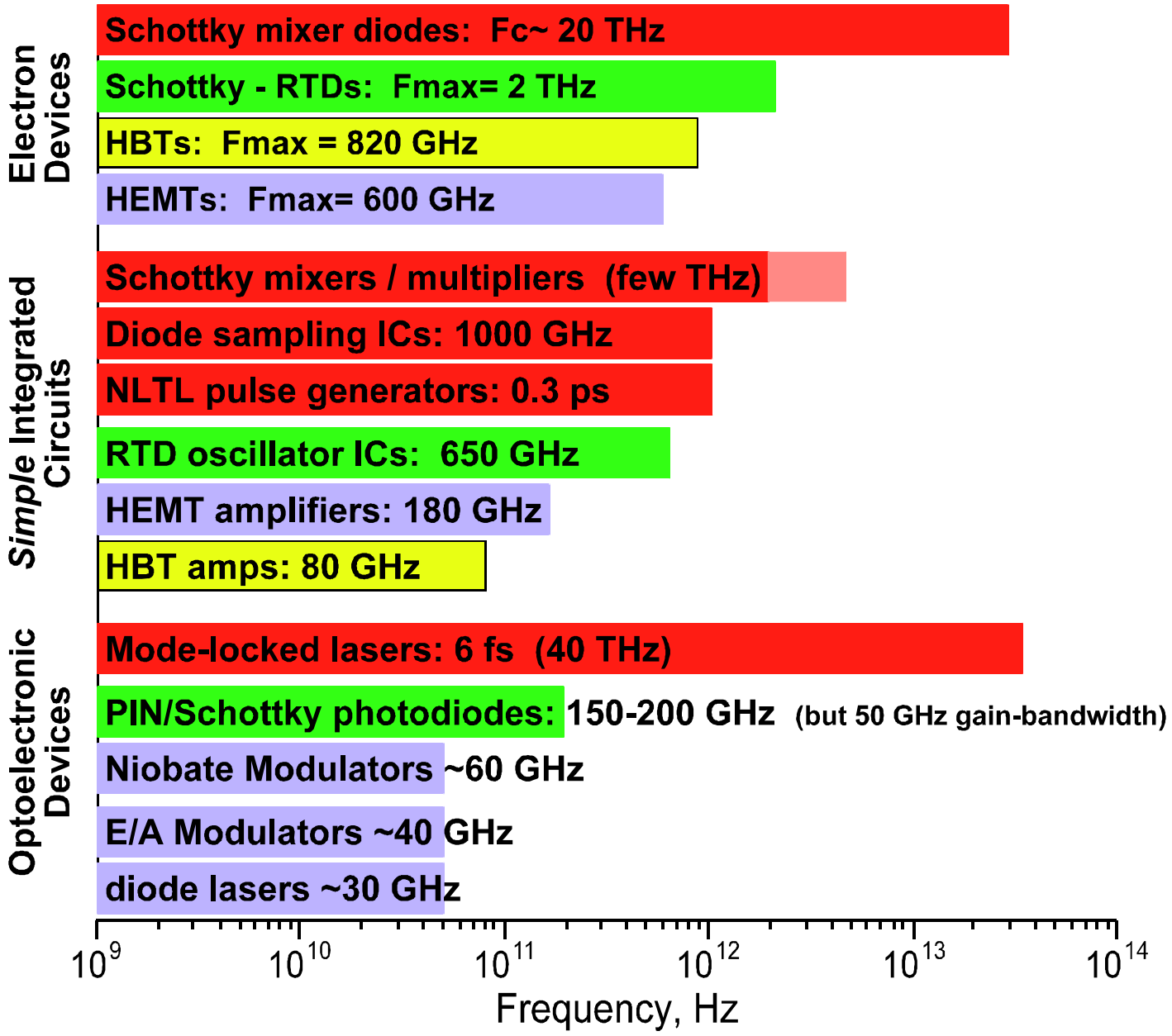
millimeter-wave bandwidths with analog & digital signals !
microstrip-lines and ground-planes for signal integrity
power delay products and impact of wiring

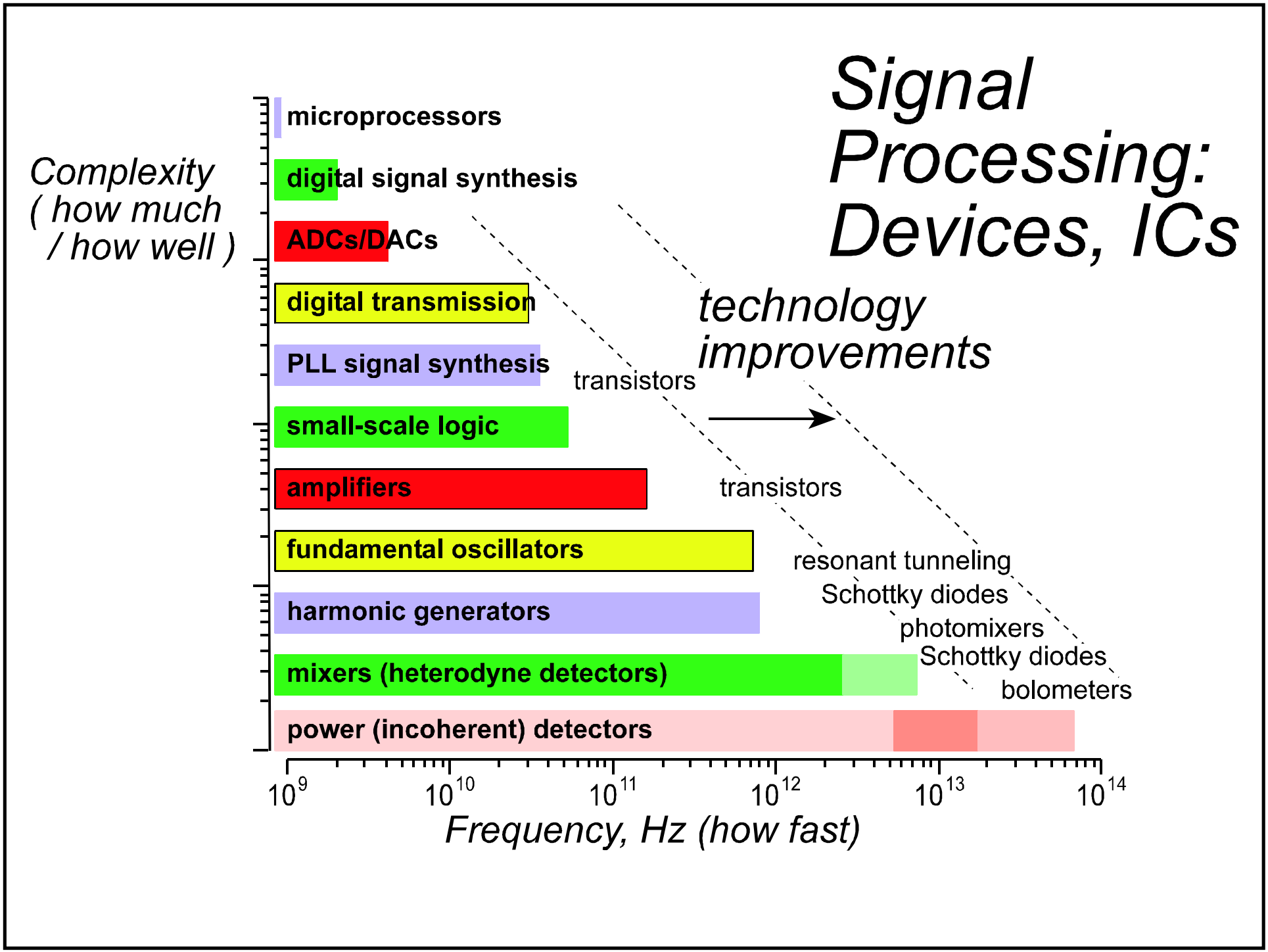
Outstanding heatsinking:

clock rates will be very high, so wiring delays must be small
transistors must be close together !
high performance transistors use high power densities !
power density on die may approach 1 kW/cm^2 !

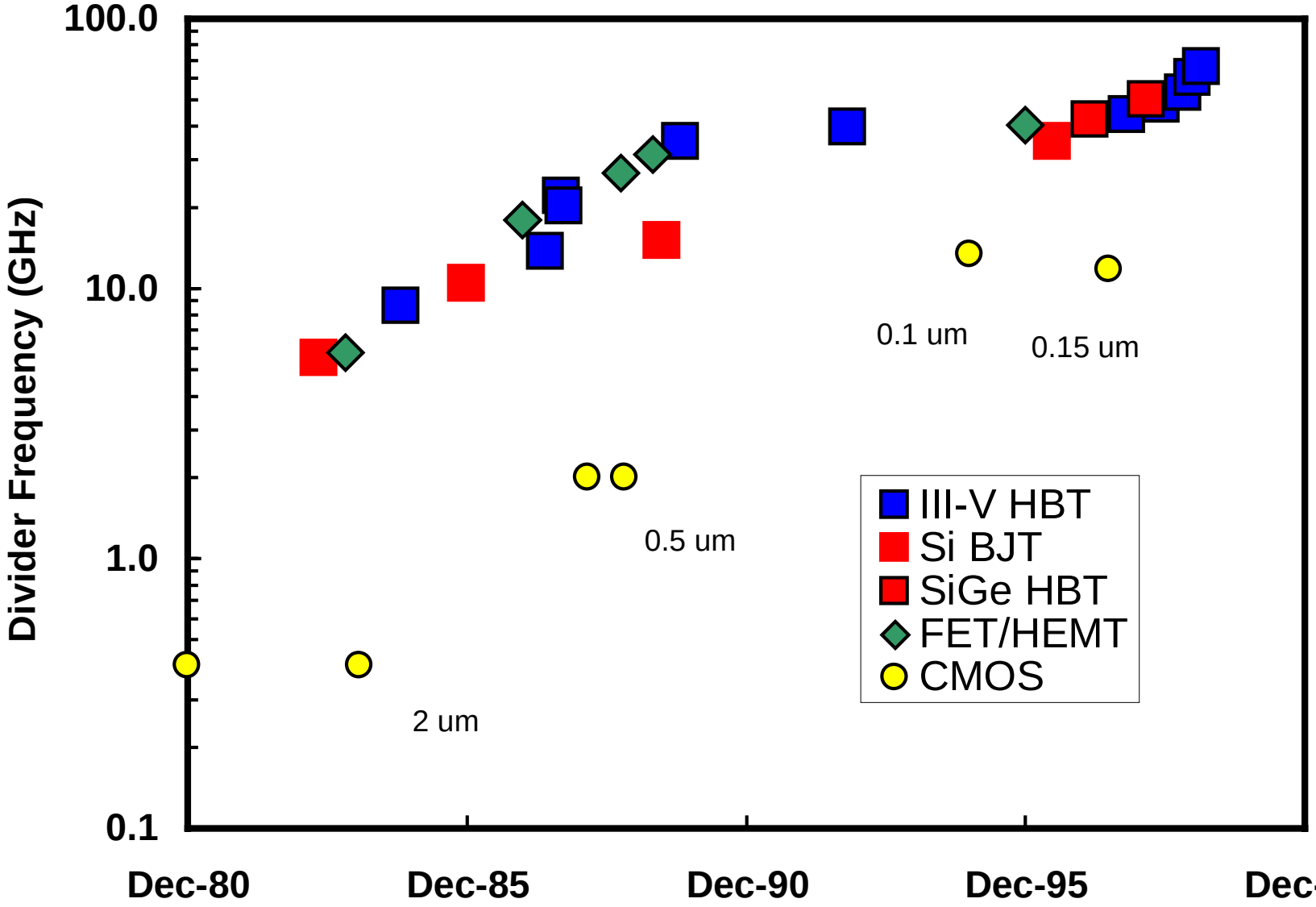
state of the art

Devices and Simple ICs: State of Art, 1999




Signal Processing: Devices, ICs
Complexity (how much / how well)
microprocessors
digital signal synthesis
ADCs/DACs
digital transmission
PLL signal synthesis
small-scale logic
amplifiers
fundamental oscillators
harmonic generators
mixers (heterodyne detectors)
power (incoherent) detectors
technology improvements
transistors
transistors
resonant tunneling
Schottky diodes
photomixers
Schottky diodes
bolometers
10^9
10^10
10^11
10^12
10^13
10^14
Frequency, Hz (how fast)

Logic Speed: III-V vs. Silicon

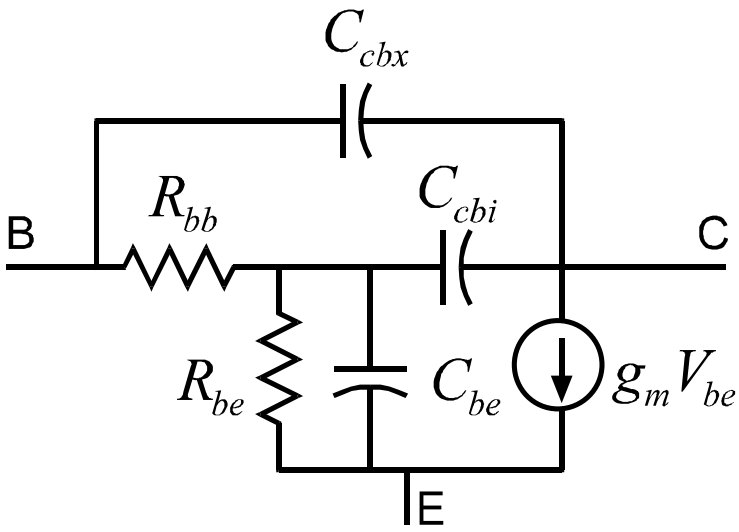


Benchmark: master-slave flip-flop configured as 2:1 static frequency divider

Source: M Sokolich, HRL. CMOS Data from Rodwell, UCSB

HBT performance

Bandwidth of Bipolar Transistors



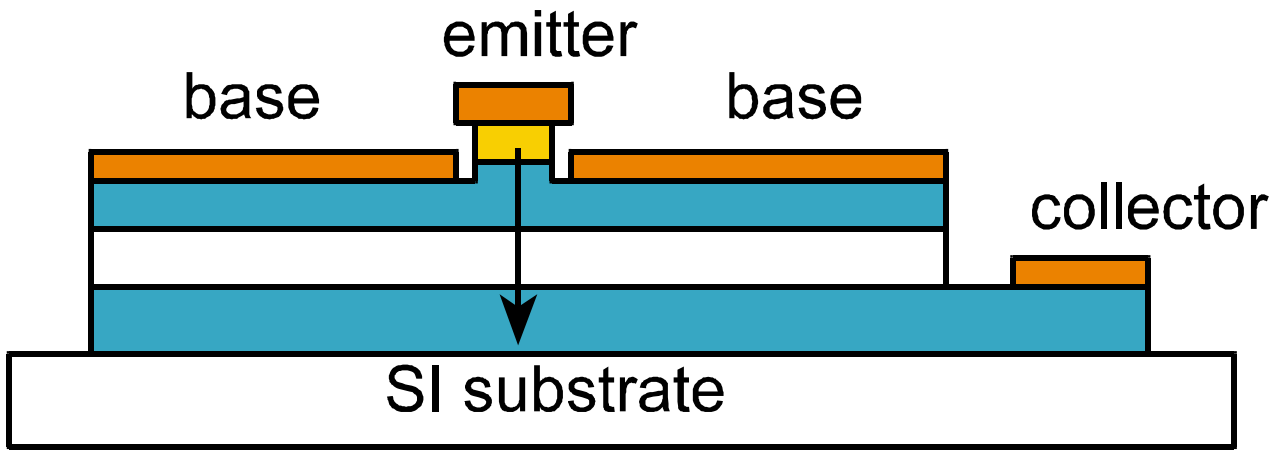
$$f_\tau = \frac{(1/2\pi)}{\tau_{base} + \tau_{collector} + (C_{je} kT/qI_e)}$$

$$f_{max} = \sqrt{\frac{f_\tau}{8\pi R_{bb} C_{cbi}}}$$

f_τ , f_{max} , and C_{cbx} are all important for high - speed circuits

$R_{bb}C_{cbi}$ and $R_{bb}C_{cbx}$ must be reduced

Current-gain cutoff frequency in HBTs



$$\frac{1}{2\pi f_\tau} = \tau_{base} + \tau_{collector} + C_{je}\frac{kT}{qI_E} + C_{bc}\left(\frac{kT}{qI_E} + R_{ex} + R_{coll}\right)$$

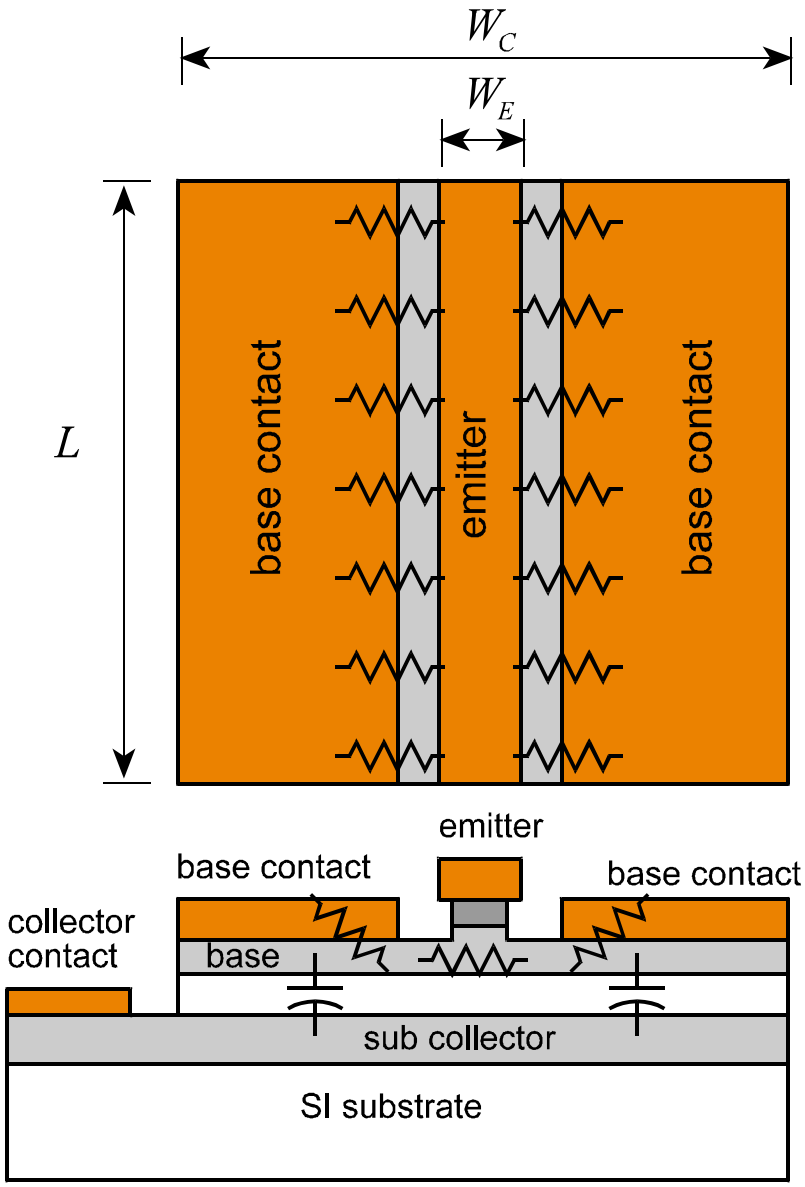
$$\tau_{base} \approx T_b^2 \big/ 2D_n \qquad \tau_{collector} \approx T_c \big/ 2v_{sat}$$

Collector velocities can be high: velocity overshoot in InGaAs

Base bandgap grading reduces transit time substantially

RC terms quite important for > 200 GHz ft devices

Fmax in Double-Mesa HBTs



$$R_{bb} = \frac{1}{2L}\rho_{contact,horizontal} + \frac{\rho_{sheet}}{12L}W_E$$

$$C_{cb} = \frac{\varepsilon L}{T_c}W_c$$

Scaling emitter width does reduce base spreading resistance.

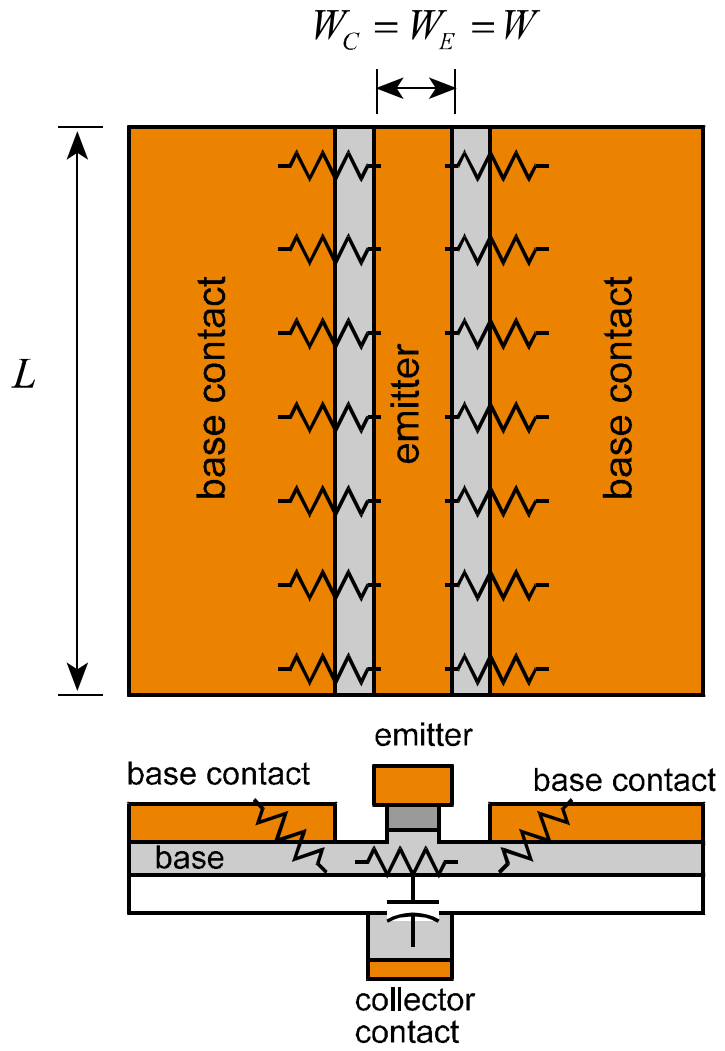
– but –

Minimum base resitance set by base contact resistance.

Minimum collector capacitance set by minimum base contact size

transferred-substrate HBTs

Fmax in Transferred-Substrate HBTs



$$R_{bb} = \frac{1}{2L}\rho_{contact,horizontal} + \frac{\rho_{sheet}}{12L}W$$

$$C_{cb} = \frac{\varepsilon L}{T_c}W$$

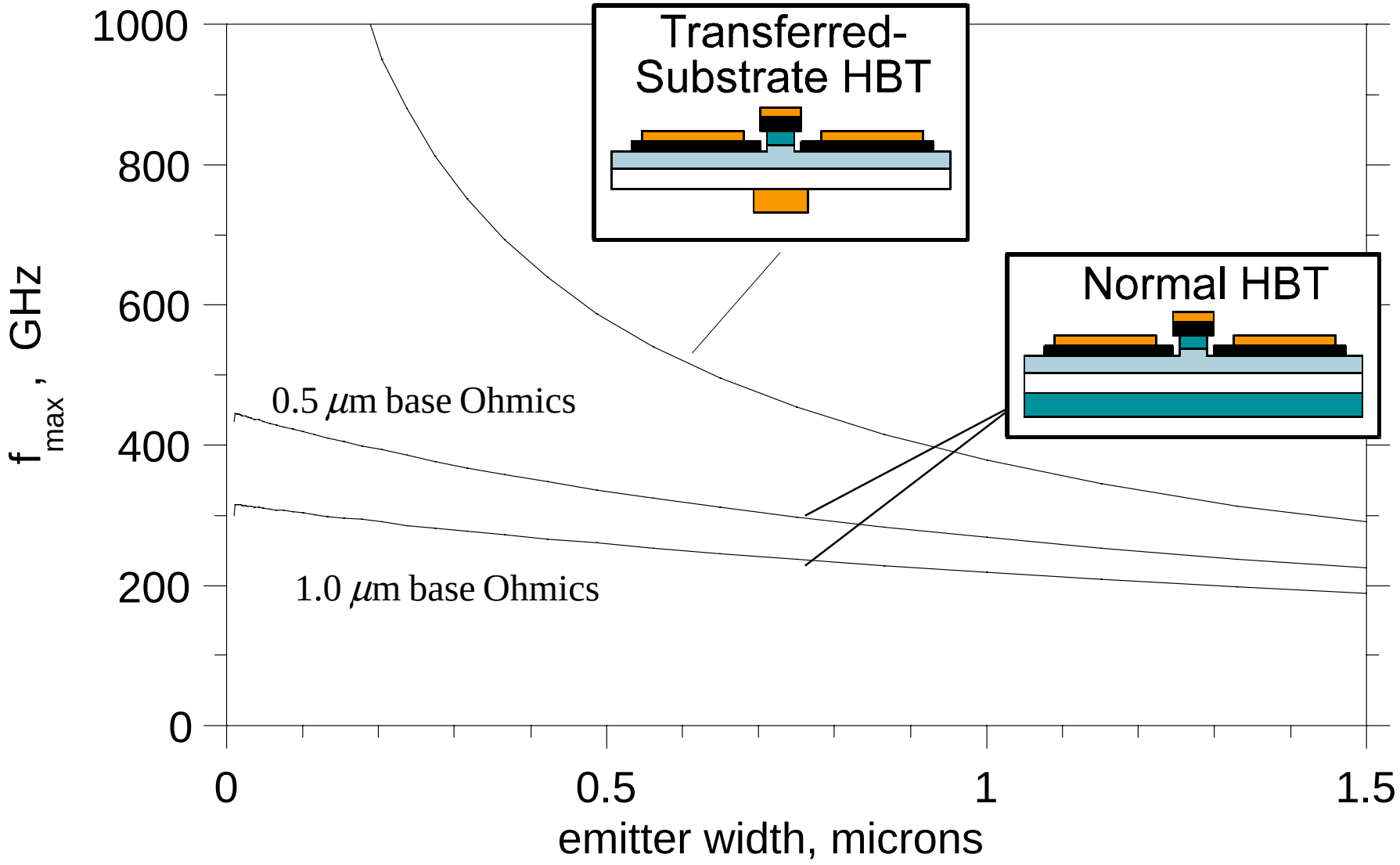
$R_{bb}C_{cb}$ reduces rapidly with deep submicron scaling

Component due to contacts scales as W^1

Base spreading component scales as W^2

F_{max} increases rapidly with deep submicron scaling

Transferred-Substrate HBTs: A ***Scalable*** HBT Technology



- Collector capacitance reduces with scaling: $C_{cb} \propto W_e$
- Bandwidth increases rapidly with scaling: $f_{\max} \propto \sqrt{1/W_e}$

Transferred Substrate HBT Process

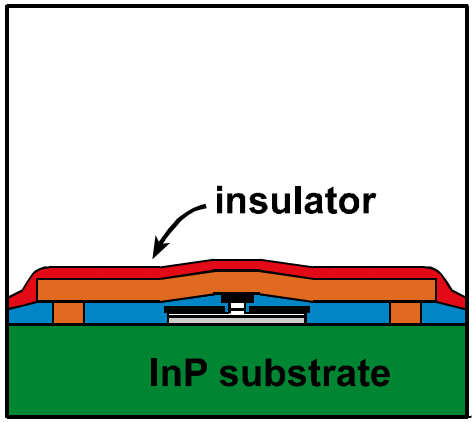
Objectives:

- 1000 GHz transistor bandwidth
- Thermal management for high power density
- Low wiring & packaging parasitics at 100+ GHz

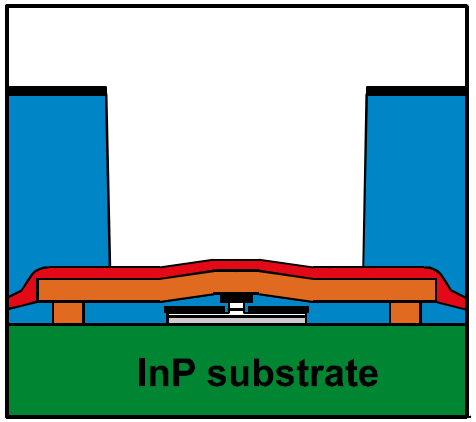
Approach:

- BCB process: standard IC materials
- Metal substrate, thermal vias
- Microstrip wiring: ground vias backside ground plane ε_r=2.7: low capacitance

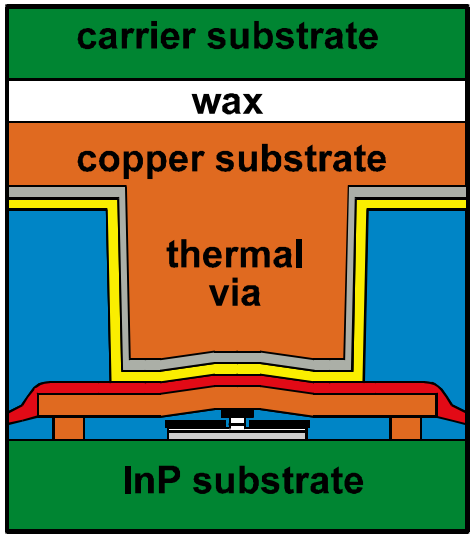
1) Normal emitter, base processes. Deposit silicon nitride insulator.



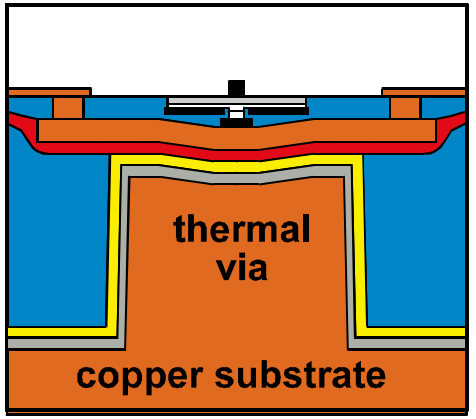
2) Coat with BCB polymer. Etch vias.



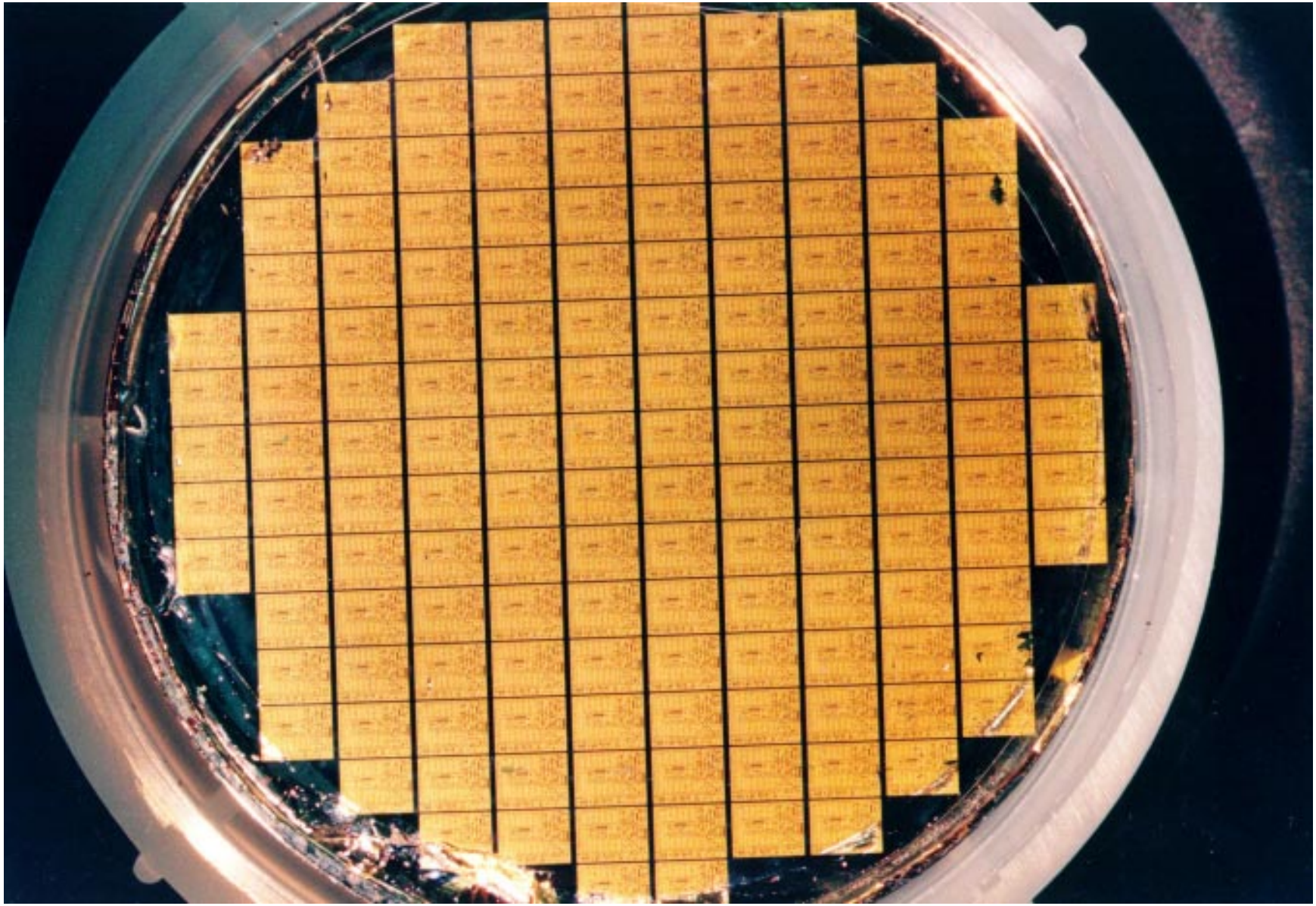
3) Electroplate with Au/Ni/Cu. Wax to carrier substrate.



4) Invert wafer. Remove InP substrate. Deposit collector. Demount from wax.

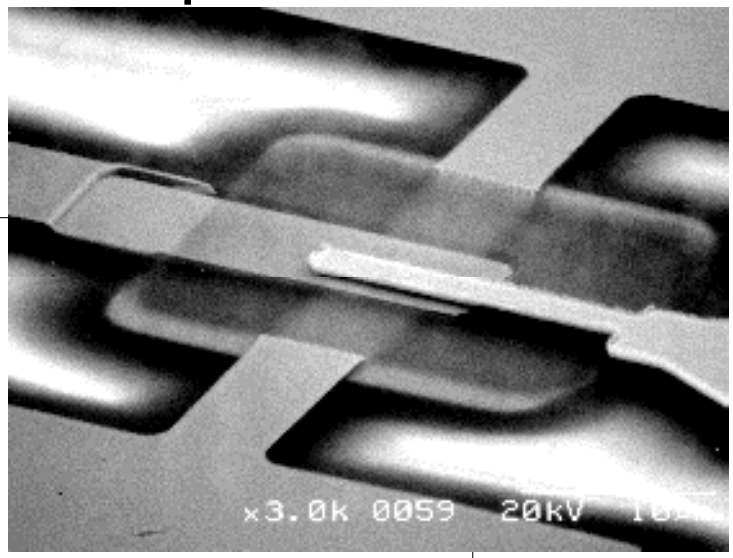


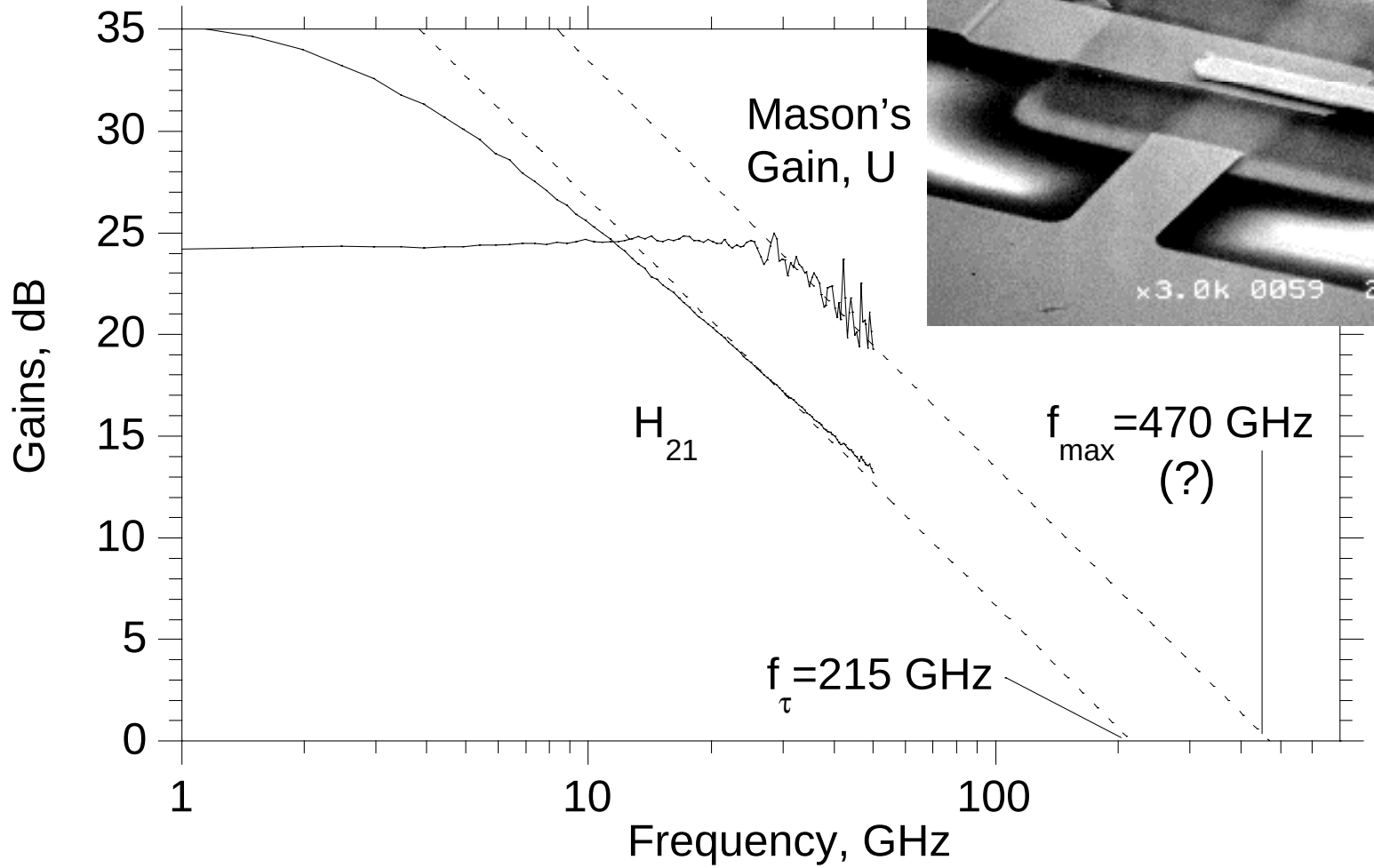
Transfer of Entire 2” HBT MMIC Wafer



Transferred-Substrate Heterojunction Bipolar Transistor

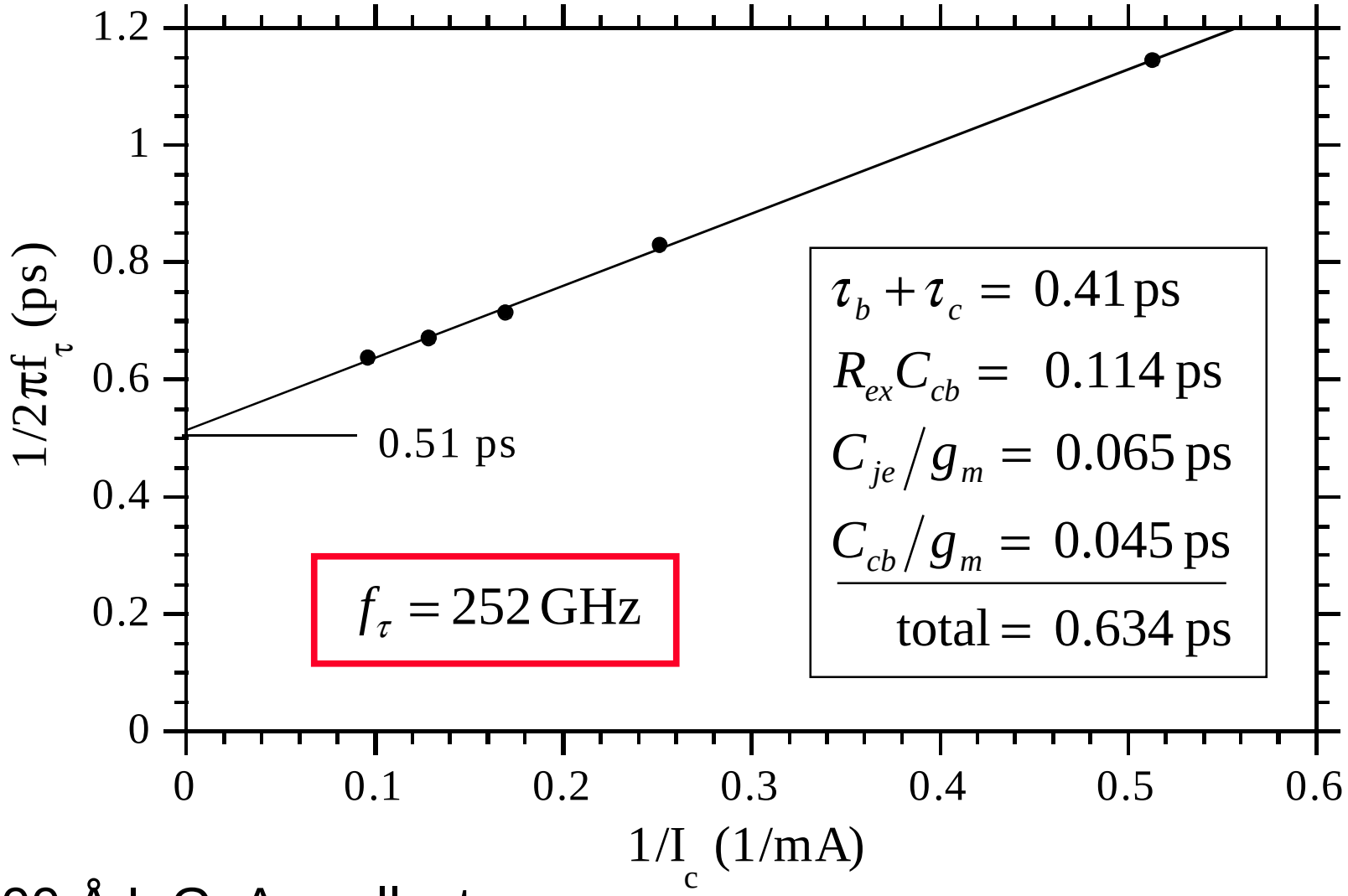
Device with 0.6 μm emitter & 1.8 μm collector
extrapolated fmax at instrument limits, >400 GHz





0.25 μm devices should obtain ~1000 GHz fmax

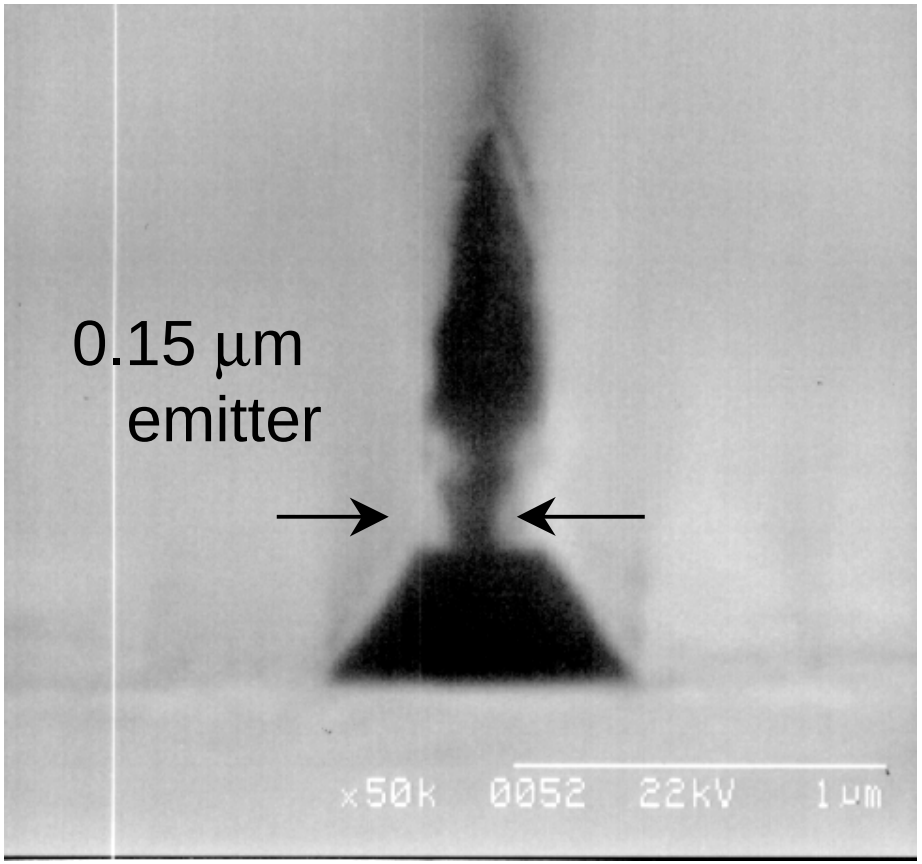
Transit times: HBT with 2kT base grading



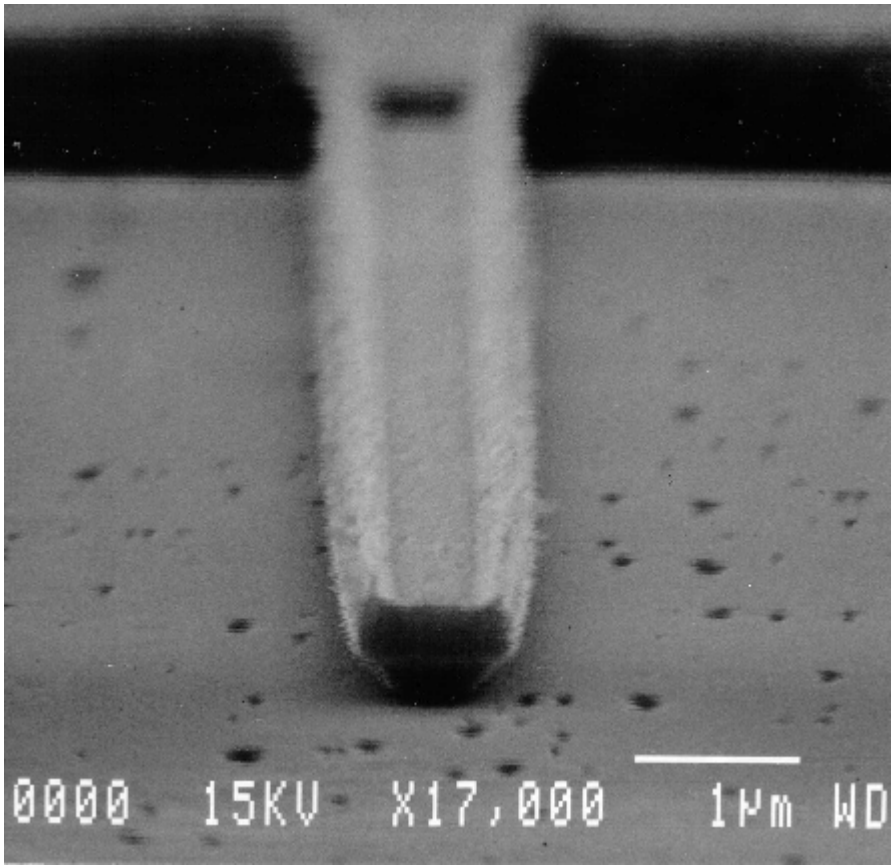
2000 Å InGaAs collector

400 Å InGaAs base, 2kT bandgap grading

SEM Photomicrographs of Deep-submicron HBTs

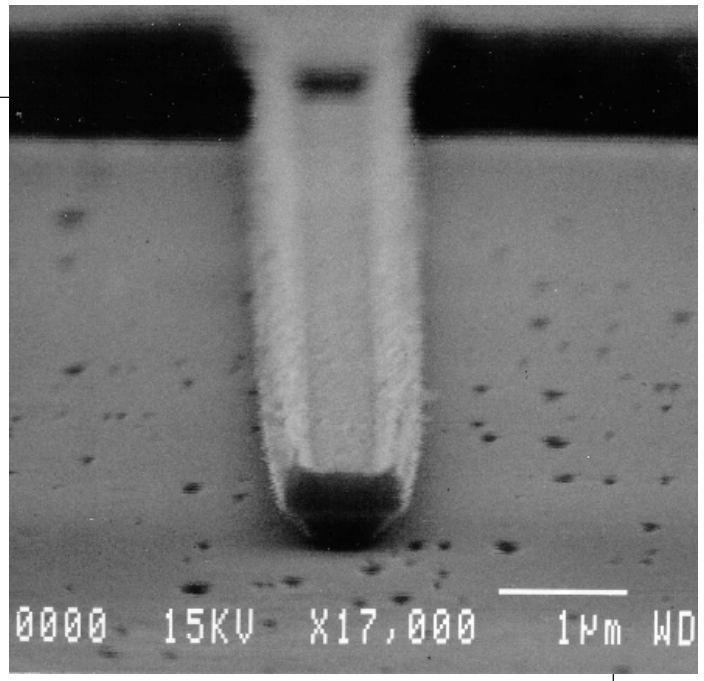


0.15 μm emitter base junction



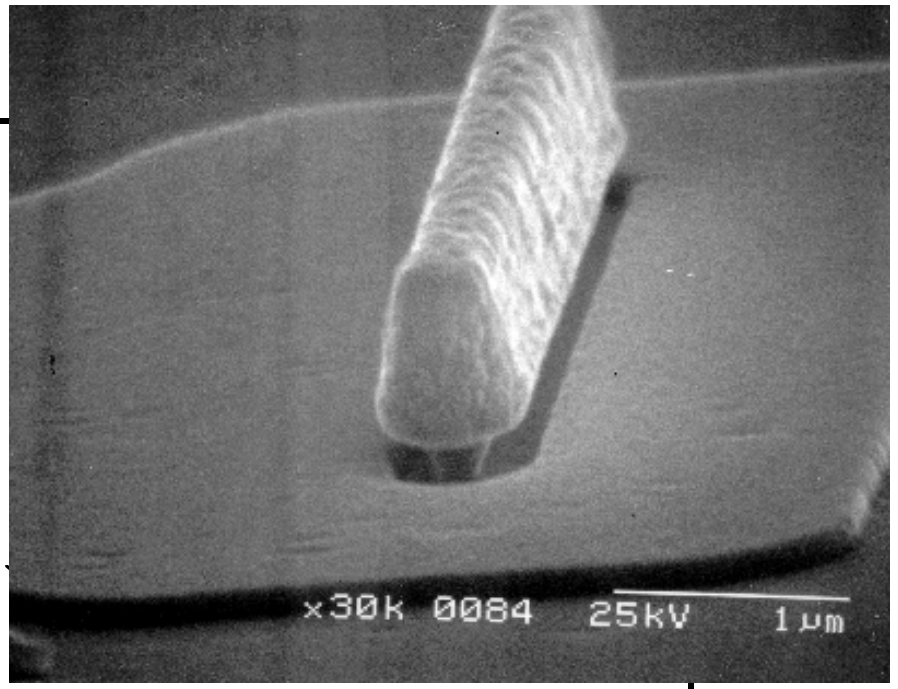
0.4 μm collector

Submicron Transferred-Substrate HBT



0.4 μm x 6 μm emitter, 0.4 μm x 10 μm collector

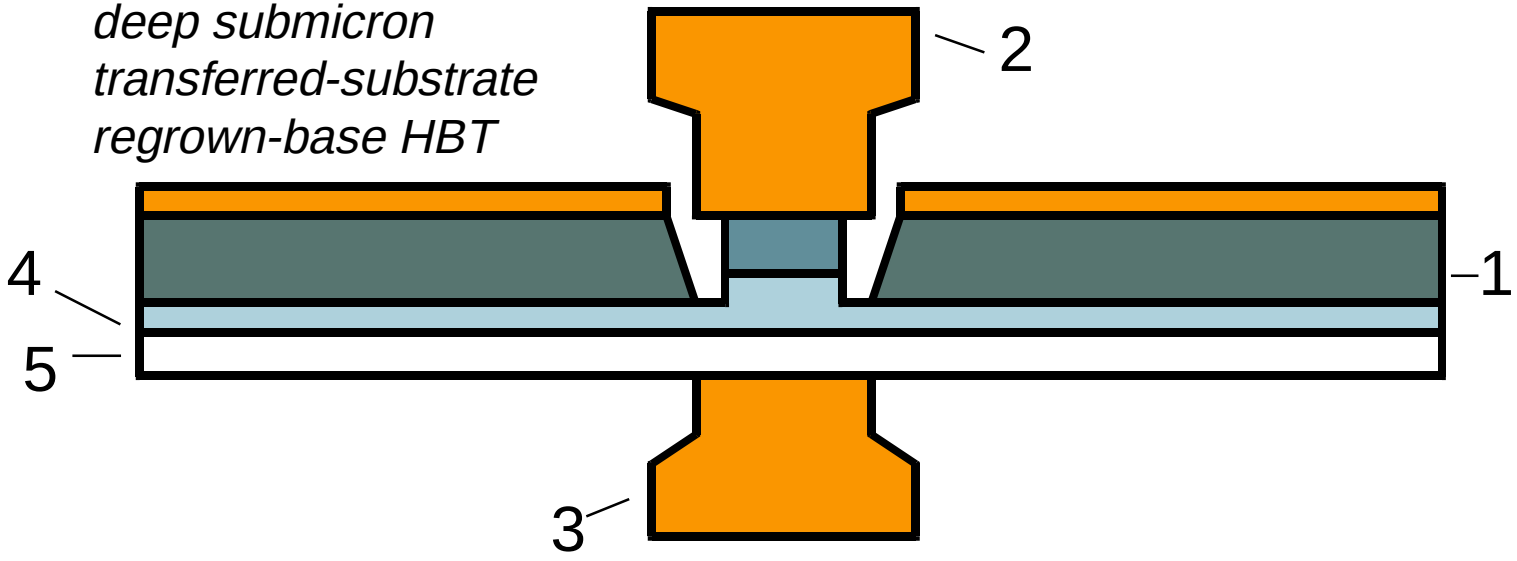
Transferred-Substrate HBT: Stepper Lithography



0.4 μm emitter, ~0.7 μm collector

Proposed THz-Bandwidth HBT ?

deep submicron
transferred-substrate
regrown-base HBT



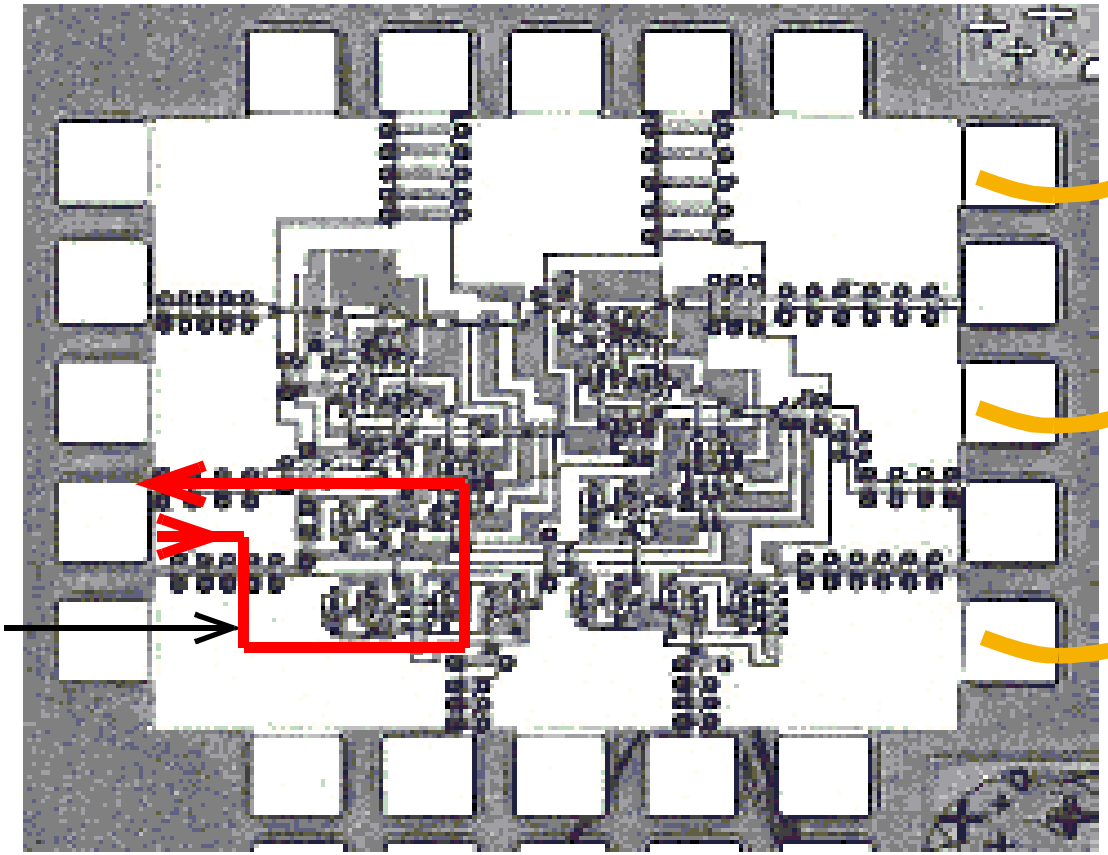
1) regrown P+++ InGaAs extrinsic base --> ultra-low-resistance
2) 0.05 µm wide emitter --> ultra low base spreading resistance
3) 0.05 µm wide collector --> ultra low collector capacitance
4) 100 Å, carbon-doped graded base --> 0.05 ps transit time
5) 1kÅ thick InP collector --> 0.1 ps transit time.

Projected Performance:

Transistor with 500 GHz ft, 1500 GHz fmax

The wiring environment for 100 GHz ICs

Why is Improved Wiring Essential?

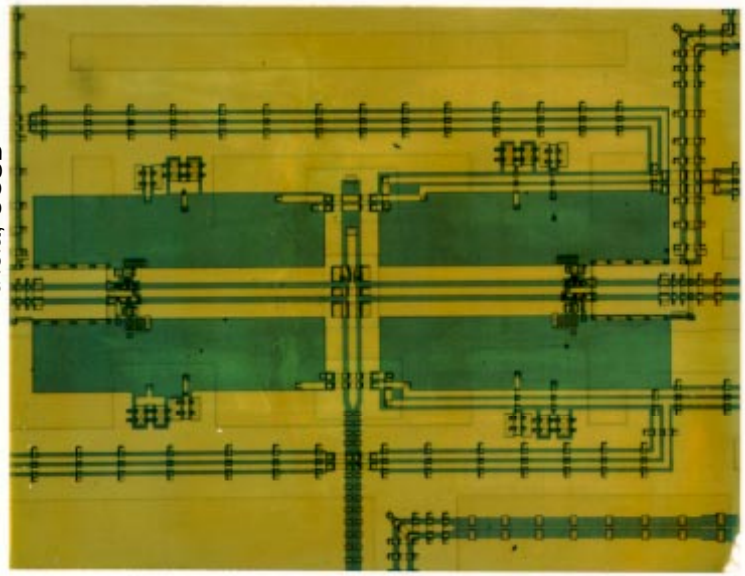


30 GHz M/S D-FF in UCSB - mesa HBT technology

Ground loops & wire bonds:
degrade circuit & packaged IC performance

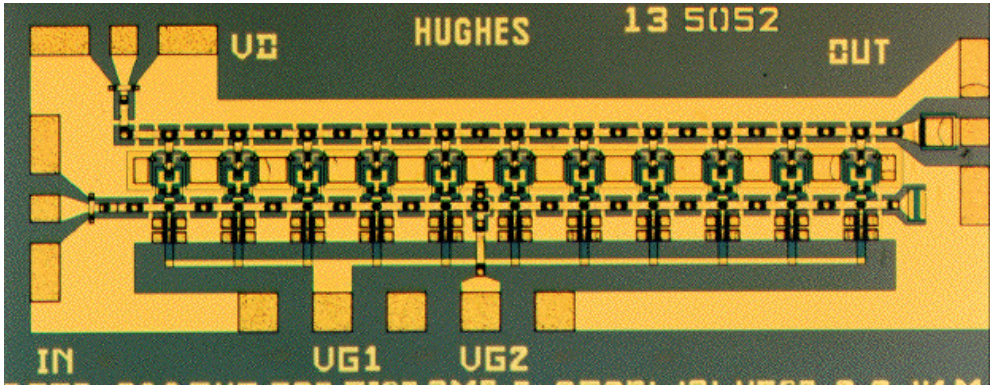
> 100 GHz CPW ICs: *severe crosstalk & ground bounce*

4-channel 100 Gb/s diode-based DMUX



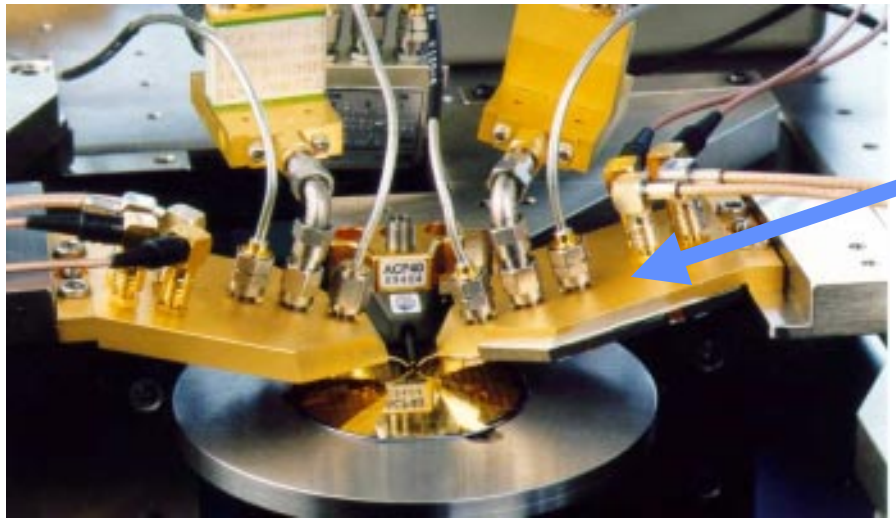
R. Pullela, UCSB

1-180 GHz HEMT amplifier (with HRL)



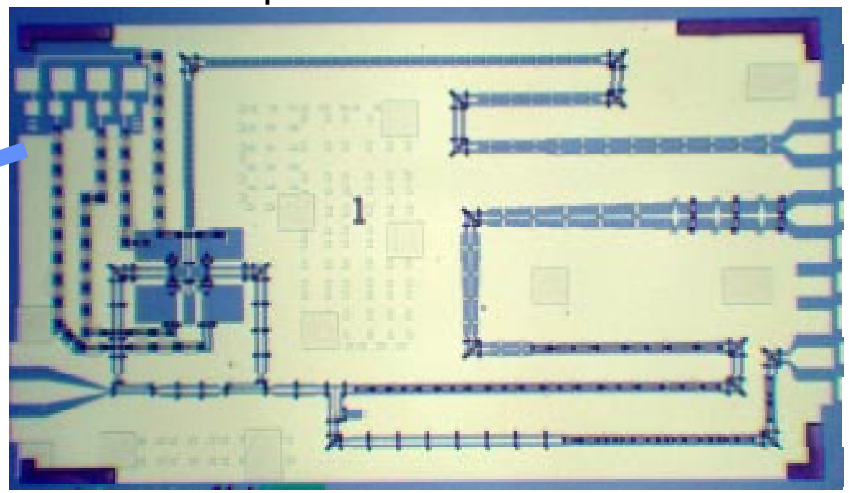
B. Agarwal UCSB, M. Matloubian, HRL

active probes for 70-220 GHz network analysis



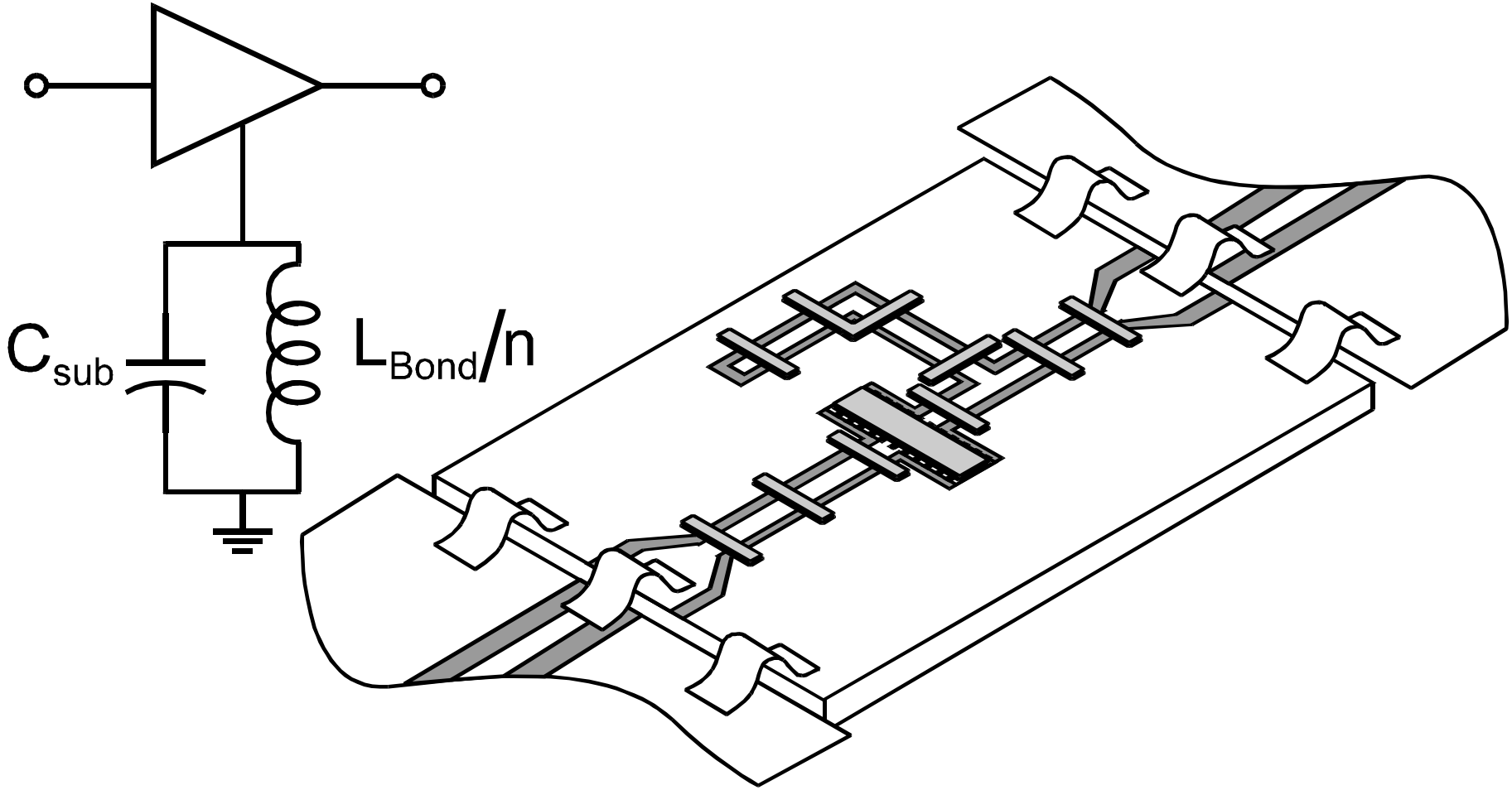
O. Wohlgemuth: Fraunhofer / UCSB

70-220 GHz network analyzer chip for active probe



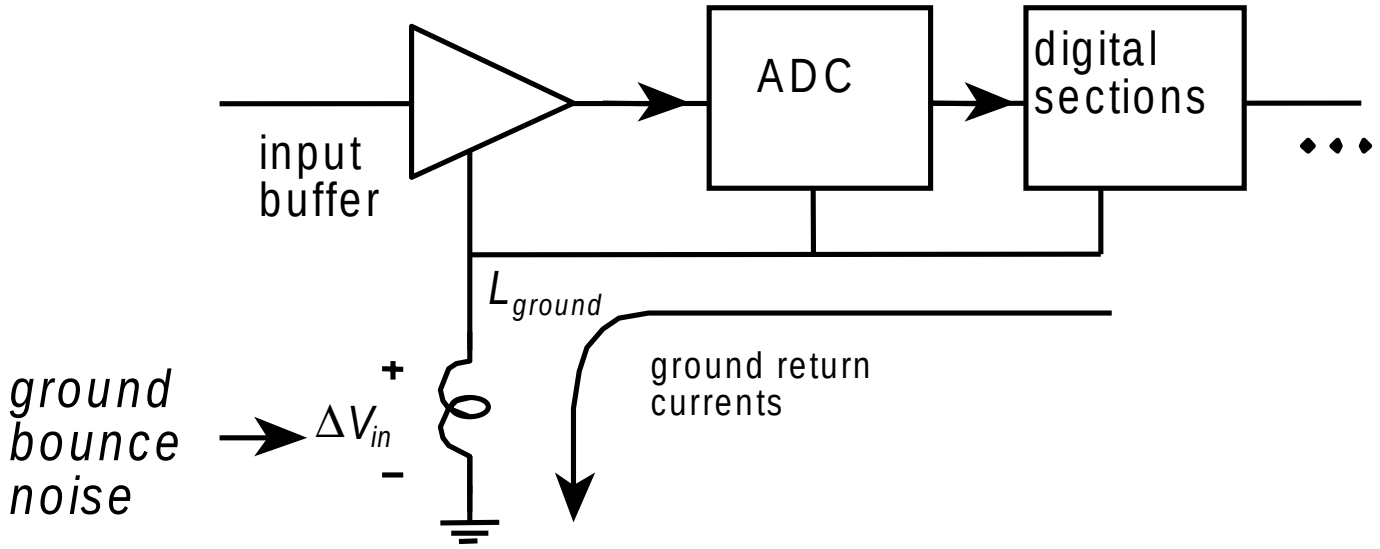
O. Wohlgemuth: Fraunhofer / UCSB

Coplanar Waveguide and Ground-Bounce



Bond wire inductance resonates with through-wafer capacitance at 5-20 GHz

Ground Bound Noise in ADCs



Ground bounce noise must be ~100 dB below full-scale input

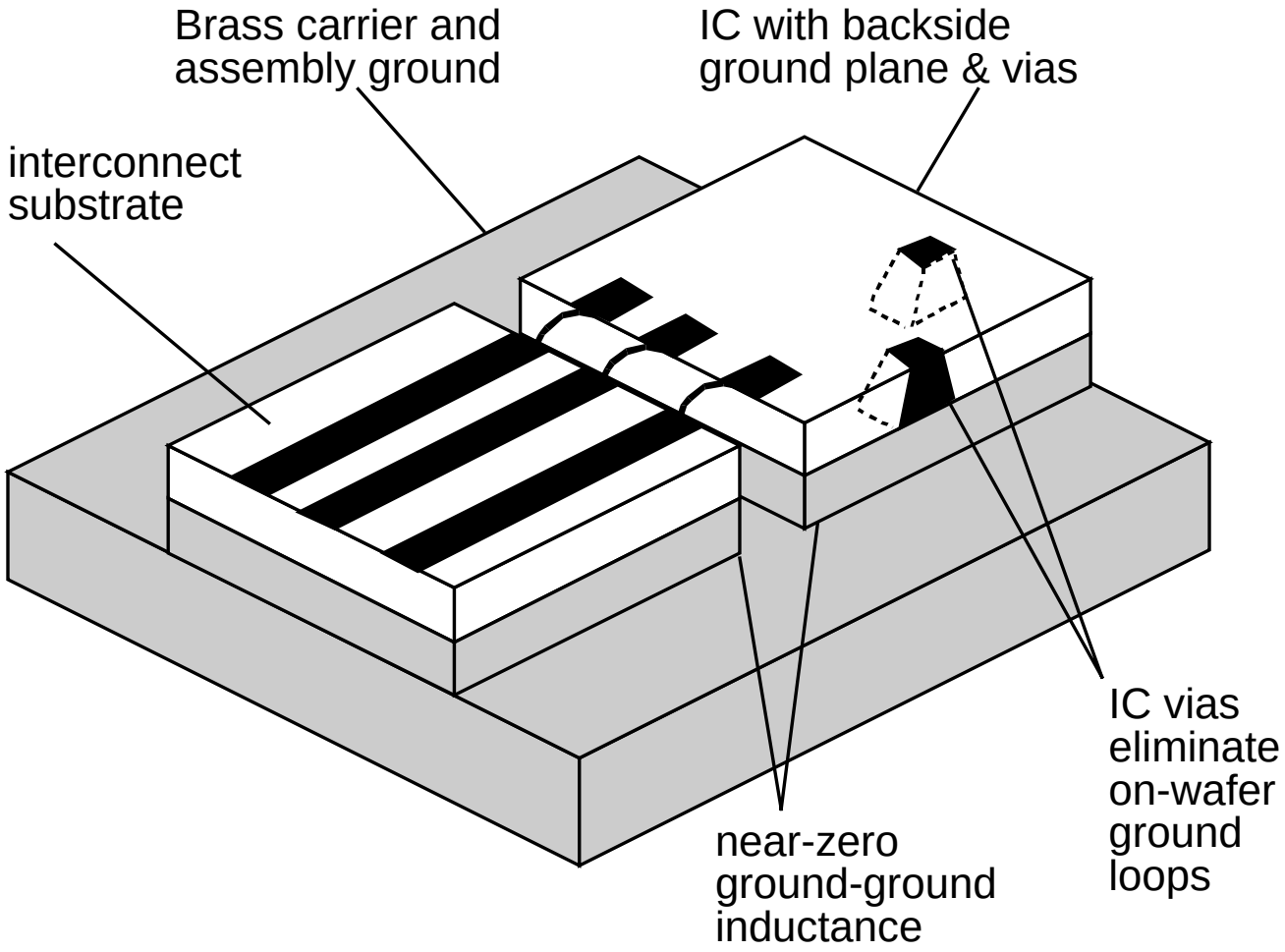
Differential input will partly suppress ground noise coupling

~ 30 to 40 dB common-mode rejection feasible

CMRR insufficient to obtain 100 dB SNR

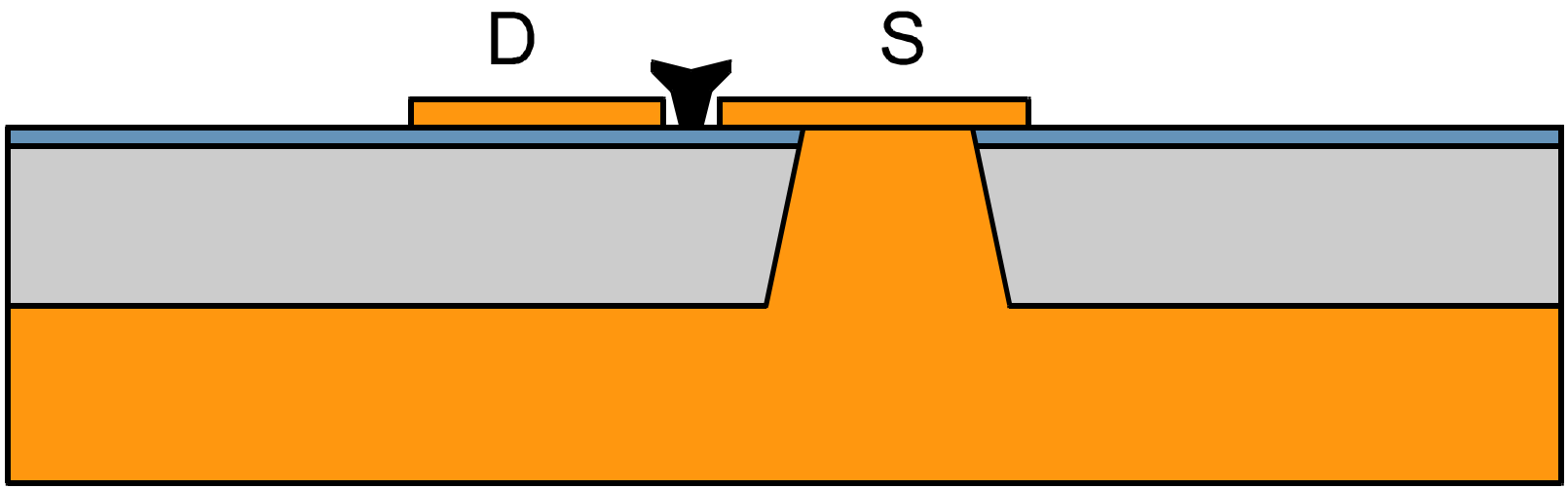
Eliminate ground bounce noise by good IC grounding

Microstrip IC wiring to Eliminate Ground Bounce Noise



Transferred-substrate HBT process provides vias & ground plane.

The microstrip via inductance problem



12 pH via inductance for 100 micron MIMIC substrate

j7.5 Ohms at 100 GHz, j15 Ohms at 200 GHz

A formidable difficulty for > 100 GHz IC design

At 100 um substrate thickness, via spacing must be > 100 um

Solutions include “masterslice”, flip-chip, substrate transfer

Standard MMIC Microstrip / Via Process

Objectives:

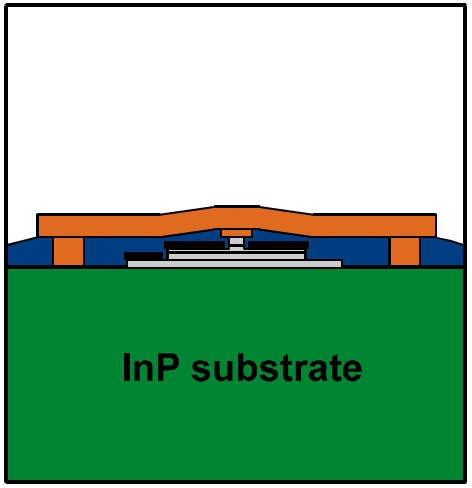
ground plane
microstrip wiring
low via inductance
avoid substrate modes

Approach:

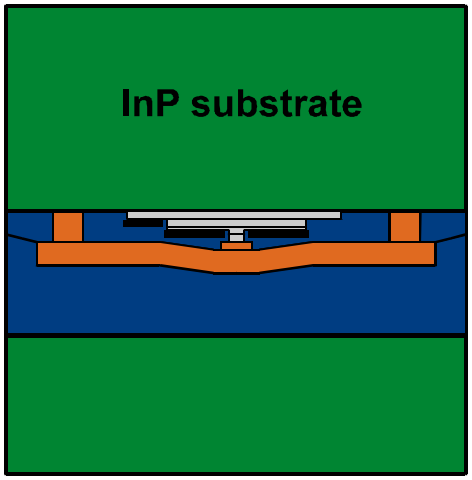
the industry standard
frontside processing
wax mounting
wafer lapping
backside metal
wafer release

Limitations:

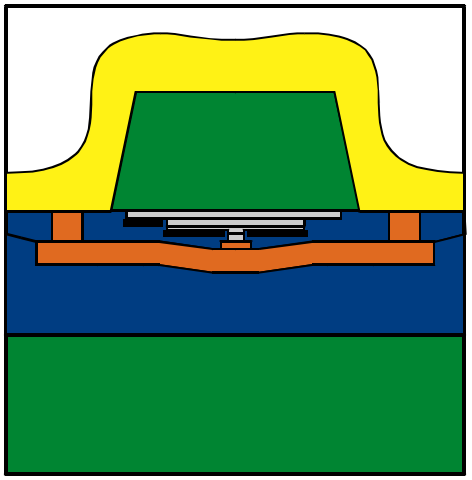
for 180 GHz must lap to 35 μm



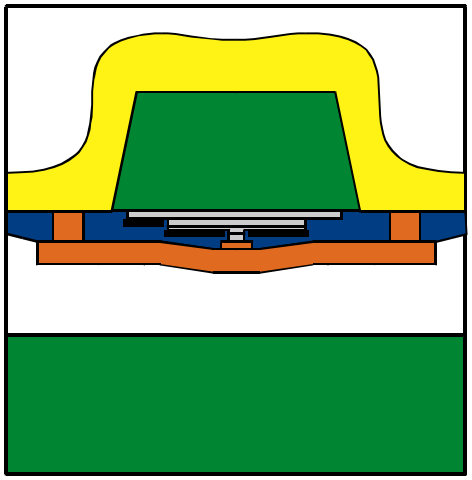
1) Process complete HBT's passives, interconnect.



2) Mount HBT wafer to carrier wafer with wax.



3) Back-thin InP, etch and plate vias.

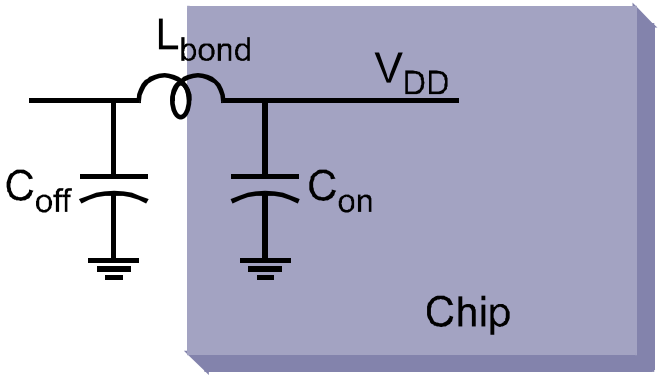


4) Peel thinned wafer off carrier.

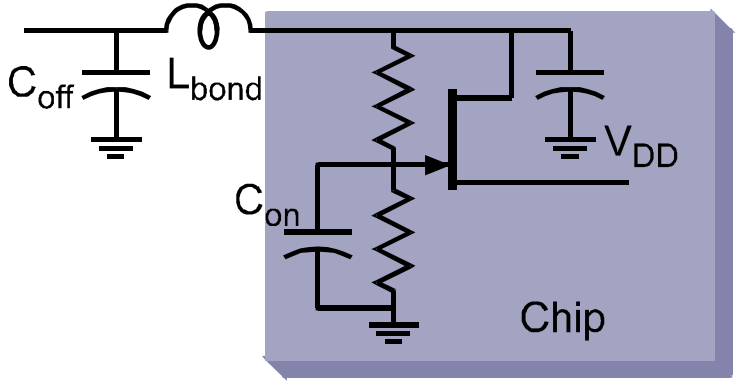
Power Supply Resonance

Resonates at $f = 1/2\pi\sqrt{L_{bond}C_{off}}$

gain peak / suckout, oscillation, etc.



Active (AC) supply regulation

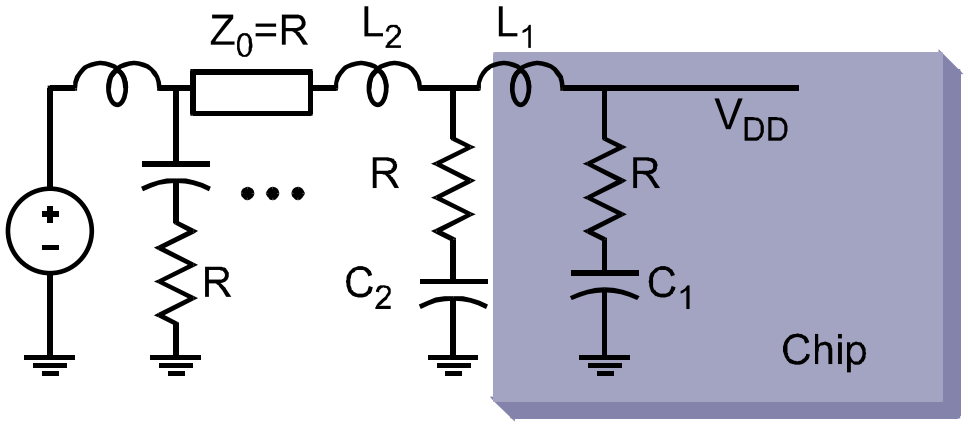


Passive filter synthesis

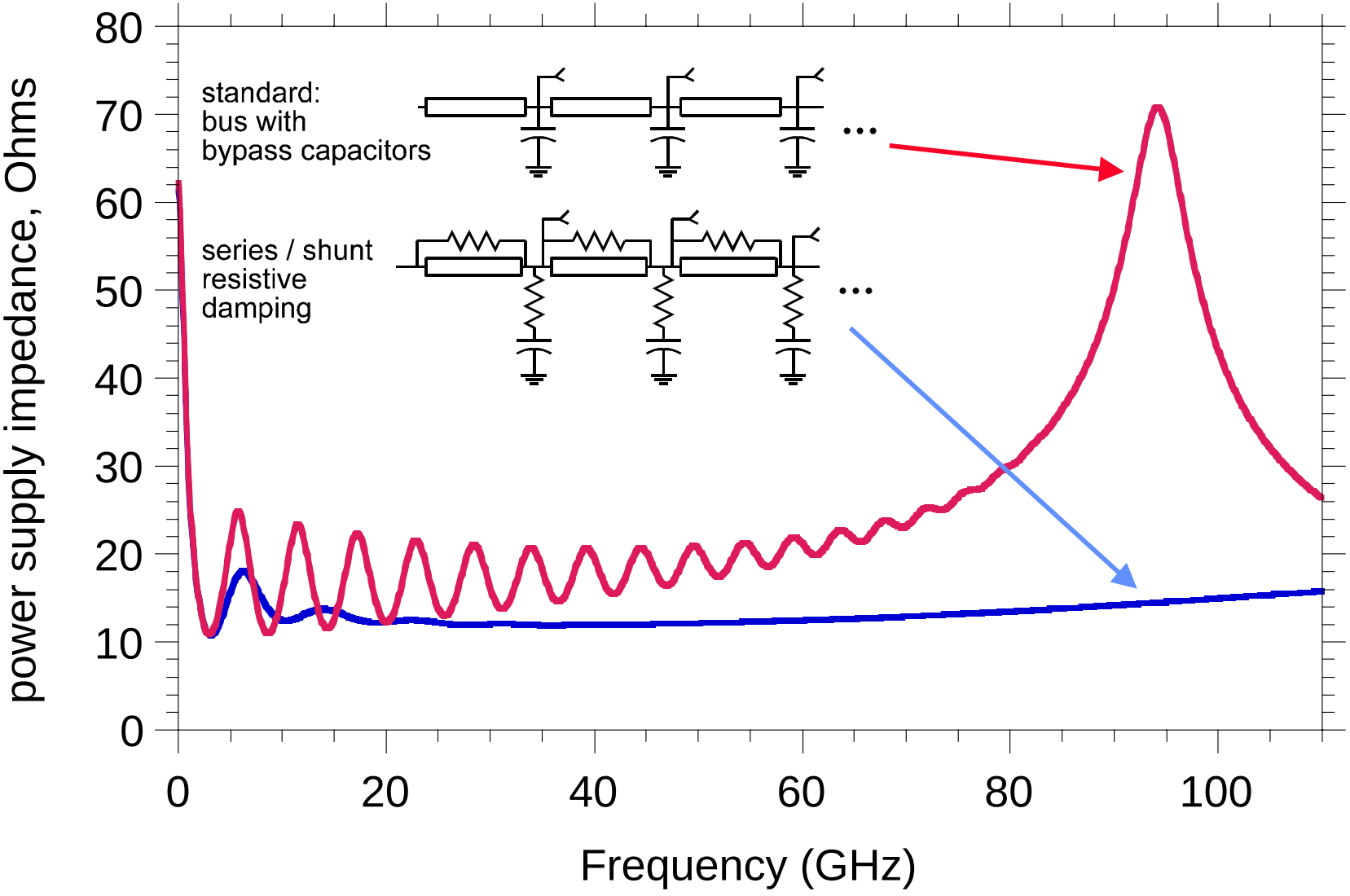
$$R = \sqrt{L_1/C_1}$$

$$\sqrt{L_1/C_1} = \sqrt{L_2/C_2} = \bullet\bullet\bullet$$

supply impedance is R at all frequencies

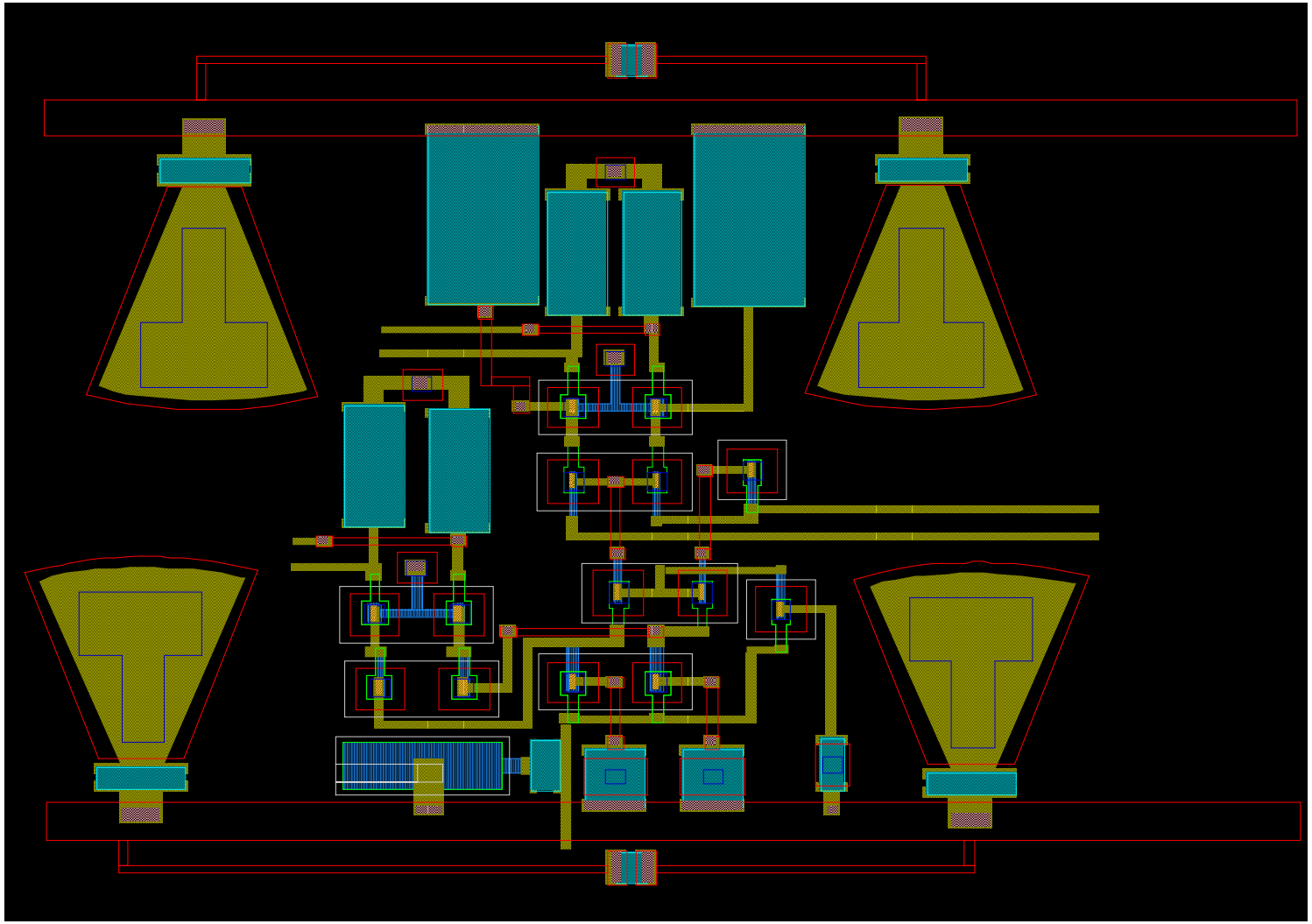


On-wafer power distribution for 100 GHz logic

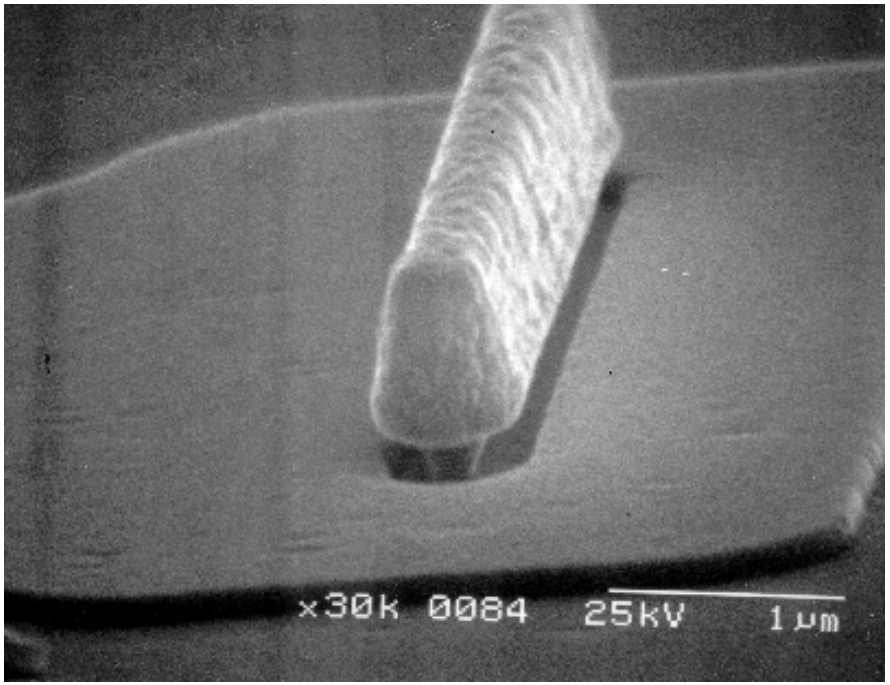


*supply **will** resonate: must prevent during design*

Standard cell showing power busses



Deep submicron HBT logic: ***low power ?***



Device sized for 100 Ω load:
(200 mV ECL logic swing)
0.15 µm x 6 µm emitter
peak speed at 2 mA bias

Shorter stripe length device:
0.15 µm x 0.5 µm emitter
peak speed at 150 µA bias

Small device is low-power but cannot drive 100 Ω line.
drives line with mismatched impedance: capacitance
lower power at higher (wiring-limited) delay

fast low-power logic requires low-voltage-swing-logic

Power-delay product in interconnect limit

$$P_{gate} T_{prop} = (1/2) C_{wire} V_{cc} \Delta V_{\text{logic}}$$

bipolar logic (static power)

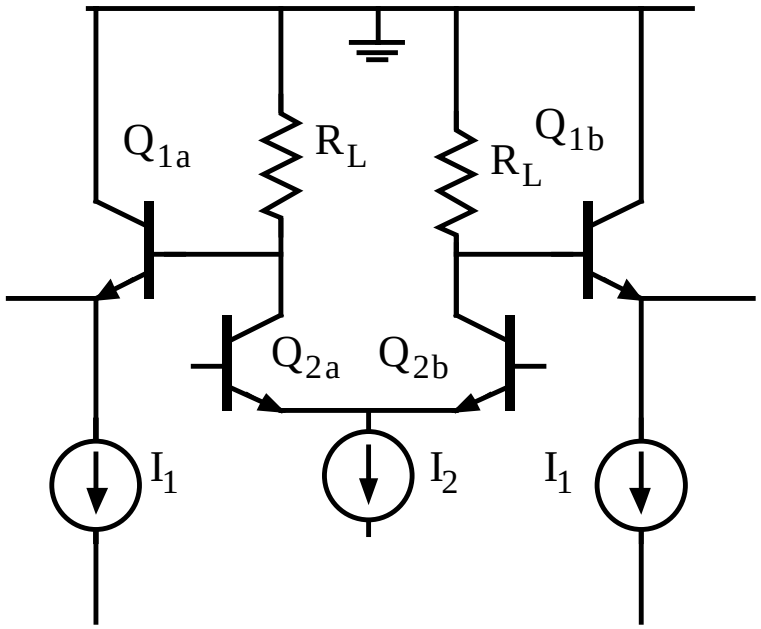
$$P_{gate} / f_{clock} = (1/2) C_{wire} V_{cc} \Delta V_{\text{logic}}$$

CMOS logic (dynamic power)

$(T_{prop} f_{clock})^{-1} \sim$ number gates between latches

For fast, low-power logic: reduce $V_{cc} \Delta V_{\text{logic}}$

The Interconnect Limit and Logic Gate Design



$$A_v = \frac{R_L}{2kT/qI_2} = \frac{I_2 R_L}{2kT/q} = \frac{\Delta V_{\text{logic}}}{2kT/q}$$

Voltage Gain must be >> 1

So: $\Delta V_{\text{logic}} = 10 \bullet (kT/q)$

But: $P_{gate} T_{gate} = (1/2) V_{cc} \Delta V_{\text{logic}} C_{wire}$

$$P_{gate} T_{gate} = (1/2)(1.5 \text{ Volt})(10 \bullet kT/q) C_{wire}$$

(power•delay) is constrained by interconnects

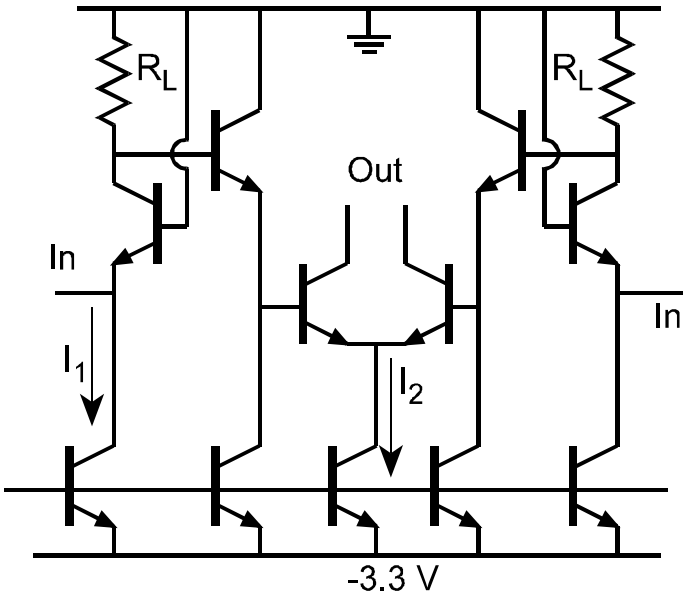
a fast transistor doesn't result in a fast IC

conclusion: a better circuit design is needed

Similar derivation for CMOS (Meindl, Proc IEEE, 1995)

Low-Voltage-Swing Logic Gates

Common-Base-Buffered
Emitter-Coupled Logic



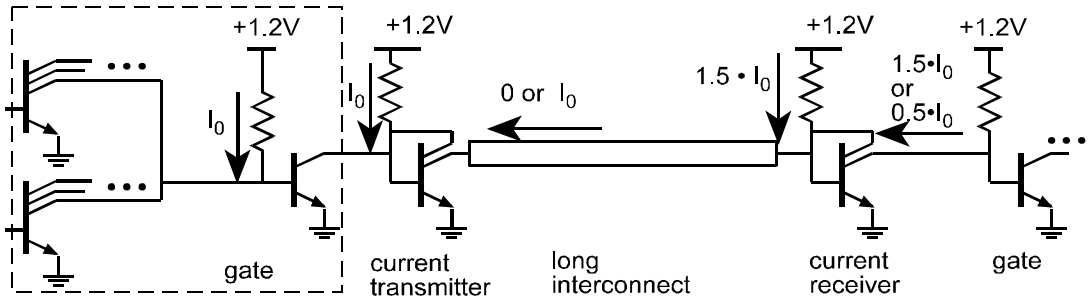
microwave DDS IC effort:
2000 HBTs @ 50-100 GHz clock
dissipation is severe issue

Solution (?):
small HBTs + low-voltage logic

Principle:
low-impedance input current buffer

Challenge:
not increasing transistor count

Current-Mirror-Buffered
Integated-Injection Logic



Common Feature:

$$\Delta V_{\text{logic}} = \frac{kT}{q} \ln\left(1 + \frac{I_{switched}}{I_{bias}}\right)$$

Power Density in 100 GHz logic

Transistors tightly packed to minimize wire delays

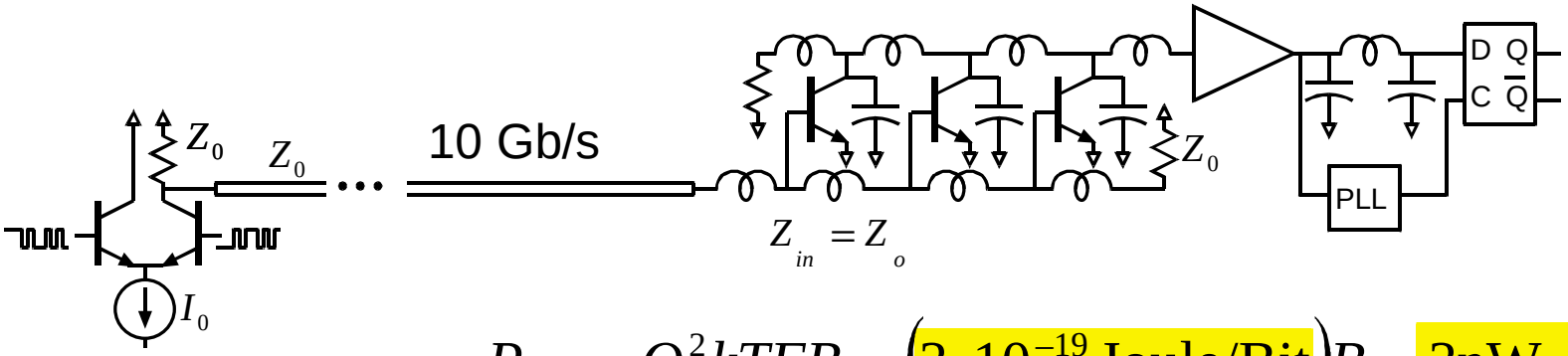
10^5 W/cm^2 HBT junction power density.

~10^3 W/cm^2 power density on-chip

--> 75 C temperature rise in 500 μm substrate.

Solutions:
thin substrate to < 100 μm
replace semiconductor with metal

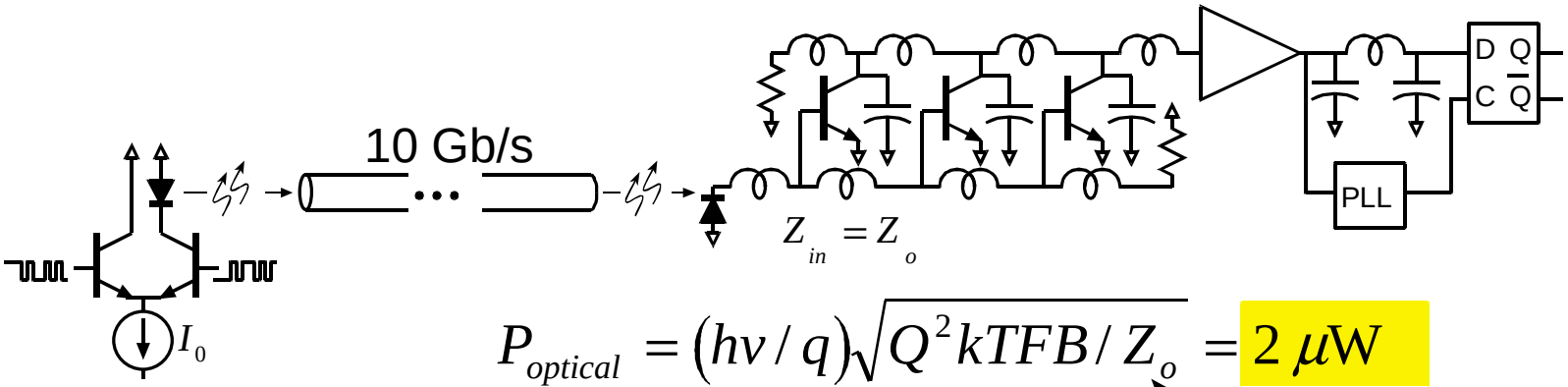
Optical vs Electrical Interconnects in Thermal Noise Limit



$$P_{\min} = Q^2 kTFB = \left(3 \cdot 10^{-19}\ \text{Joule/Bit}\right) B = 3\text{nW}$$

$Q^2 = 36$ Binary Antipodal Modulation,

$Q^2 = \ln(2)$, Shannon's limit

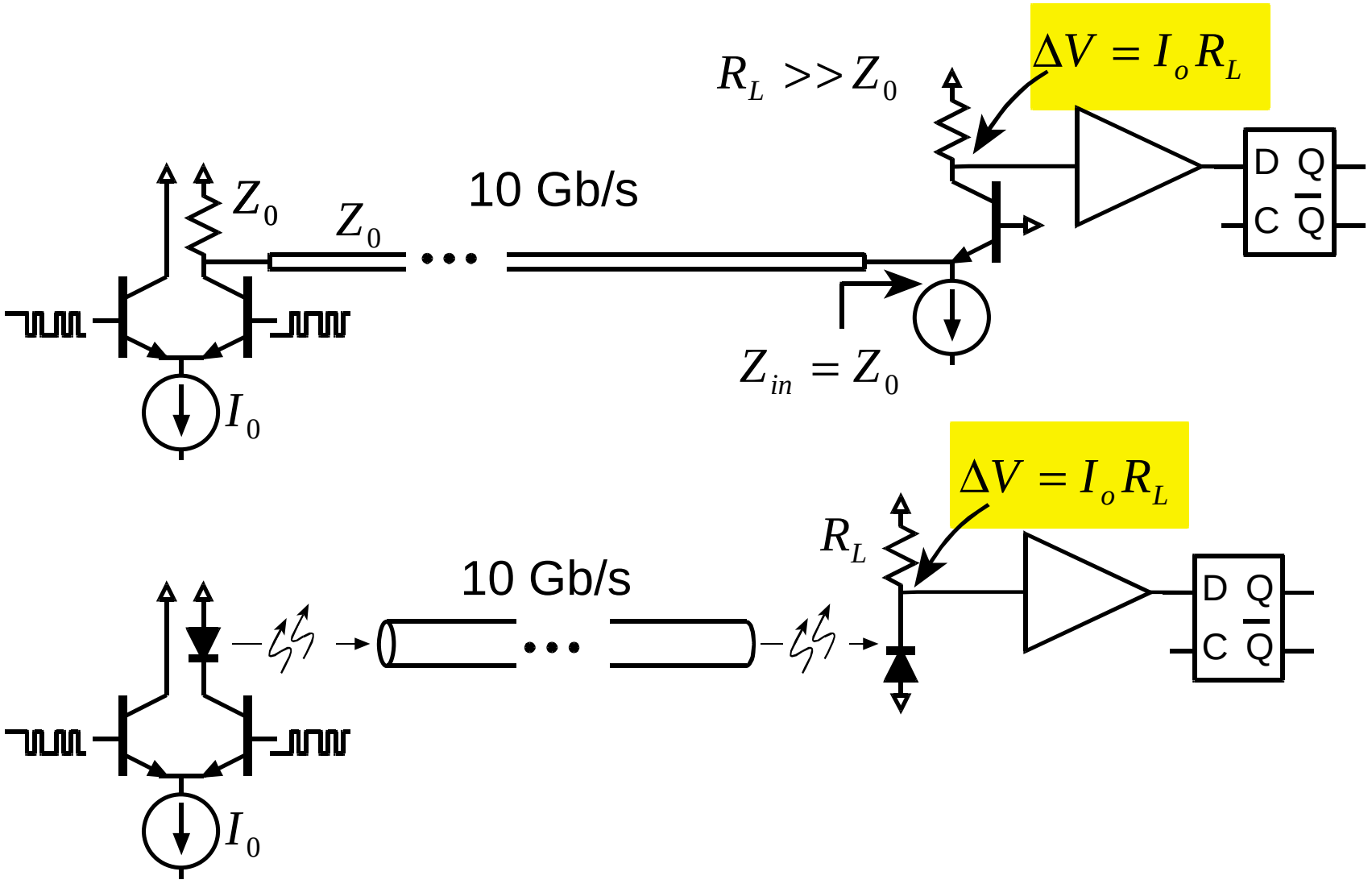


$$P_{optical} = (h\nu / q)\sqrt{Q^2 kTFB / Z_o} = 2\ \mu\text{W}$$

$Z_0 = 500\ \Omega$

Optical receivers are much less sensitive (square law!)

Optical vs. Electrical Interconnects: Minimum Signal Amplitude (EMI Tolerance) Limit



Required currents are similar...

So why use optical interconnects ?

Optical fibers are cheap

microwave cables, connectors, are expensive

but lasers, modulators, detectors must be made cheap

Optical fibers have very low loss

microwave cables have high skin effect losses

but lasers, modulators have coupling loss

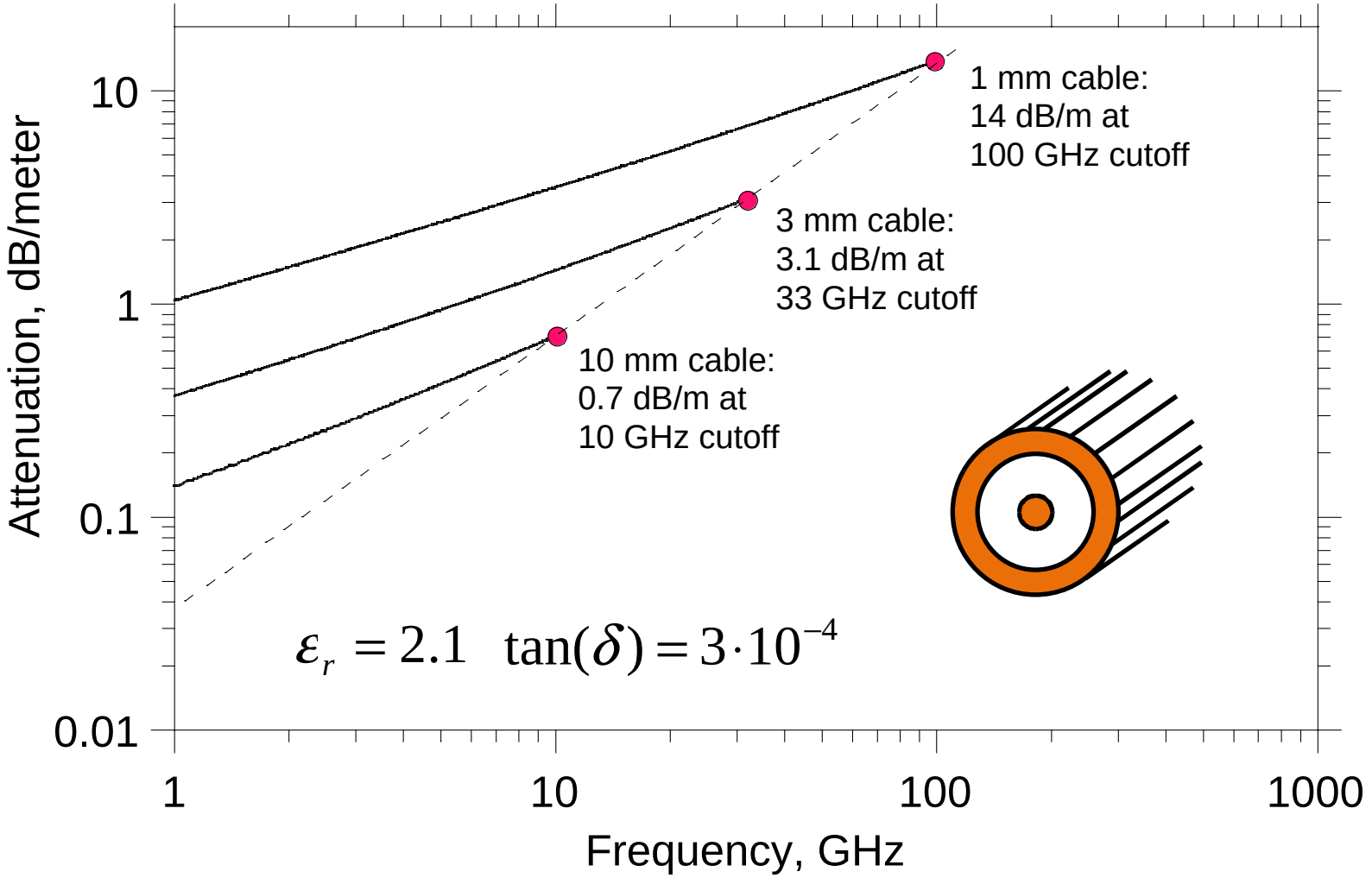
Optical fibers are compact

thin electrical conductors have very high losses

multi-pin packages must use thin, lossy, conductors

Fiber optics is advantageous
because optical fibers have very low attenuation

Loss of Coaxial Cable



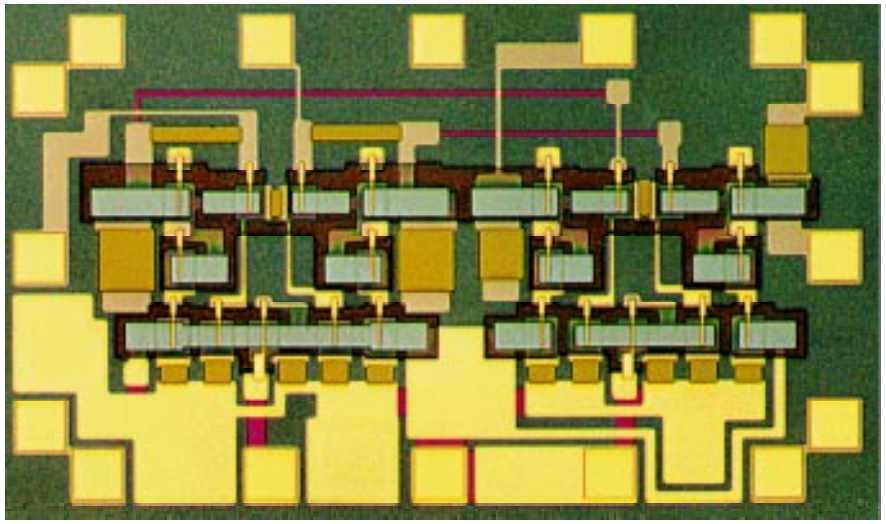
Single-mode propagation requires $f \le c \cdot (2/\pi)\varepsilon_r^{-1/2}\left(D_{inner} + D_{outer}\right)^{-1}$

Skin loss $\alpha_{skin} \propto f^{1/2} / D_{inner} \longrightarrow$ Loss $\alpha_{skin} \propto f^{3/2}$

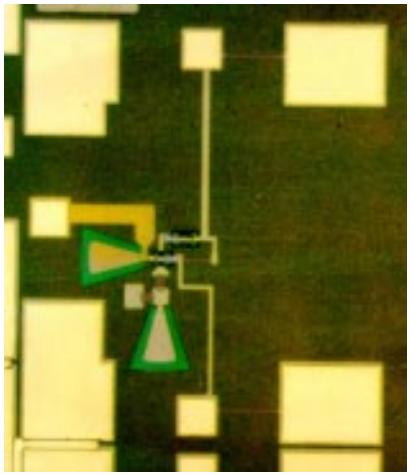
circuit results: transferred-substrate technology

Transferred-Substrate HBT Integrated Circuits

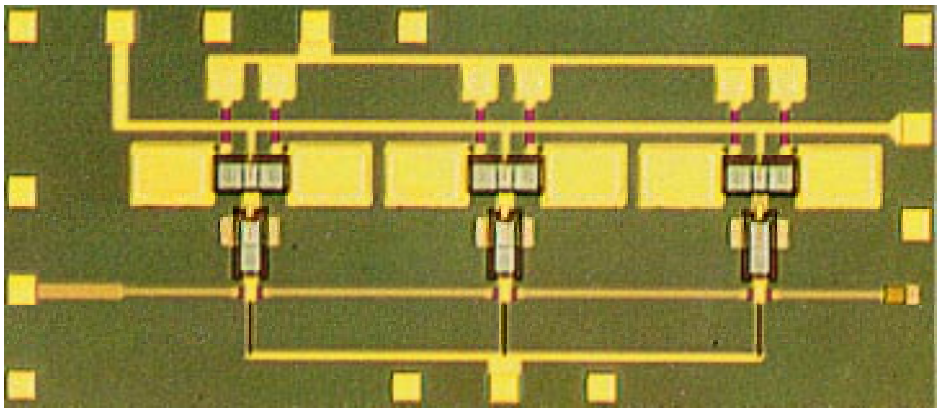
11 dB, 50+ GHz AGC / limiting amplifier



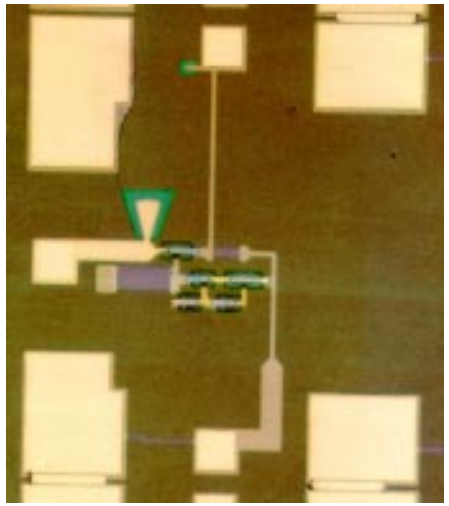
16 dB, DC-60 GHz amplifier



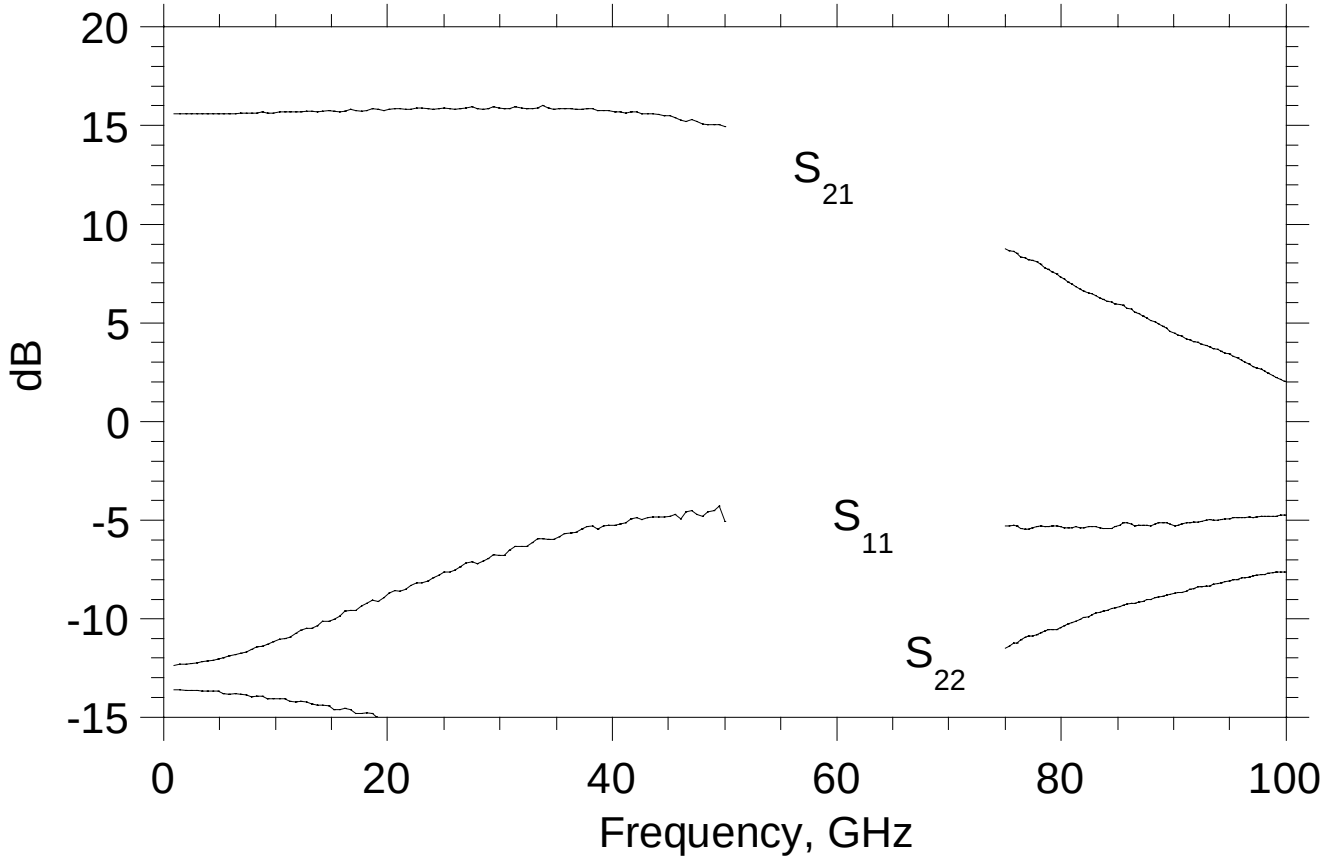
7 dB, 5-80 GHz distributed amplifier

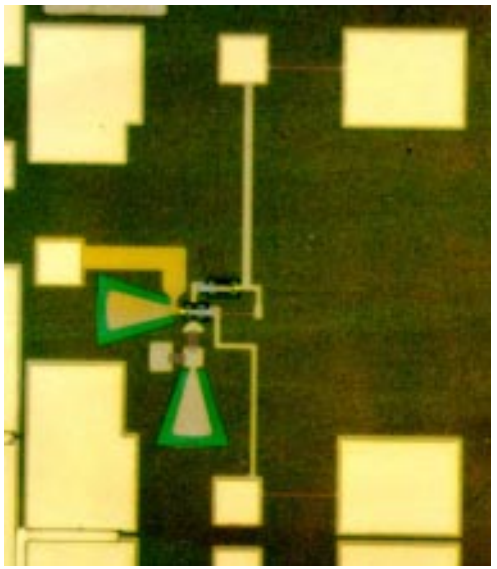


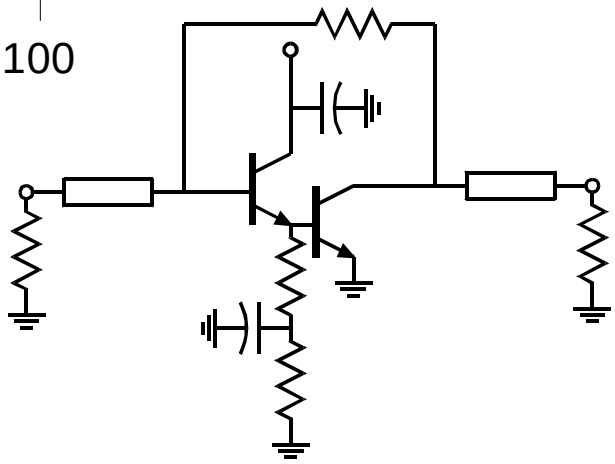
6.7 dB, DC-85 GHz amplifier



Darlington Amplifier - 360 GHz GBW

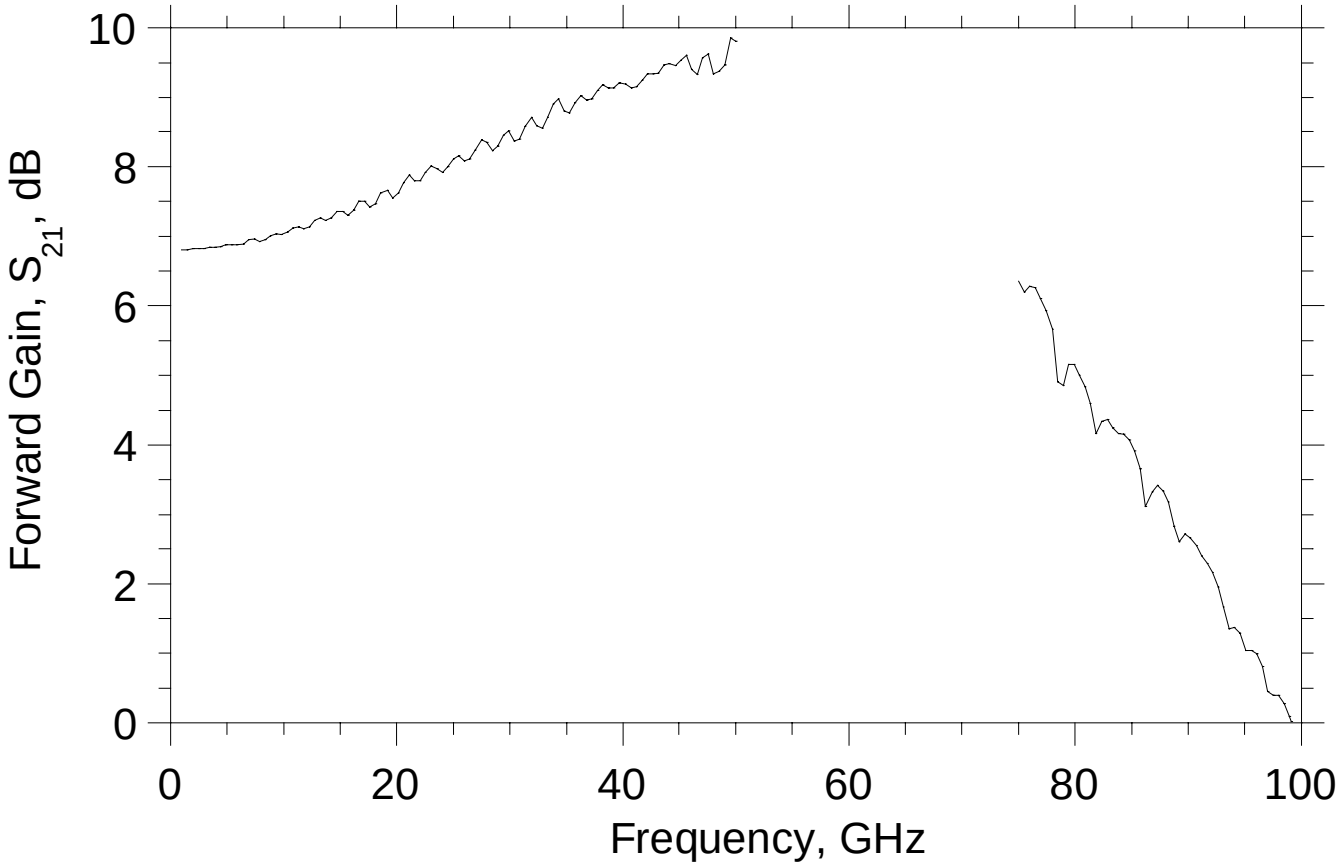


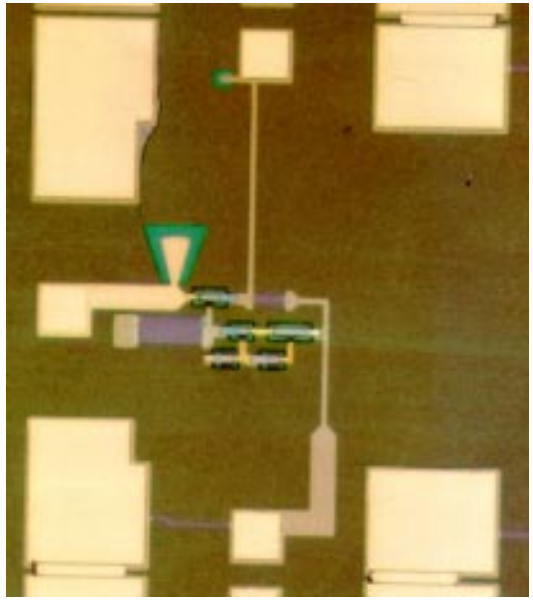


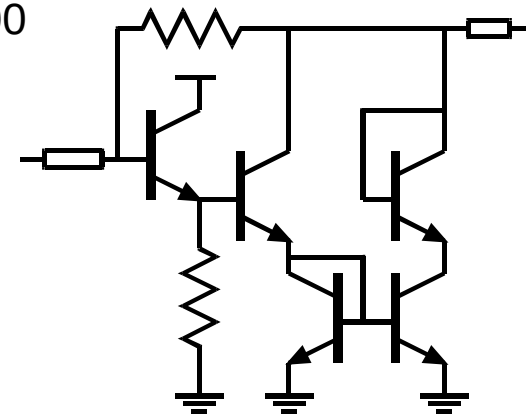


- 15.6 dB DC gain
- Interpolated 3dB bandwidth of 60 GHz
- 360 GHz gain-bandwidth product

6.7 dB, 85 GHz Mirror Darlington Amplifier







- 6.7 dB DC gain
- 3 dB bandwidth of 85 GHz
- f_τ-doubler (mirror Darlington) configuration

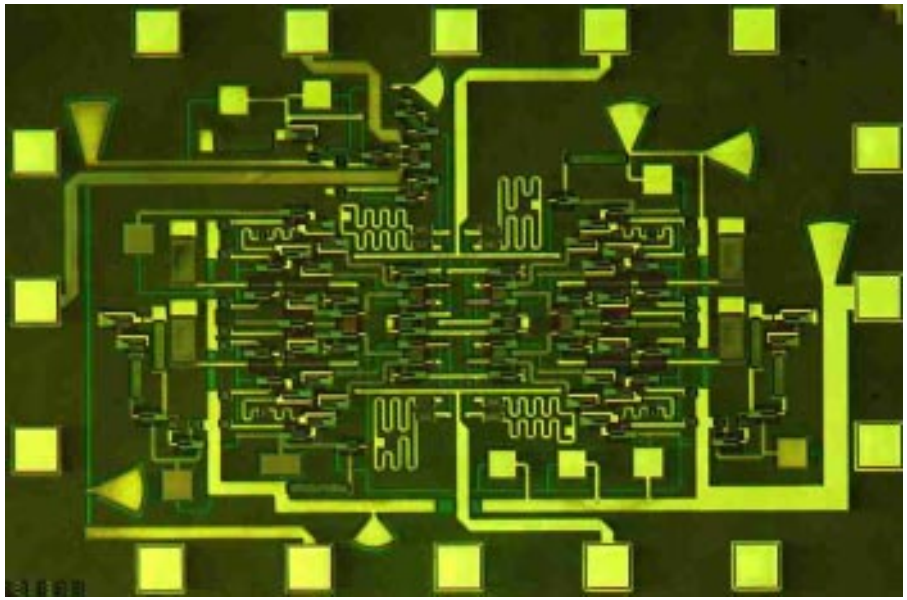
> 66 GHz HBT master-slave flip-flop

Objectives: 100 + GHz logic

Approach:
transferred-substrate HBTs
efficient circuit design

Simulations:
95 GHz clock rate in SPICE

Measurements:
operation to 66 GHz limit of test setup
now building 75-110 GHz test setup



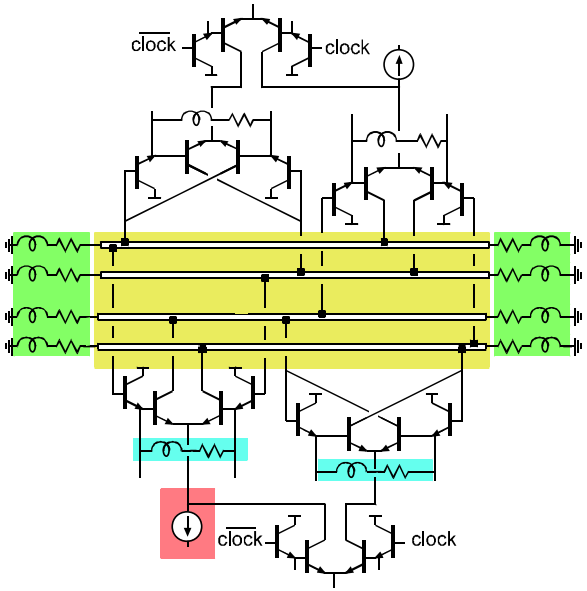
Design features:

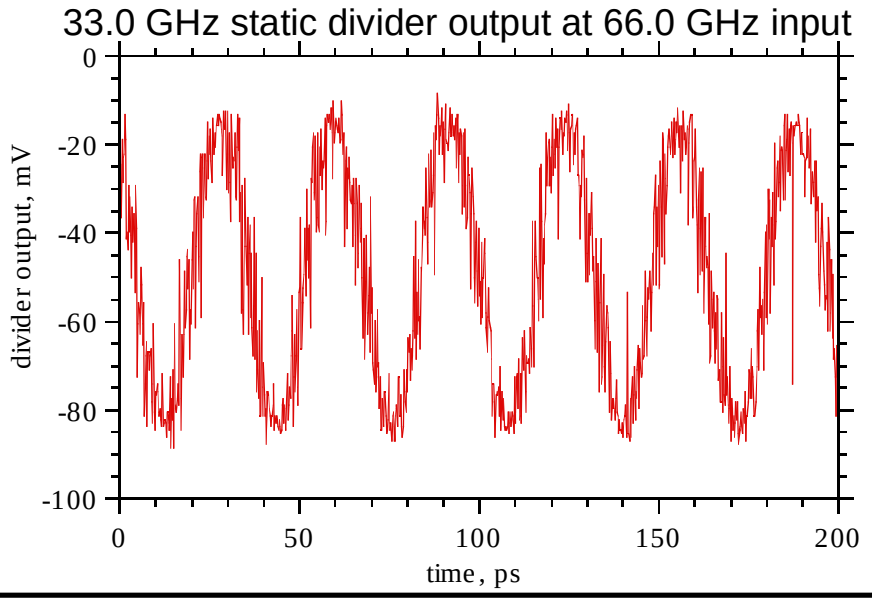
transmission-line bus
short signal path

inductive load

emitter-follower damping

keep-alive bias currents





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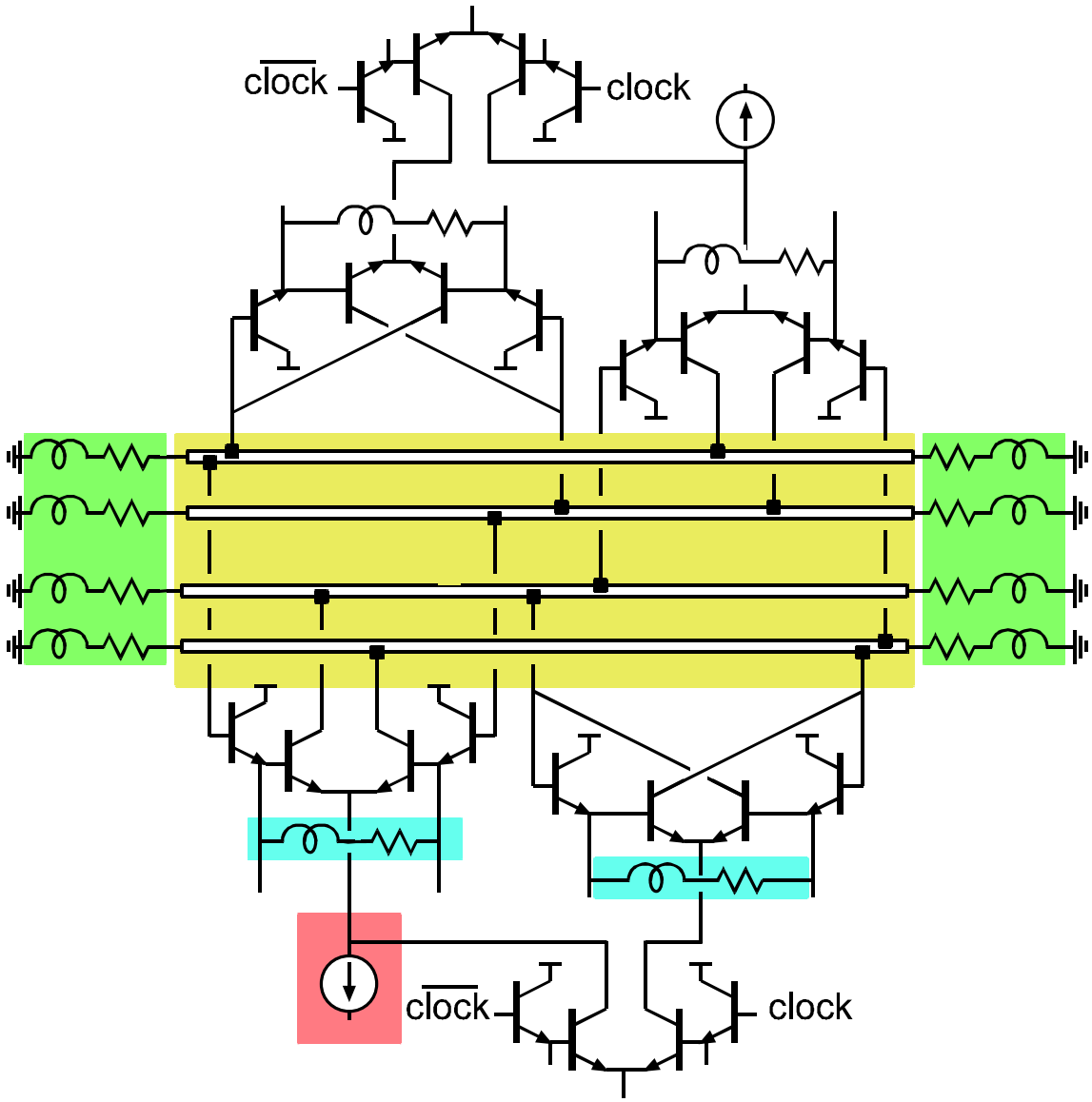
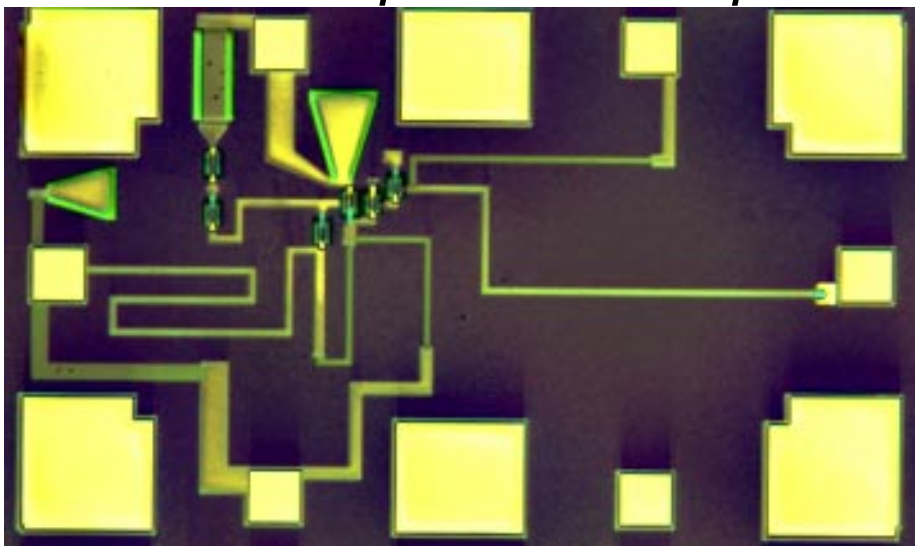


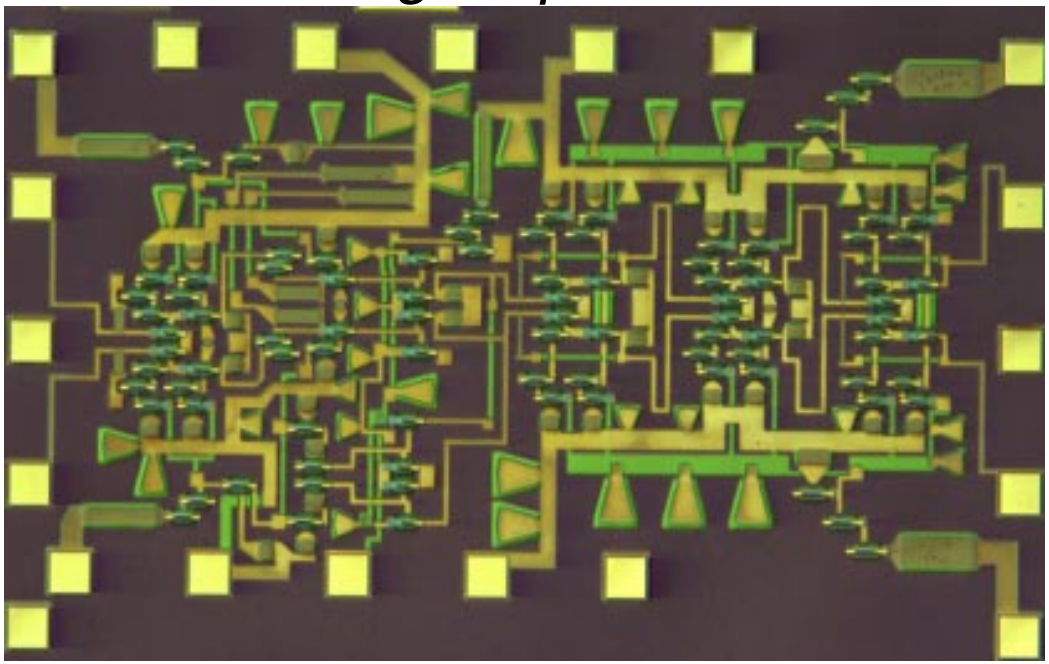
Fiber Optic ICs

not yet tested
(design 40 Gb/s)

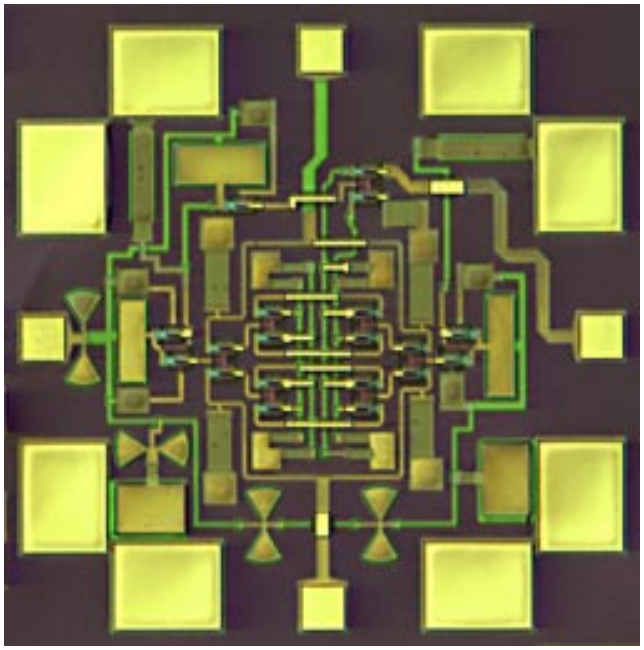
PIN / transimpedance amplifier



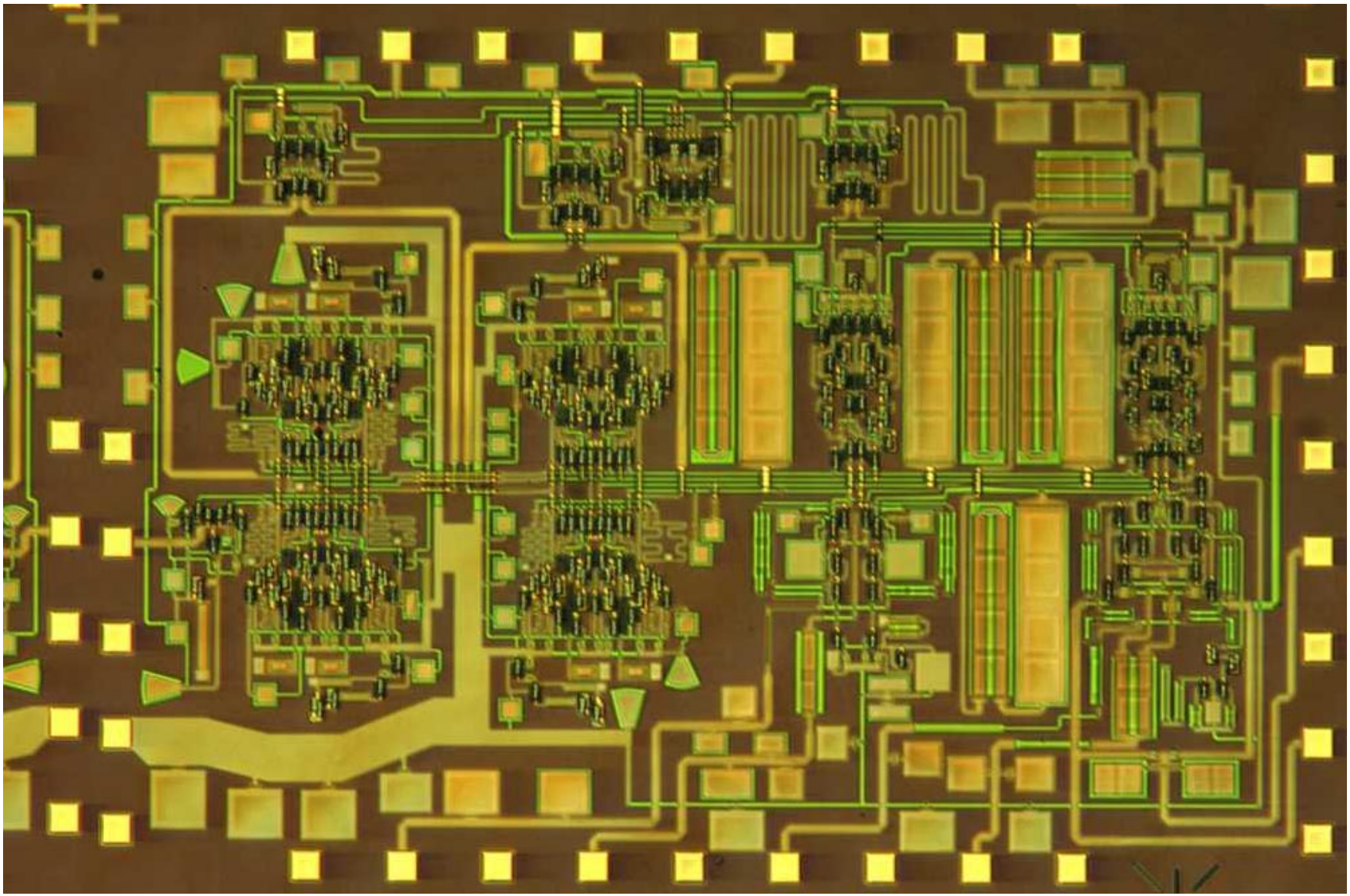
AGC / limiting amplifier



CML decision circuit



Delta-Sigma ADC (300 HBTs)



*Fast ICs **for** fast interconnects*
*Fast ICs **needing** fast interconnects*

ICs for GHz communications:

- Optical fiber transmission to, beyond 40 Gb/s
  - with electronic data switching
- millimeter-wave (60/90/180 GHz) wireless networks
  - at mm-wave, bandwidth is cheap & plentiful
  - …but the hardware must become cheap
- ADCs, DACs for digital processing of RF signals

Challenges for fast ICs

- Fast transistors: scaling is key
- Wiring environment: signal, ground and power integrity
- Interconnect-limited power-delay products
- Managing high dissipated power densities