A Clock and Data Recovery IC for Communications and Radar Applications

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Abstract

A clock and data recovery (CDR) circuit for communications and radar applications was designed and fabricated in a 0.8μm, 27 GHz f_T bipolar process. Experimental measurements demonstrate that the circuit achieves a data rate of 4 Gbit/s with a bit error rate less than 10^{-7}. The circuit includes two phase-locked loops for clock recovery, a delay-locked loop for synchronizing multiple channels with different path delays, and a 1:16 tree-type demultiplexer. In operation, the circuit consumes 3W from a single 3.3V power supply.

Introduction

Continuing improvements in the effective resolution and bandwidth of analog to digital (A/D) conversion circuits have made feasible the processing of high-frequency IF and RF signals in the digital domain. The data rate at the output of the A/D converters used in these applications may be as high as 1-10 Gbit/s. Conveying digital data from an A/D converter to a signal processor at this bit rate is one of the most important challenges in the design of digital radio systems.

In one commonly used approach for representing the output of an A/D converter, the data is encoded in a high-speed serial bit stream. The serial bit stream can then be conveyed to a signal processor through the use of a low-cost single-mode electrical or optical transmission line. Some A/D converter architectures such as one bit oversampling ΔΣ converters (1) are particularly well suited to the serial output approach since their output data is inherently in serial format. Furthermore, the output of an oversampling converter can sometimes be guaranteed to have a specified maximum run length so that the data can be represented in NRZ (non-return-to-zero) format with no encoding overhead.

Clock and Data Recovery

At the destination of the serial data stream, the clock and data must be recovered in order to permit further processing of the digital signal. This is accomplished with a circuit of the form shown in Fig. 1. The core of the circuit is a phase-locked loop (PLL) comprising a voltage-controlled oscillator (VCO), a lowpass filter (LPF) and a dual-edge triggered flip-flop type phase detector (PHD).

The clock and data recovery circuit has been implemented in a commercially available bipolar process (4). Logic functions are generated with a family of emitter-coupled logic gates. To permit the use of two levels of current steering within a 3.3V ($3V_{be}$+0.5V) supply, the voltage drop between levels is set to 0.6V (rather than V_{be}) using a resistor and capacitor (rather than a diode) as shown in Fig. 2(b). The resulting logic is about 50% faster than the directly collector-coupled logic conventionally used for low-supply bipolar gates. The speed improvement results from the decreased effective load capacitance on the collectors of the differential pairs.

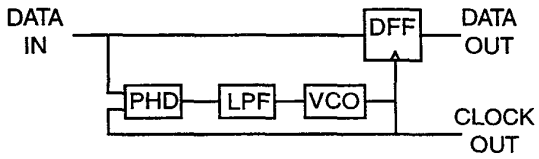

Fig. 1: Clock and data recovery.

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A simplified schematic of the VCO is shown in Figure 3. The oscillator is implemented using an off-chip inductor in conjunction with the base-collector capacitance (C_{bc}) of a transistor as a reactive tank circuit. The frequency of oscillation is varied by changing the voltage applied across the base-collector junction, which changes C_{bc}. This results in a VCO tuning range of ± 20%, which is adequate to compensate for process and component variations. The required inductance for the oscillator is included within the package of the IC. Part of the inductance is obtained from the bond wires connecting the die to the lead frame. The remainder is obtained from a trace on the lead frame. In order to perform on-wafer testing at full speed, a trace with the inductance required for the VCO has been included on the on the probe card.

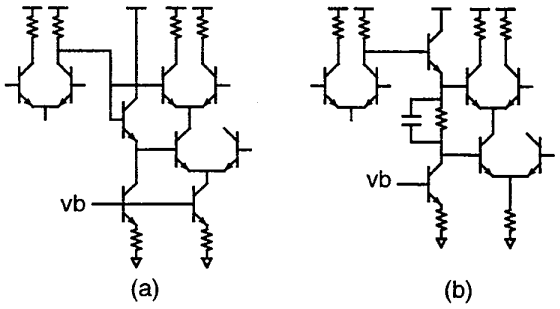

Fig. 2: Implementations of high-speed low-supply bipolar logic:
(a) conventional collector-coupled logic,
(b) faster emitter-coupled logic.

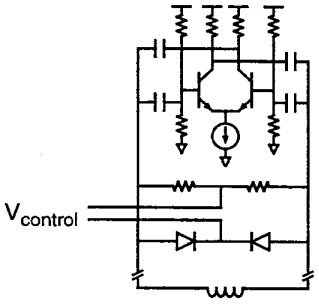

Fig. 3: Simplified schematic diagram of the VCO.

Demultiplexing and Channel Synchronization

The development of the ASIC described in this paper was motivated by an application in which high-speed data streams from multiple sensors are integrated in a central digital signal processor (DSP). The data streams come from oversampled A/D converters (1) placed adjacent to the sensors, as shown in Fig. 4. In order for the central DSP to integrate the data streams, they must be reduced to a lower data rate and synchronized to the central master clock. This is accomplished with the demultiplexing and channel synchronization circuit shown schematically in Fig. 5.

The synchronization is accomplished using a frequency multiplier to generate a 4 GHz clock from the 125 MHz master clock and using a voltage-controlled delay (VCD) to phase-lock the generated clock to the clock recovered from the input data. The voltage-controlled delay modifies the phase relationship of the two 4 GHz clocks to prevent pathological race conditions.

Testability Considerations

In order to increase test fault coverage and to permit the location of faults to be identified, features have been included that allow the three loops and the demultiplexer to be tested independently. The outputs of each of the two VCOs and the VCD have been buffered and made available

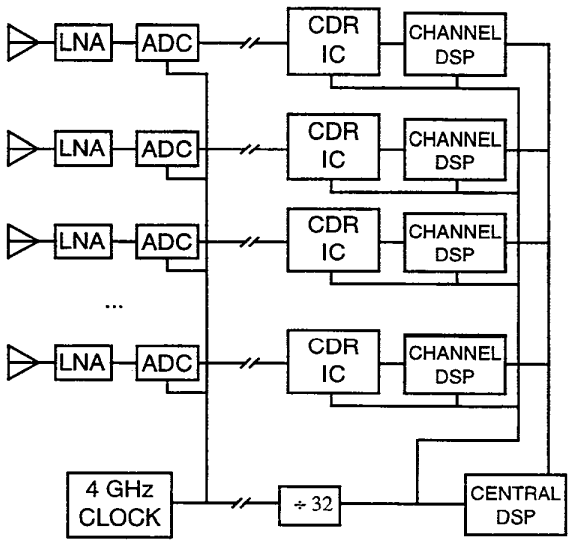

Fig. 4: Interconnections among sensor array, CDR ASICs and DSPs.

on bond pads. Multiplexers have been placed throughout the circuit in such a way that any of the internal clocks or an externally supplied clock can be substituted for the output of the two VCOs and the VCD.

Experimental Results

The IC has been experimentally characterized using a commercially available bit error rate tester (5). For the clock recovery loop operating in isolation, a bit error rate of less than 10^{-8} was measured at a clock rate of 4 GHz. For the circuit operating in its entirety, a bit error rate of less than 10^{-7} was measured at a the same clock rate.

Acknowledgments

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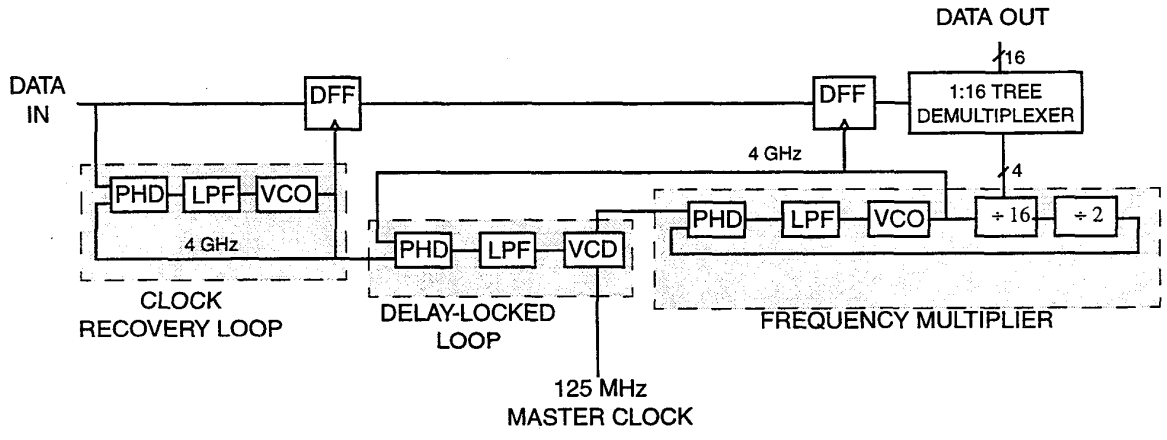

Fig. 5: Demultiplexing and channel synchronization.