HBT MMIC 75GHz and 78GHz Power Amplifiers

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We report W band MMIC power amplifiers in an InGaAs/InAlAs HBT technology. A cascode amplifier with an emitter area of $100\mu m^2$ and a total die size of $0.42x0.36\mu m^2$ delivers 10dBm at 75 GHz under 1.7dB of gain compression. A balanced amplifier composed of two such cascode cells delivers 10.7dBm at 78GHz under 1dB of gain compression. A common-base amplifier delivers 9.7dBm at 82.5GHz under 0.8dB of gain compression. To the best of our knowledge, these results represent the best reported power performance at W band for HBT MMIC amplifiers.

Introduction

Recently, there has been substantial progress in monolithic mm-wave power amplifiers based on InAlA/InGaAs HEMTs [1]. HEMTs with electron beam written gate fingers have until recently exhibited higher mm-wave gains than HBTs, and have dominated W-band applications. By scaling HBTs to submicron junction dimensions and reducing the impact of extrinsic parasitic capacitance [2], very high cutoff frequencies can be obtained which make HBT amplifiers at W-band feasible. Morf et al [3] reported a 98 GHz 4-stage HBT amplifier with 26-dB gain and 250μW output power. Here, we report W-band HBT amplifiers with greatly increased output power. 11.7 mW (10.7dBm) output power has been obtained at 78GHz and 9.3mW (9.7dBm) at 82.5GHz.

Device Technology

Monolithic circuits were fabricated in a substrate transfer process which reduces device parasitics by accessing both sides of the film of epitaxial material. InGaAs/InAlAs single heterojunction bipolar transistors in this technology have demonstrated record RF figures of merit, f_t >250GHz and f_{max} >1 THz [4,5] when the emitter and collector are scaled to deep sub-micron dimensions. The process provides NiCr thin film resistors and Si_3N_4 MIM capacitors along with microstrip transmission lines on a deposited polymer dielectric 5μm thick. Ground vias as small as 5μm square can be defined in this thin microstrip dielectric, providing low inductance, low thermal resistance ground connections which may be located directly "under" device mesas. In the present work, transistors with relaxed lithographic dimensions were used. The nominal emitter and collector finger dimensions were $1x25\mu m^2$ and $2x29\mu m^2$, respectively. A single finger device with these dimensions achieves an f_{max} of 280GHz and an f_t of 170GHz (see Fig. 1). The use of an InGaAs collector small signal device layer structure limits BV_{ceo} to 2.5 V and BV_{cbo} to 6V, where the latter only pertains at zero current.

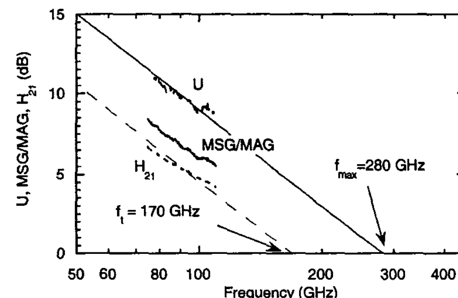

Figure 1 Mason's gain, U, and short circuit current gain, H_{21}, of $1x25\mu m^2$ emitter, $2x29\mu m^2$ collector device.

Circuit Design

Power amplifiers were designed in both common base and cascode topology. In each of these designs the common base output device, as well as the common emitter input device in the cascode amplifier, consisted of four $1x25\mu m^2$ emitter

fingers, where each emitter finger was aligned to a corresponding 2μm wide collector finger. Strong emitter degeneration and the segmented multifinger cascode [6, 7] were used to assure thermally stable operation (see Fig. 2). Large signal output matching to 50Ω was accomplished with a shunt inductor to a large MIM radial stub, along with a quarter wave transformer. The input matching network consisted of an MIM radial stub capacitor and a section of high impedance line. Broadband stability was assured by means of a quarter wave short circuited stub on the input and a resistor shunted to ground on the output. As seen in figure 3, microstrip lines in the input, output, and quarter wave stub networks were meandered tightly, taking advantage of the very thin microstrip substrate. The total die area is 0.42x0.36μm^2.

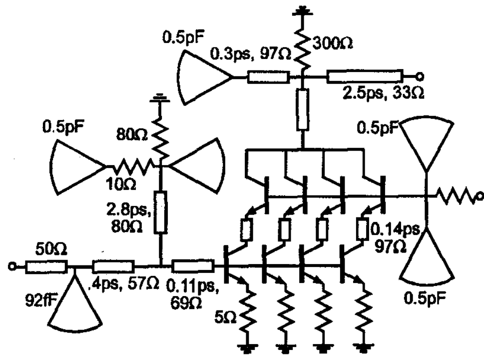

Figure 2: Schematic diagram of cascode power amplifier circuit.

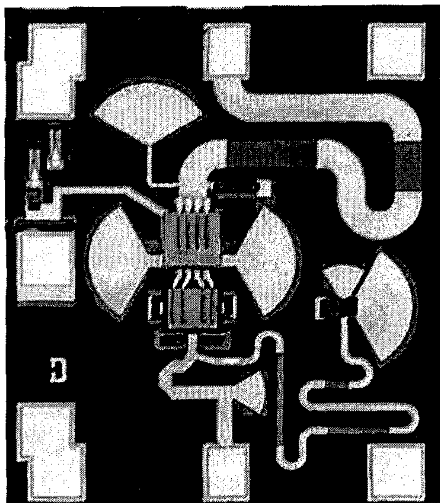

Figure 3 Die photo of cascode power amplifier.

A balanced amplifier was designed using a pair of the above cascode amplifiers (see Fig. 4). A circuit configuration consisting of Wilkinson binary divider and combiner networks along with quarter wave delay lines was chosen for ease of fabrication.

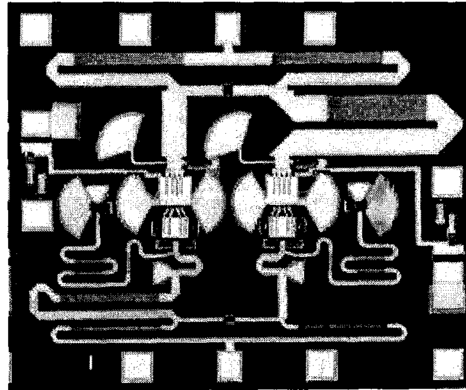

Figure 4 Die photo of balanced amplifier.

Testing

The amplifiers were tested on wafer with waveguide coupled probes. Small signal measurements were made on an HP 8510 network analyzer, calibrated with a commercial LRM substrate. For large signal measurements, a synthesized source was sextupled with active multipliers. The output power was measured with a waveguide coupled power sensor. Losses in the wafer probes and waveguide segments were measured with on-wafer through lines, and output power measurements corrected for the indicated losses, which amounted to some 3.5dB on the output at 75GHz.

Results

The cascode amplifier exhibited 8.5dB of insertion gain at 75GHz, with input and output return losses of greater than 10dB at that frequency (see Fig.4), when biased for peak gain. When biased for peak output power, the amplifier exhibited 7.5dB of insertion gain and 1dB of gain compression at 9.4dBm output power. The maximum output power attained, 10dBm, was limited by the available signal source and not by saturation of the amplifier, which could only be driven to 1.7dB of gain compression.

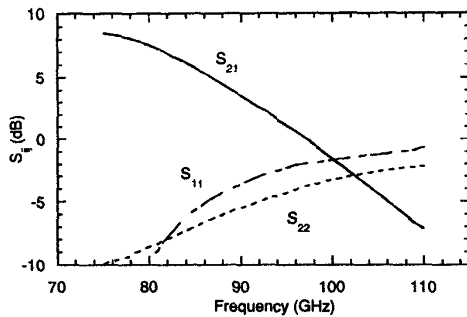

Figure 5 Small signal characteristics of cascode power amplifier.

A balanced amplifier composed of two cascode power amplifiers combined with Wilkinson binary dividers and quarter wave delay lines exhibited 7.9dB of gain at 78GHz under small signal drive, and delivered 10.7dBm output power under 1dB of compression (see Fig.6.)

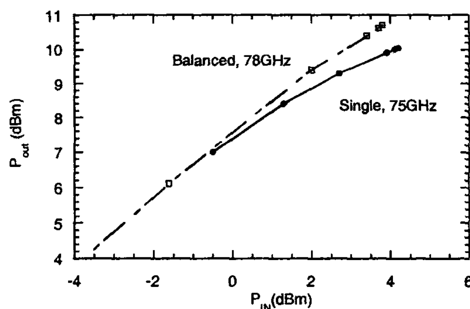

Figure 6 Output power characteristics of single and balanced pair of cascode amplifiers.

The common base amplifier design achieved 5.3dB of gain and 9.7dBm output power at 82.5GHz under 0.8dB of gain compression. This last design did not exhibit unconditionally stable operation, however.

Conclusions

Lithographic scaling applied to the widths of the emitter and collector junctions together has resulted in InP-based HBTs with high power-gain cutoff frequencies. These devices will enable monolithic circuit operation at W-band and beyond. Using InAlAs/InGaAs HBTs with low-breakdown InGaAs collector drift layers, we have demonstrated medium power W-band amplifiers producing approximately 10mW of output power. Submicron scaling of the integrated HBTs can further increase the frequency of operation. With the introduction of InP collectors, greater breakdown voltage and hence output power can be achieved.

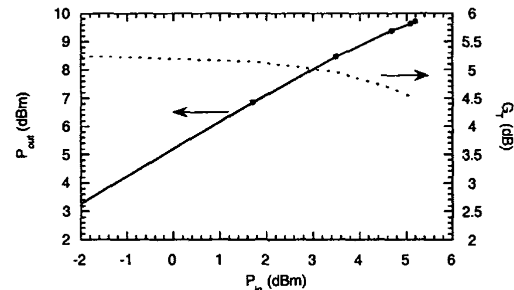

Figure 7 Output power characteristic of common base amplifier at 82.5GHz. Transducer gain, G_T is shown on the right axis.

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