

- 2 LANCASTER, M.J., POWELL, J., and PORCH, A.: 'Thin-film ferroelectric microwave devices', *Supercond. Sci. Technol.*, 1998, **11**, (11), pp. 1323-1334
- 3 MIRANDA, F.A., SUBRAMANYAM, G., VAN KEULS, F.W., ROMANOFSKY, R.R., WARNER, J.D., and MUELLER, C.H.: 'Design and development of ferroelectric tunable microwave components for Ku- and K-band satellite communication systems', *IEEE Trans. Microw. Theory Tech.*, 2000, **48**, (7), pp. 1181-1189
- 4 DEMIDOV, V.E., and KALINIKOS, B.A.: 'Spectra of exchange dipole electromagnetic-spin waves in asymmetric metal-insulator-ferromagnetic-insulator-metal systems', *Tech. Phys.*, 2001, **46**, (2), pp. 219-222
- 5 ISHAK, W.S.: 'Magnetostatic wave technology: a review', *Proc. IEEE*, 1988, **76**, (2), pp. 171-187

## 2-bit adder: carry and sum logic circuits at 19 GHz clock frequency in InAlAs/InGaAs HBT technology

T. Mathew, S. Jaganathan, D. Scott, S. Krishnan, Y. Wei, M. Urteaga, M.J.W. Rodwell and S. Long

Carry and sum circuits for a 2-bit adder used in a pipelined 2*N*-bit adder-accumulator architecture are reported. To obtain high clock rates in a design with multiple gate delays a novel merged AND-OR-Latch structure using four-level series gated current steering logic is employed. These integrated circuits were fabricated in InAlAs/InGaAs transferred substrate heterojunction bipolar transistor technology and operate up to 19 GHz clock rate.

**Introduction:** Adder-accumulators are used as phase accumulators in direct digital frequency synthesis (DDFS) systems [1 - 3]. The DDFS frequency resolution is given by  $\Delta f = f_{ck}/2^N$  and the frequency tuning range is from DC to approximately  $f_{ck}/3$  where  $N$  is the adder-accumulator digital word width [3] and  $f_{ck}$  the clock frequency [3]. Increasing the DDFS frequency range requires increasing the maximum clock frequency of the DDFS components, specifically the phase accumulator (adder-accumulator), Sine ROM, and digital-analogue converter (DAC) [3]. The work reported in this Letter is aimed at increasing the adder-accumulator clock rate.

High clock rates are achieved in pipelined adder-accumulators [3]. These circuits are complex because numerous latches are required for synchronisation between stages (Fig. 1) [3]. For adder-accumulators of 8 to 10 bits total resolution, a pipelined architecture using 2-bit adder blocks provides a good compromise between circuit complexity and clock speed (Fig. 1). In this Letter we describe design techniques employed to increase the clock rate of the carry and sum logic circuit of a 2-bit adder.

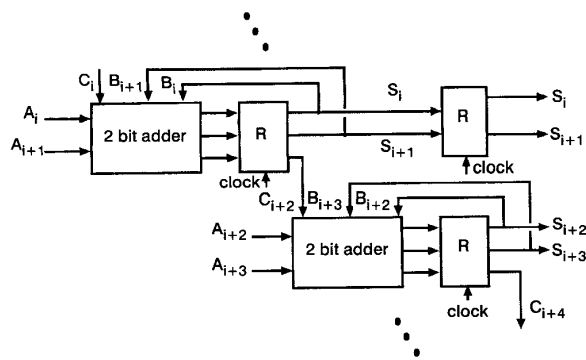


Fig. 1 Pipelined adder-accumulator architecture realised using 2-bit adder blocks

R: register  
A: input word  
S: sum word  
C: carry bit

**Circuit design:** We now describe Boolean logic of the 2-bit adder (Fig. 1). To implement an accumulator, the 2-bit sum is fed back

as an adder input, i.e.  $B_i = S_i$  and  $B_{i+1} = S_{i+1}$ . The 2-bit adder carry input is  $C_{in}$ . The sum ( $S_i, S_{i+1}$ ) and carry ( $C_{i+1}, C_{i+2}$ ) terms are given by

$$\begin{aligned} S_i &= A_i \oplus B_i \oplus C_i \\ S_{i+1} &= A_{i+1} \oplus B_{i+1} \oplus C_{i+1} \\ C_{i+1} &= A_i B_i + A_i C_i + B_i C_i \\ C_{i+2} &= A_{i+1} B_{i+1} + A_{i+1} C_{i+1} + B_{i+1} C_{i+1} \end{aligned}$$

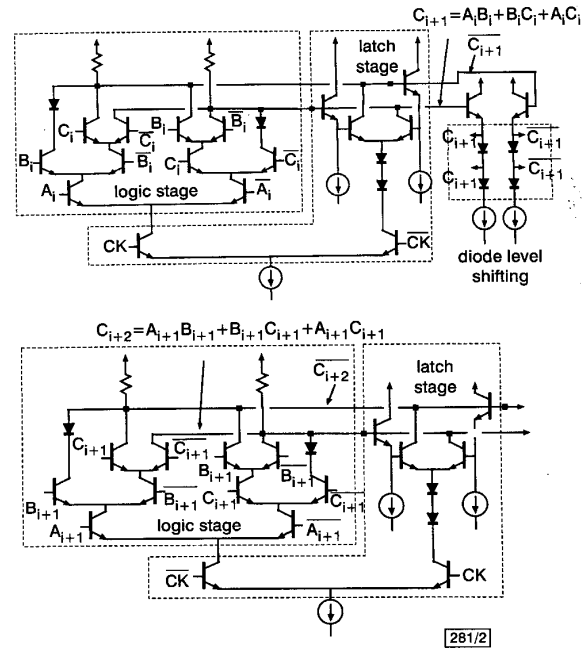


Fig. 2 Carry logic circuit of 2-bit adder

For testing, circuit is configured as frequency divider by setting  $B_i = B_{i+1} = \text{High}$ ,  $A_i = A_{i+1} = \text{Low}$  and  $C_i = C_{i+2}$

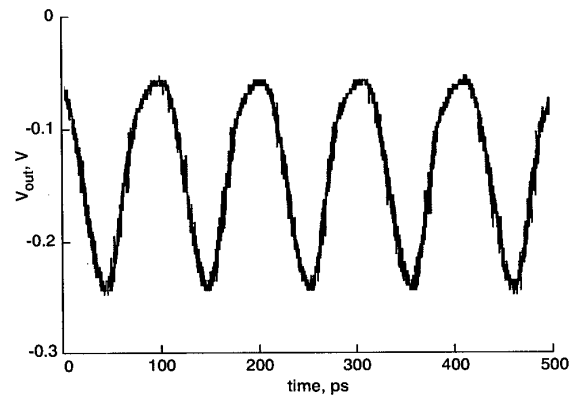


Fig. 3 Output waveforms of carry logic circuit at 19 GHz clock rate  $f_{out} = 9.5$  GHz

Gate propagation delays in forming ( $S_i, S_{i+1}$ ) and ( $C_{i+1}, C_{i+2}$ ) determine the maximum clock frequency, with computation of  $C_{i+2}$  having the longest delay [3]. To reduce delays in evaluating ( $C_{i+1}, C_{i+2}$ ), the AND-OR logic is realised as a single three-level series-gated ECL gate (Fig. 2). This has approximately 1.4:1 smaller gate delay than a carry logic circuit using standard two-level series-gated ECL logic, which requires two cascaded gates. The clock frequency is further increased by merging the logic evaluation and latching (synchronisation) circuits (Fig. 2). This results in a four-level series-gated structure. Simulations indicate a 1.8:1 improvement compared to a standard series-gated ECL AND-OR logic gate implementation with a cascaded latch stage. A similar four-level series-gated circuit (not shown) generates the sum out-

puts ( $S_i, S_{i+1}$ ) by replacing the logic stage shown within the indicated region of Fig. 2 with a three-input, three-level, series-gated XOR gate.

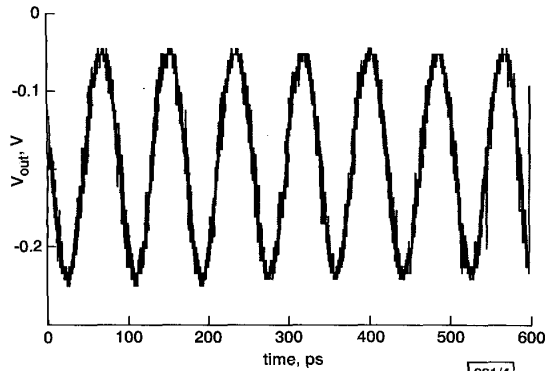


Fig. 4 Output waveforms of sum logic circuit at 24 GHz clock rate  $f_{out} = 12$  GHz

**Measurements and results:** The carry and sum logic circuits were fabricated in transferred substrate InAlAs/InGaAs HBT technology [4]. The HBTs had low DC current gain  $\beta$ , between 5 and 8, due to an error in the growth of the HBT epitaxial base layer. To measure the maximum clock frequency, the carry and sum logic circuits were configured as frequency dividers. This involved setting appropriate inputs to the adder either high (digital 1) or low (digital 0) and feeding back the adder output as one of the inputs. The carry and sum logic circuits operated up to a maximum clock frequency of 19 and 24 GHz, respectively. The output waveforms are shown in Figs. 3 and 4.

**Acknowledgments:** This work was supported by the Office of Naval Research (ONR) under ONR N00014-98-1-0068.

© IEE 2001  
Electronics Letters Online No. 20010788  
DOI: 10.1049/el:20010788

25 June 2001

T. Mathew, D. Scott, S. Krishnan, Y. Wei, M. Urteaga, M.J.W. Rodwell and S. Long (Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106, USA)

E-mail: mathew@ece.ucsb.edu

S. Jaganathan (GTRAN Inc, Westlake Village, CA 91362, USA)

## References

- EDWIN, A.: 'Direct digital synthesis applications', *Microw. J.*, 1990, 33, (1), pp. 149–151
- MANASSEWITSCH, V.: 'Frequency synthesizers theory and design' (Wiley-interscience, New York, 1980), pp. 37–43
- EKROOT, C.G., and LONG, S.: 'A GaAs 4-bit adder-accumulator circuit for direct digital synthesis', *IEEE J. Solid-State Circuits*, 1988, 23, (2), pp. 573–580
- LEE, Q., AGARWAL, B., MENSA, D., PULLELA, R., GUTHRIE, J., SAMOSKA, L., and RODWELL, M.J.W.: 'A >400 GHz  $f_{max}$  transferred-substrate heterojunction bipolar transistor technology', *IEEE Electron. Device Lett.*, 1998, 39, (3), pp. 97–99

## 1480–1510 nm band Tm-doped fibre amplifier with high power conversion efficiency of 42%

S. Aozasa, H. Masuda, H. Ono, T. Sakamoto, T. Kanamori, Y. Ohishi and M. Shimizu

The highest reported overall power conversion efficiency of 42% using a high Tm<sup>3+</sup> concentration-doped fluoride fibre amplifier (TDFFA) with one colour 1.4  $\mu$ m pumping and a double pass configuration for S-band amplification has been achieved. This TDFFA was used for a successful 8  $\times$  10 Gbit/s WDM transmission.

**Introduction:** As the transmission capacity of WDM transmission systems has increased, there have been attempts to expand the signal wavelength band. The S-band has great potential in this respect due to its low fibre loss, and the gain-shifted Tm-doped fluoride fibre amplifier (GS-TDFFA) is one of the most promising candidates for S-band (1480–1510 nm) applications. Two kinds of GS-TDFFA have been developed by shifting the gain band of an S<sup>+</sup>-band (1450–1480 nm) thulium-doped fibre amplifier (TDFFA) [1–5]. One is a dual wavelength (1.4  $\mu$ m/1.56  $\mu$ m) pumped TDFFA [1–3]; the other is a high Tm<sup>3+</sup> concentration-doped TDFFA [4, 5]. To date, GS-TDFFAs have achieved an overall power conversion efficiency (PCE) (defined as the ratio of the output signal power from the amplifier to the total launched pump power into the TDF modules) of 29% [2] and an internal PCE (defined as the ratio of the output signal power from the TDF module to the total launched pump power into the TDF modules) of 48% [3] with dual wavelength pumping. However, dual wavelength pumping requires an extra pump/signal multiplex coupler and this leads to a more complex amplifier configuration.

In this Letter, we present a high Tm<sup>3+</sup> concentration-doped GS-TDFFA with one colour 1.4  $\mu$ m pumping and a double pass configuration. The amplifier achieved the highest overall PCE yet reported, 42%. Furthermore, we achieved an error-free transmission of 10 Gbit/s eight-channel signals through 120 km of dispersion-shifted fibre (DSF) by employing our GS-TDFFAs as post- and preamplifiers.

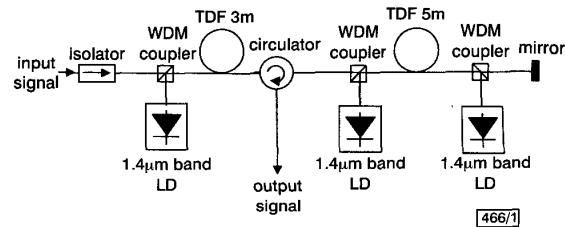


Fig. 1 Proposed GS-TDFFA configuration

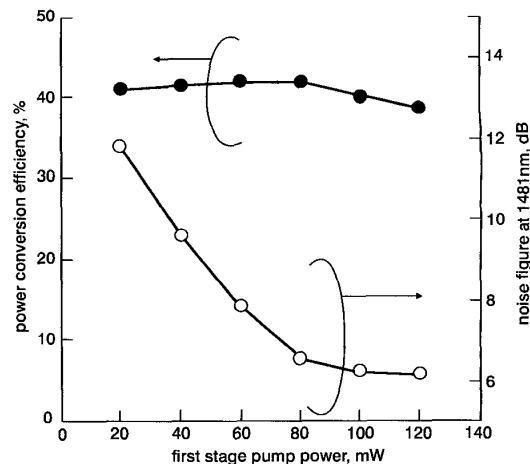


Fig. 2 PCE and NF dependence on first stage pump power

**Experiments and results:** Fig. 1 shows our proposed GS-TDFFA, which consists of cascaded single pass and double pass configurations. The active fibres we used were ZBLAN (ZrF<sub>4</sub>-BaF<sub>2</sub>-LaF<sub>3</sub>-AlF<sub>3</sub>-NaF<sub>3</sub>) fibres with a Tm<sup>3+</sup> concentration of 6000 ppm. The TDFs in the first and second stages were 3 and 5 m long, respectively. We used five LDs operating at 1400 and 1420 nm as pump sources. We measured the amplification characteristics using the inversion locked technique with eight saturation signals. The input saturation signal power was kept at -16 dBm/ch (total power of -7 dBm). We measured the gain and NF for -30 dBm probe signals scanned over the gain bandwidth.

Fig. 2 shows the first stage pump power dependence of the PCE and NF (at 1481 nm). We kept the pump power for the second stage at 500 mW. Pump power is defined as the power launched into the TDF modules. The PCE does not depend greatly on the first stage pump power. When the first stage pump