International Conference on Infrared and Millimeter Waves, September 5-10, Monterey, CA

Low Voltage Swing Techniques for 100 GHz Logic

Y. Betser, S. Jaganathan, T. Mathew, Q. Lee, J. Guthrie, D. Mensa and M.J.W. Rodwell.

Department of Electrical and Computer Engineering
University of California, Santa Barbara, CA 93106

Abstract

Low voltage swing techniques for 100 GHz logic applications are discussed. The use of common base stages as current receivers and of current mirror logic topology is shown to have a high potential for design of very fast digital integrated circuits. In addition, transmission line effects are shown to be of importance for long interconnection lines at the 100 GHz regime.

Introduction

100 GHz digital integrated circuits become more and more of interest for fast fiber optic links, high resolution Direct Digital Frequency Synthesis (DDFS) and several more applications. A key issue for achieving the 100 GHz goal is a MMIC technology, which incorporates very fast devices, passive elements and fast interconnections. Fast devices [1] and fast low scale integrated circuits [2] have already been demonstrated using the Heterostructure Bipolar Transistor (HBT) Transferred-Substrate technology. A schematic cross-section of a Transferred-Substrate HBT is shown in Fig. 1. The low dielectric Benzocyclobutene (BCB) substrate and ground plane (see Fig. 1), which are inherent to the technology makes it potentially suitable for 100 GHz logic applications.

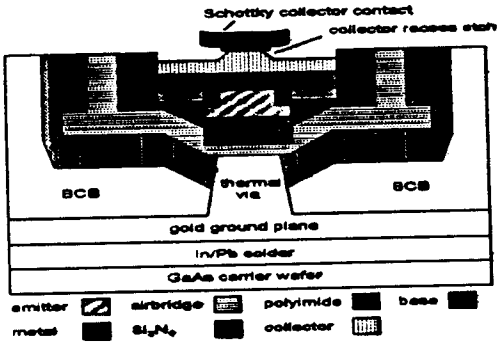

Fig. 1. Schematic cross-section of transferred-substrate HBT.

For larger scale digital integrated circuits, however, device performance is not always the limiting factor in the design. Interconnection design becomes an important issue when the line delay is of the order of the rise/fall time of the digital signal. In addition, when large fan-in and/or fan-out circuits are implemented, innovative circuit design techniques are necessary to obtain the desired circuit performance. In this paper we discuss several key issues in fast bipolar logic circuit design with emphasis on low voltage swing techniques.

The Interconnection Limit

Consider an interconnection environment on a low dielectric substrate (such as BCB) for a 100 GHz digital circuit. Roughly, a 200 μm long line, exhibits a 1 ps delay. Thus, for a 100 GHz digital signal with a rise/fall time of ~ 3 ps, the interconnection distributed LC structure becomes important for lines longer than 600 μm. A complex digital design with several decision circuits (flip-flops) is expected to have interconnect lines longer than the above limit. One way of solving this problem is by implementing regeneration buffers along the interconnect lines. However, this would increase both power dissipation and circuit dimensions. It is therefore necessary to implement broadband analog RF matching techniques. An example of a doubly terminated differential interconnection is shown in Fig. 2. Note that the Emitter follower stage, which is commonly used in many fast digital designs, is located at the far end of the line and not close to the driver buffer. This is done in order to prevent oscillations due to the inductive low impedance nature of an emitter follower at high frequencies and in order to increase the bandwidth of reliable matching.

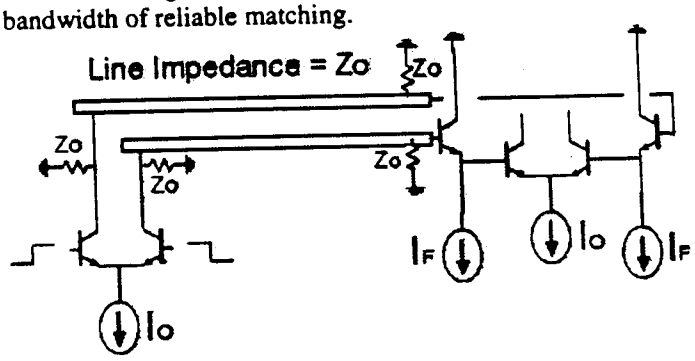

Fig. 2. Doubly terminated interconnect line with Emitter Follower buffer.

In Fig. 2 the termination resistors were chosen to have the same value as the line impedance. However, when an interconnect line is frequently loaded with a capacitance loading so that $C_{Load} > C_{Line}$ (e.g. memory structures, clock distribution busses) the loaded line impedance is decreased by a factor of $\sqrt{C_{Load} / C_{Line}}$ and the resistors values should be appropriately modified.

Low Voltage Swing Techniques

A basic expression for approximating a digital circuit time delay, τ, with a digital voltage-swing ΔV, a driver current I_O and a load capacitance C_L is: $\tau \sim C_L \Delta V / I_O$. Usually, ΔV is chosen to be the minimum voltage swing sufficient for defining a logic state. For a bipolar technology, ΔV of 300-600 meV is mostly chosen. It is obvious from the above expression that in order to minimize τ for a given ΔV and C_L, a large I_O is necessary. However, for a given current density, an increase in I_O will increase not only the power dissipation but also the device dimensions, which in turn will increase C_L.

An alternative circuit design topology is suggested, in which an "analog" voltage swing of only a few 10's meV will be generated along high capacitance nodes, with a following digital regeneration performed at low capacitance nodes. The basic idea behind this scheme is the use of current signals instead of voltage signals. Due to the exponential current dependence of bipolar transistors, a change by a factor of n in the current signal will create a voltage change of the order of KT x ln(n). The same principle was used by Gilbert for his Translinear circuits [3], but here the circuit topology is adjusted for fast digital logic circuits. Two basic configurations are shown in Figs. 3 and 4: a common base current receiver configuration and a current-mirror logic configuration.

In Fig. 3 a multiple input NOR gate is shown using an ECL wired OR configuration. Unlike regular ECL gates, where the output is the voltage of the emitter node, here the output is the collector current. Due to the large fan-in, both collector and emitter lines have a large capacitance loading which will limit frequency operation if digital voltage swing is present. The voltage swing, however, in the collector output, which is given by $KT \times \mathrm{Ln}(I_O / I_K)$, is of the order of 20 meV, for $I_O = I_K$. The digital state is regenerated at the collector of the common base HBT.

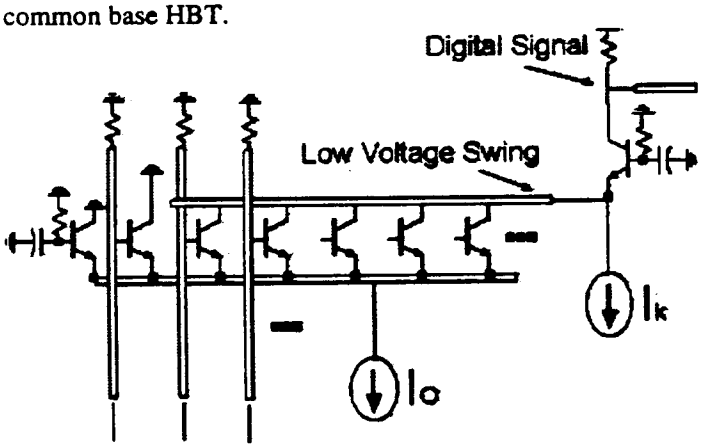

Fig. 3. ECL multiple input NOR gate with common base current receiver.

In Fig. 4 multiple digital functions are implemented using a current mirror configuration. One current mirror driver is used for driving a large fan-out of gates. The gates on and off states are defined by the currents I_{ON} and I_{OFF}, respectively. Therefore, the voltage swing along the high capacitance base line is relatively low. In additional to being a logic driver, a current mirror can also serve as a low impedance termination and digital regeneration stage for a low impedance line, in a similar way to the common base receiver shown in Fig. 2b.

A third voltage swing configuration, not shown here, implements a trans-impedance amplifier as a combined low impedance and low voltage swing termination with a gain regeneration.

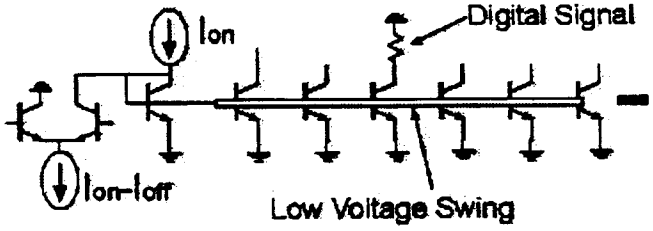

Fig. 4. Current mirror low voltage swing logic.

Conclusions

Innovative circuit design techniques, which implement "analog" design into the digital circuits, are described. It is suggested that the use of low voltage swing techniques as well as proper interconnection design will enable the future design and fabrication of 100 GHz logic integrated circuits.

References

1. Q. Lee, S.C. Martin, D. Mensa, R.P. Smith, J. Guthrie, S. Jaganathan, Y. Betser, T. Mathew, S. Krishnan, L. Samoska, M. Rodwell, "Submicron Transferred-Substrate Heterojunction Bipolar Transistors with greater than 1 THz fmax ", 1999 IEEE Device Research Conference.
2. Q. Lee, D. Mensa, J. Guthrie, M. Rodwell, S. Long, S.C. Martin, R. P Smith, Y betser, S. Jaganathan, T. Mathew, P. Krishnan, C. Serhan, "Ultra high frequency HBT integrated circuits ", 1999 Ultrafast Electronics and Optoelectronics Conference.
3. B. Gilbert, "Translinear circuits: an historical overview" Analog Integrated Circuits and Signal Processing, vol.9, (no.2) March 1996. pp. .95-118.