Submicron Scaling of III-V HBTs for 40-200 GHz Analog & Digital ICs

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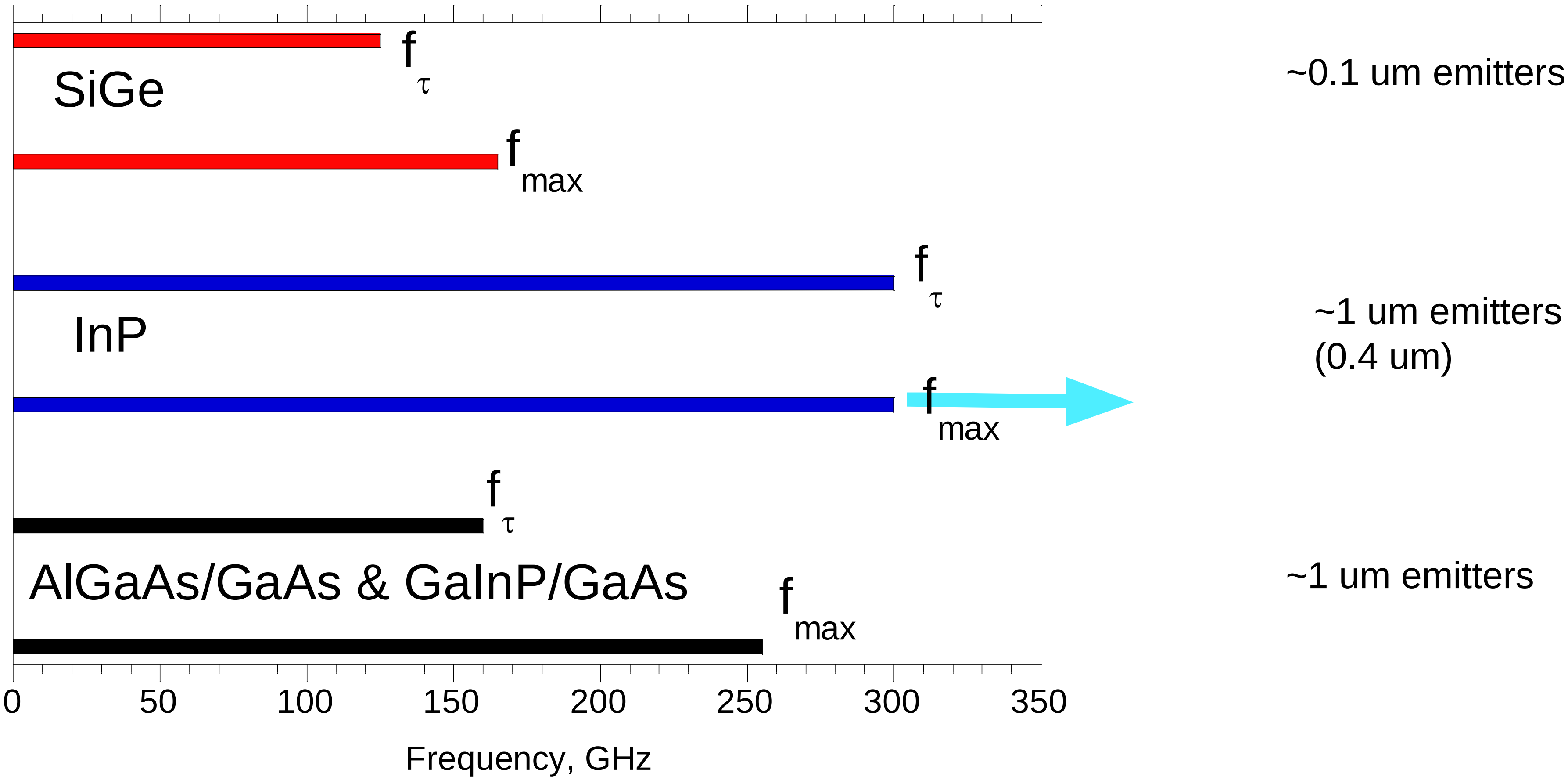
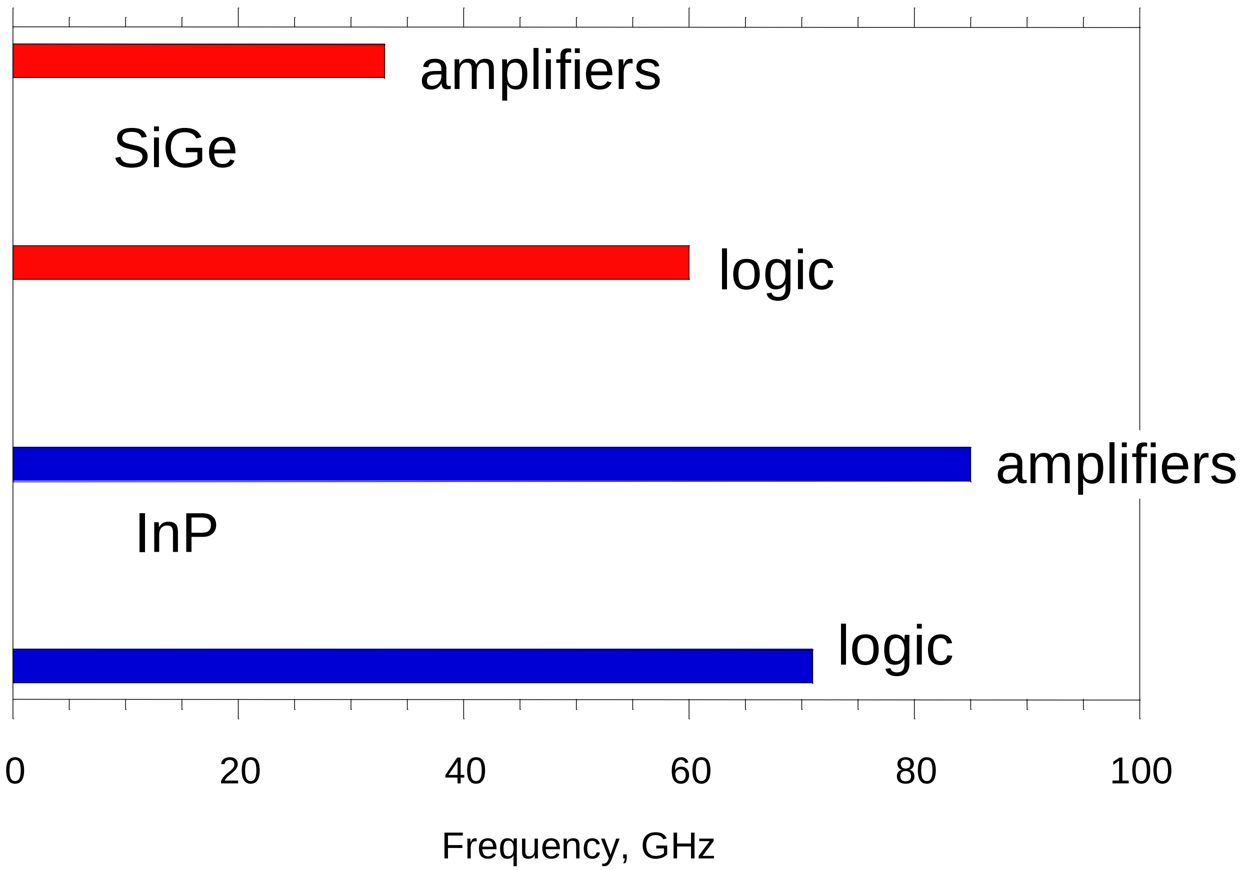
State-of-art in HBTs, 2000: cutoff frequencies



Si / SiGe have significantly poorer material parameters

…but are ***much better scaled in size and current density***

State-of-Art in HBTs, 2000: small-scale circuits



Si / SiGe has rough parity in logic with InP despite lower ft, fmax

due to higher current density, better emitter contacts

Si/SiGe has significantly slower amplifiers due to lower ft, fmax

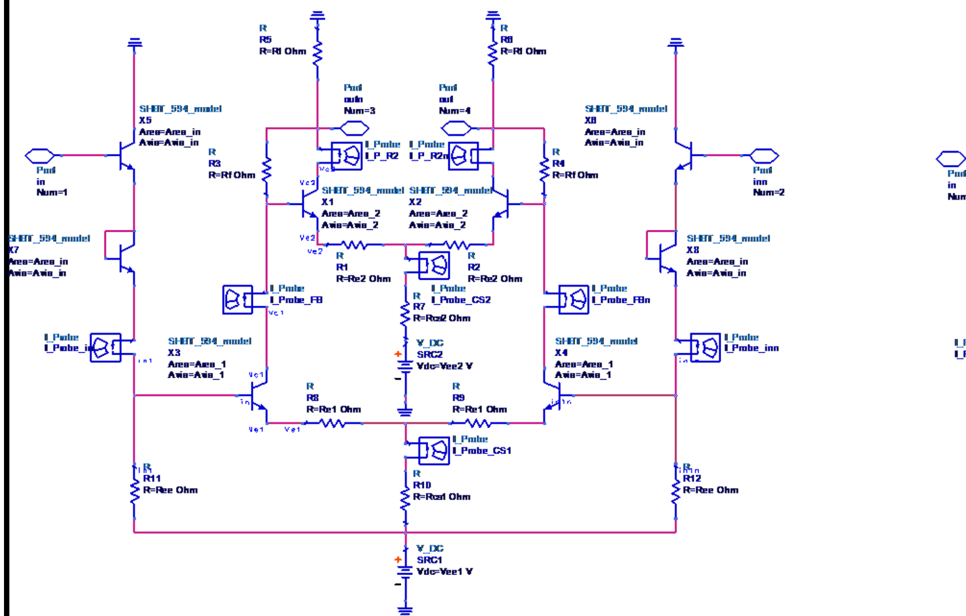
Si/SiGe has ***much better scales of integration, etc***

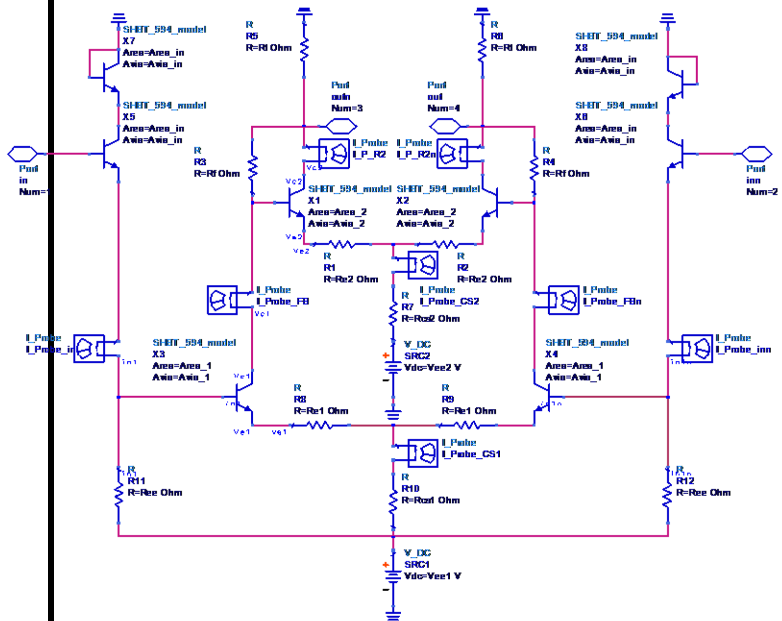
Agilent
Conexant

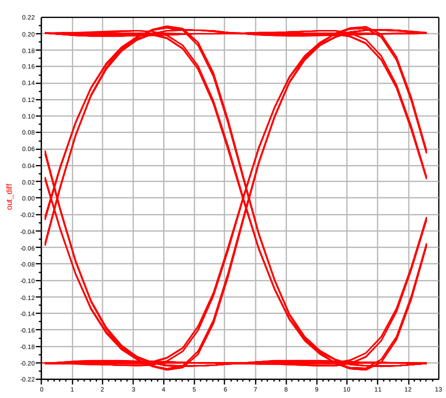
160 Gb/s is more than possible !

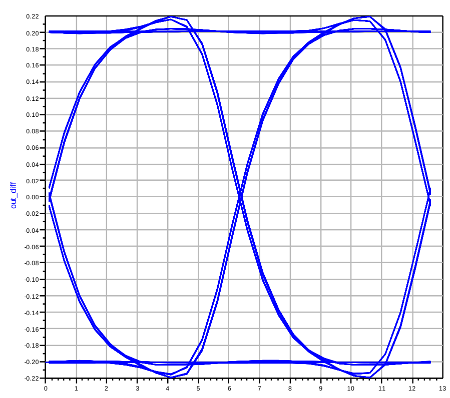
UCSB

Zach Griffith

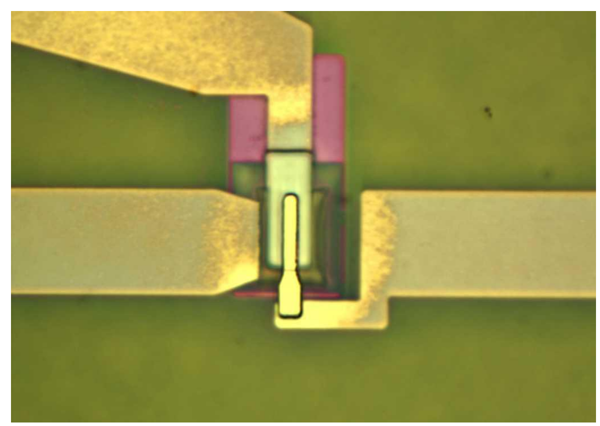








160 Gb/s LIA simulations using UCSB HBT model



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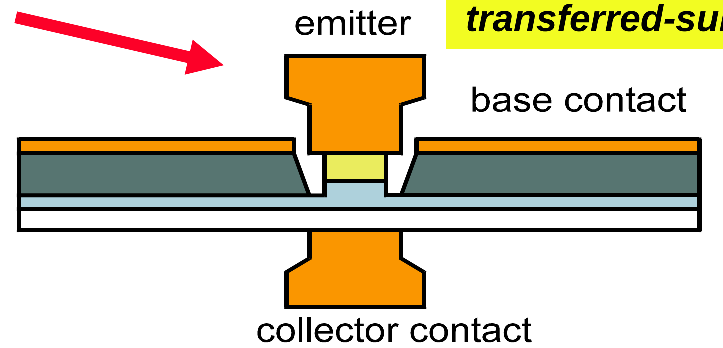
Scaling Laws for fast HBTs

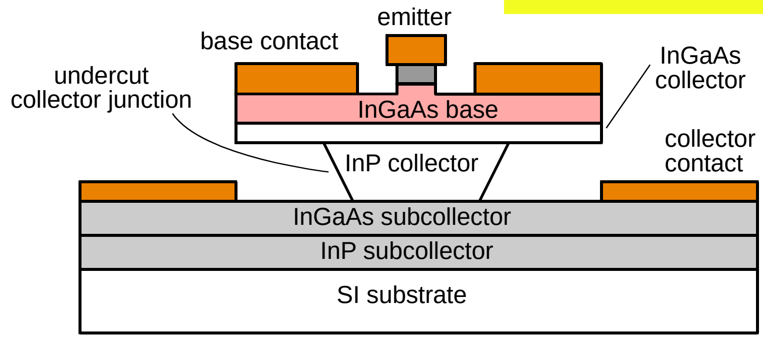
for x 2 improvement of *all* parasitics:
f_t, f_{max}, logic speed…
base √2: 1 thinner
collector 2:1 thinner
emitter, collector junctions 4:1 narrower
current density 4:1 higher
emitter Ohmic 4:1 less resistive

Challenges with Scaling:
Collector
mesa HBT: collector under base Ohmics.
Base Ohmics must be one transfer length
sets minimum size for collector
Emitter Ohmic:
hard to improve…how ?
Current Density:
dissipation, reliability
Loss of breakdown
avalanche Vbr never less than collector Egap
(1.12 V for Si, 1.4 V for InP)
….sufficient for logic, insufficient for power

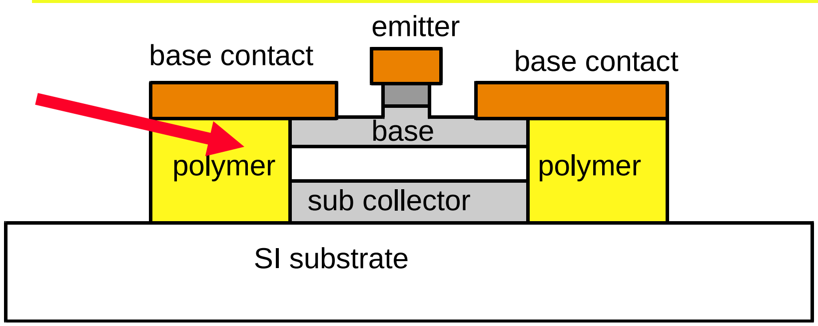
transferred-substrate



undercut-collector



Narrow-mesa with 1E20 carbon-doped base



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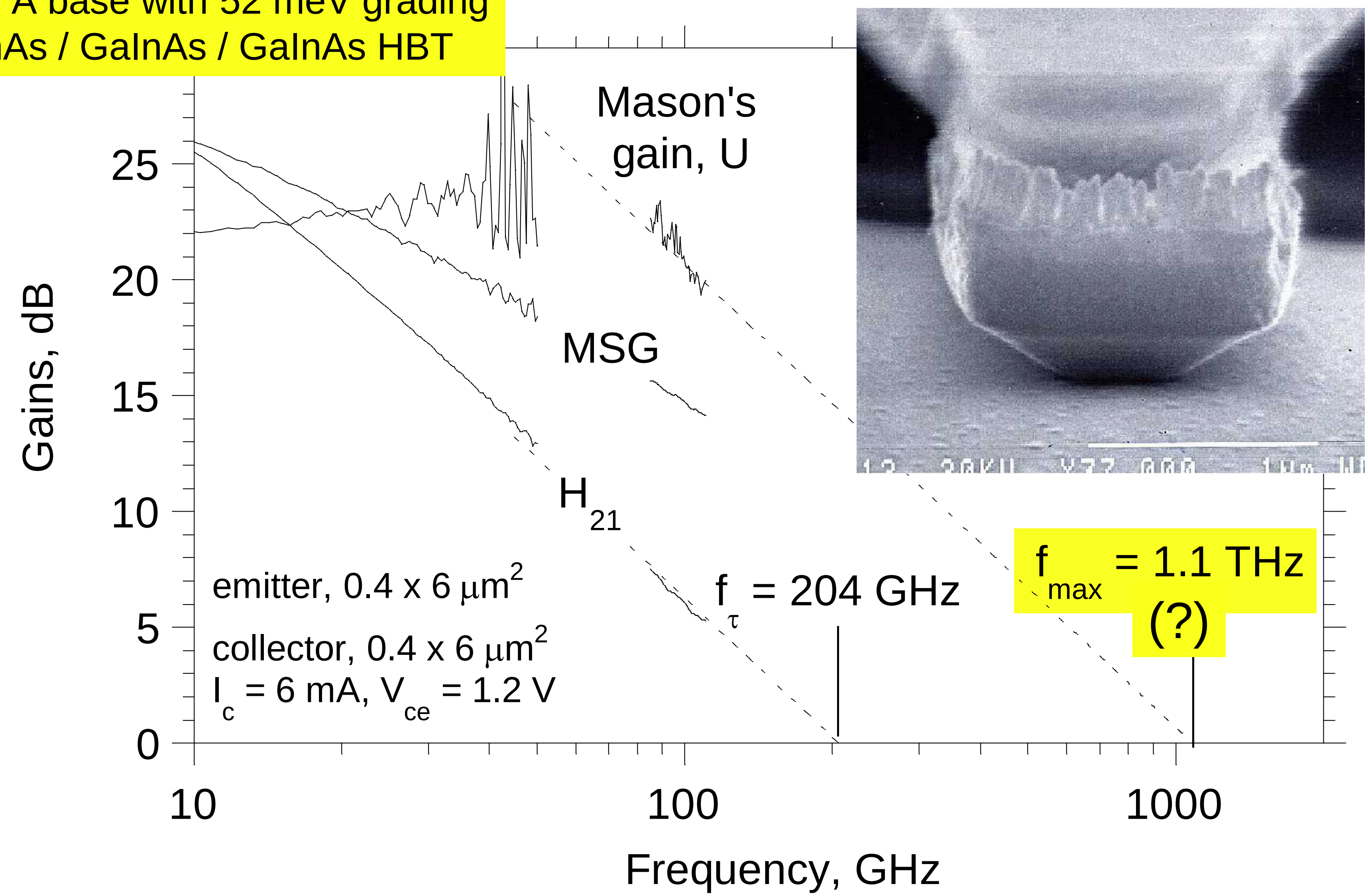
Submicron Transferred-Substrate HBT

UCSB

Michelle Lee

3000 Å collector
400 Å base with 52 meV grading
AlInAs / GaInAs / GaInAs HBT



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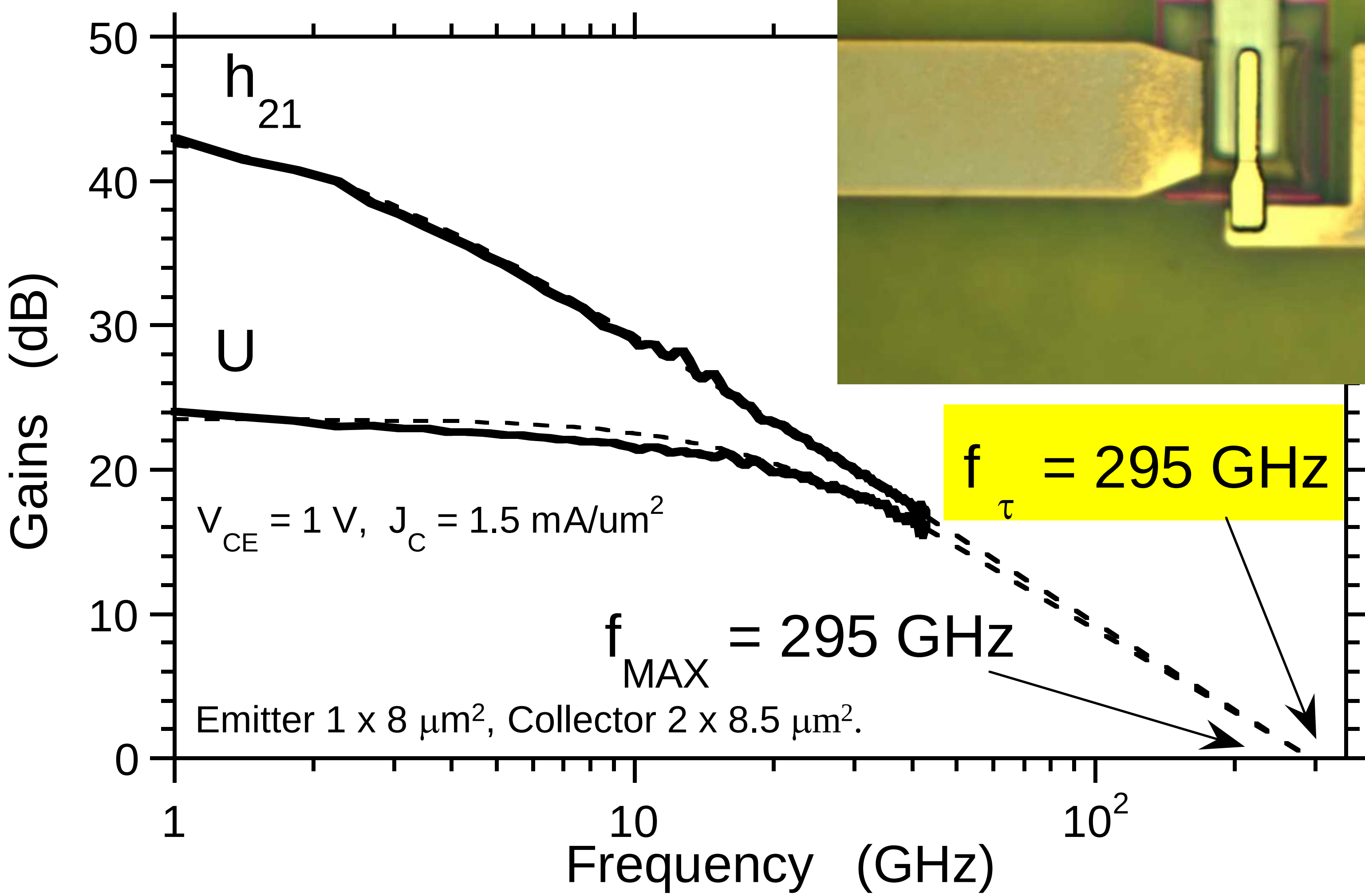
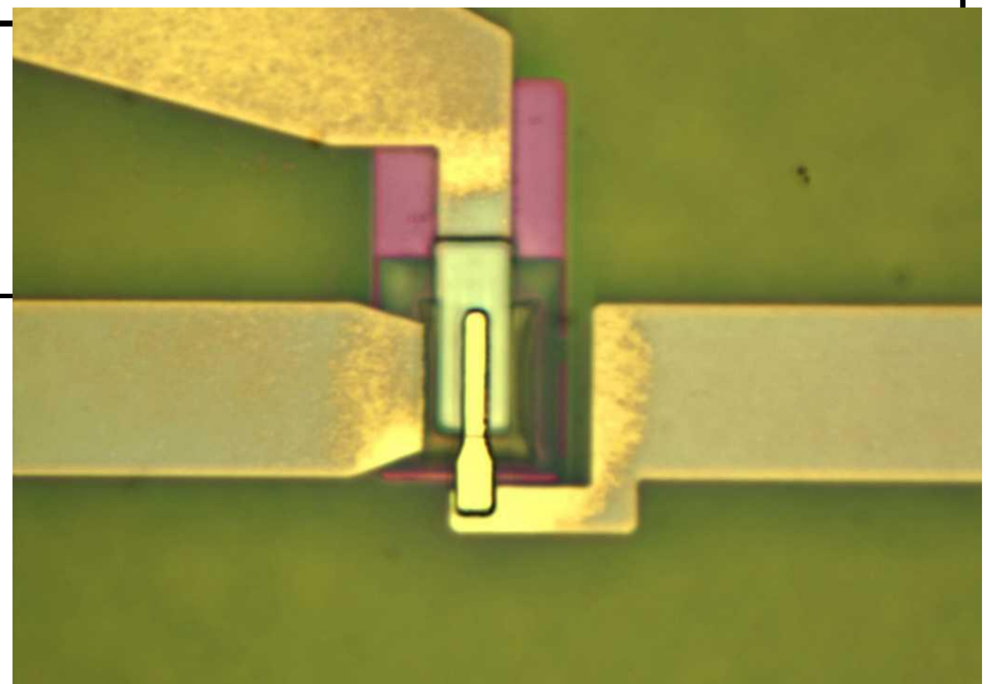
Record f_τ HBT

UCSB

Yoram Betser

2000 Å collector
300 Å base with 52 meV grading
AlInAs / GaInAs / GaInAs HBT



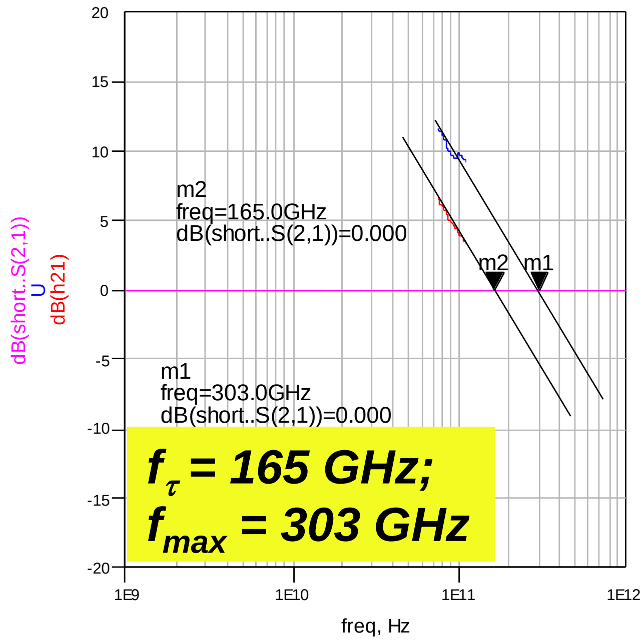


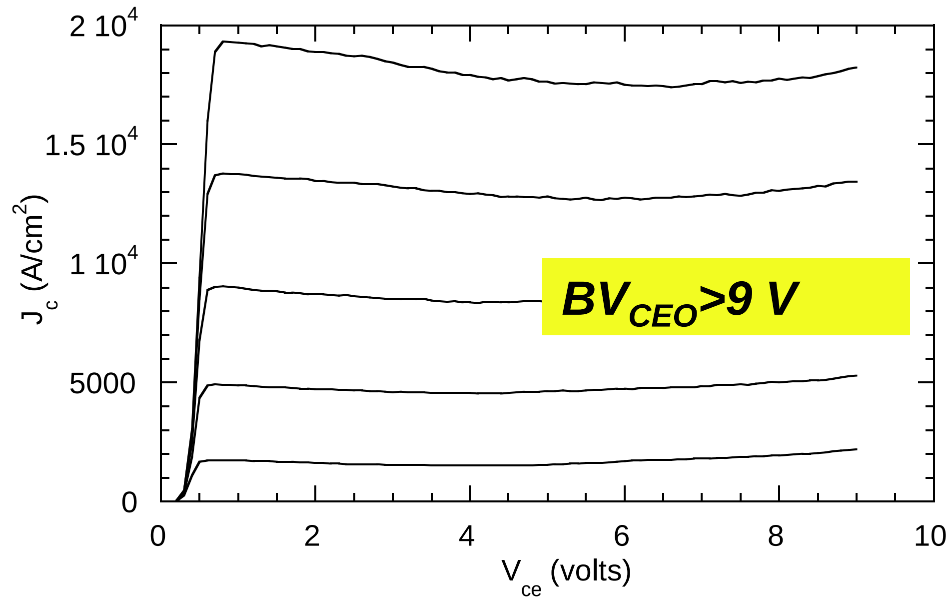
UCSB

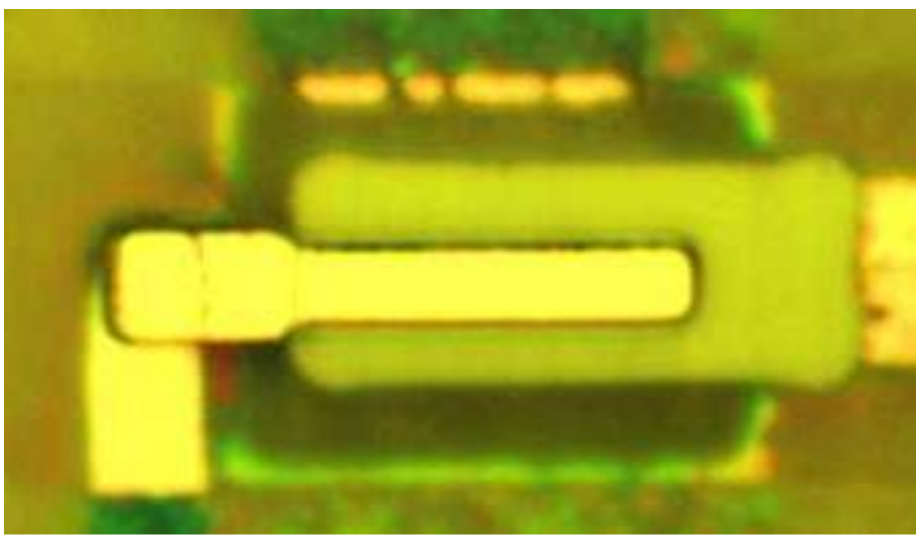
pk Sundararajan
M Dahlstrom

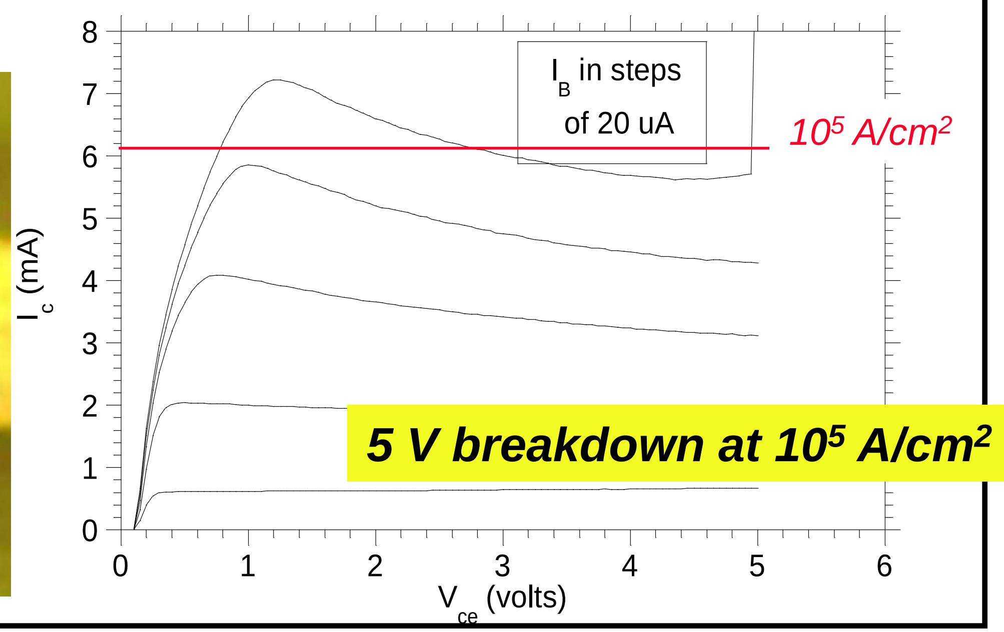
High Speed, High Breakdown DHBTs

1x 8 micron emitter, 2x 10 micron collector









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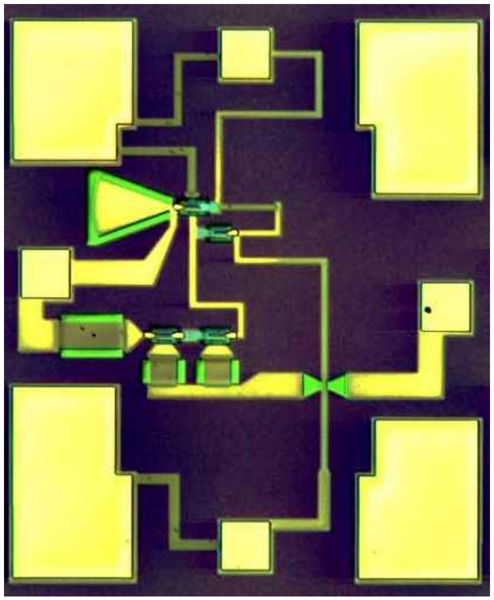
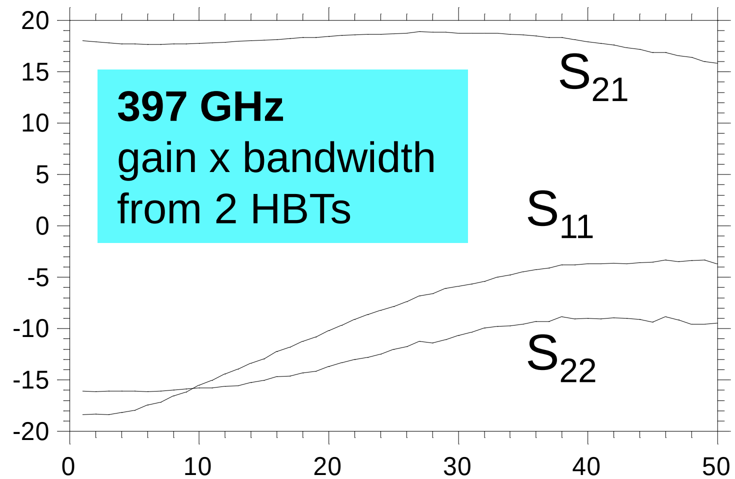
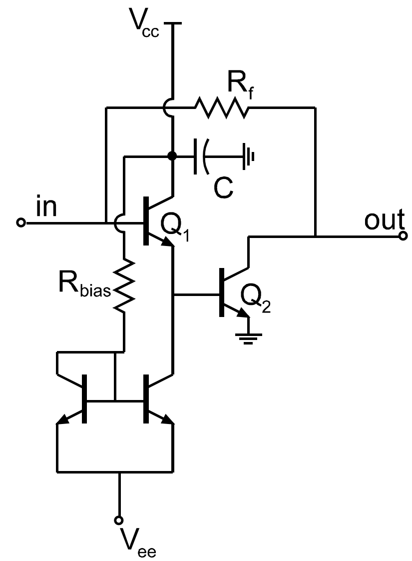
High Speed Amplifiers

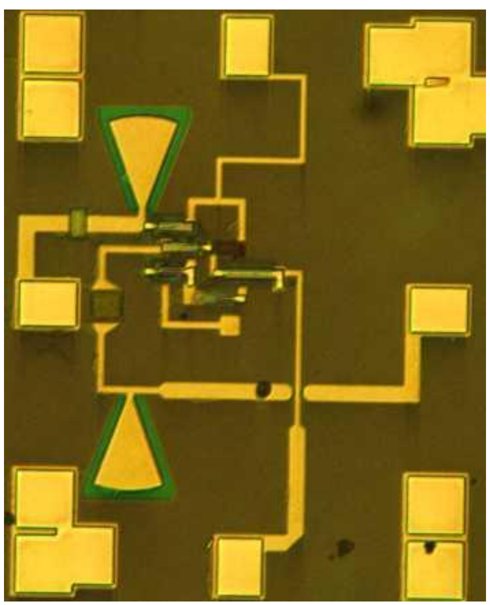
UCSB
Dino Mensa
PK Sundararajan



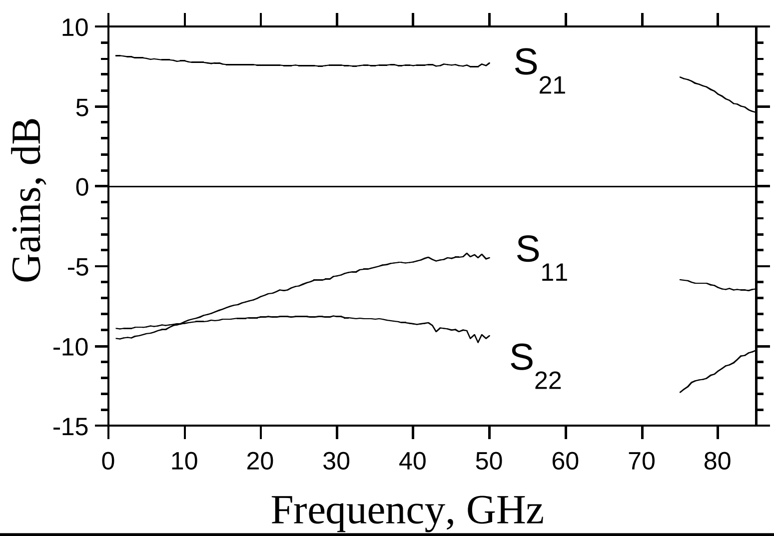
18 dB, DC-50 GHz

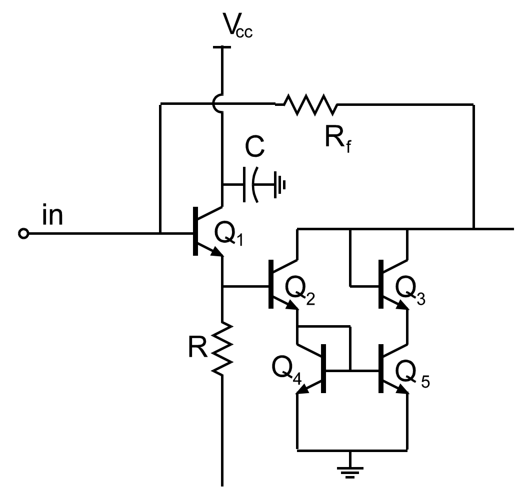






8.2 dB, DC-80 GHz





AFOSR

HBT distributed amplifier

11 dB, DC-87 GHz

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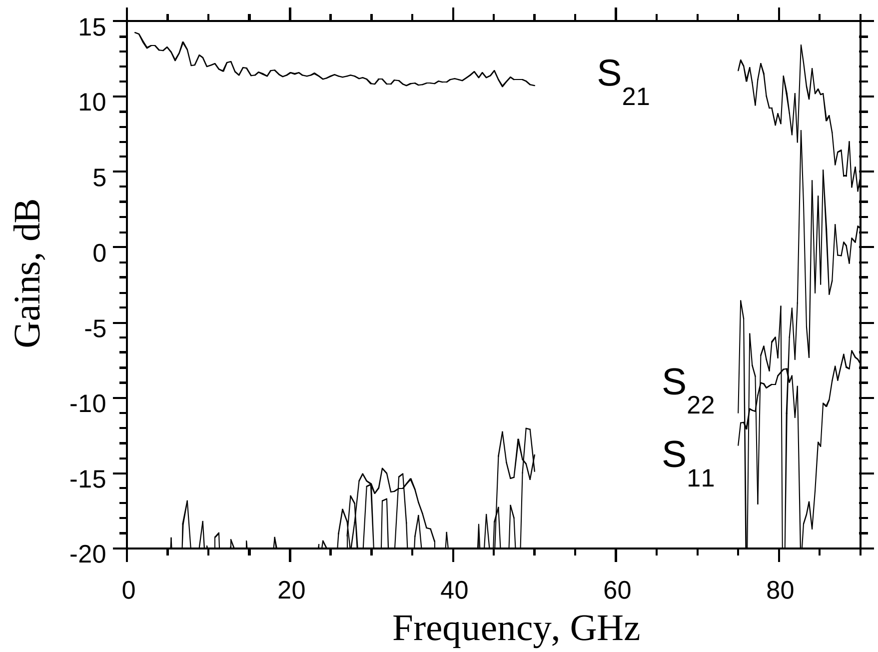
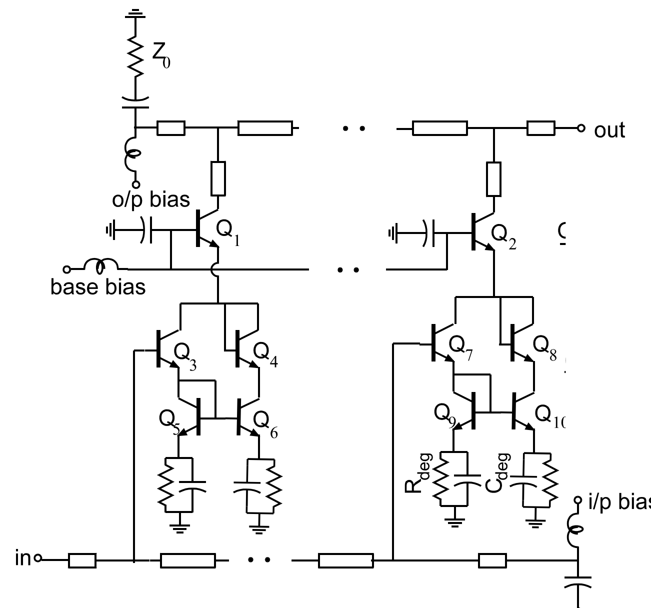
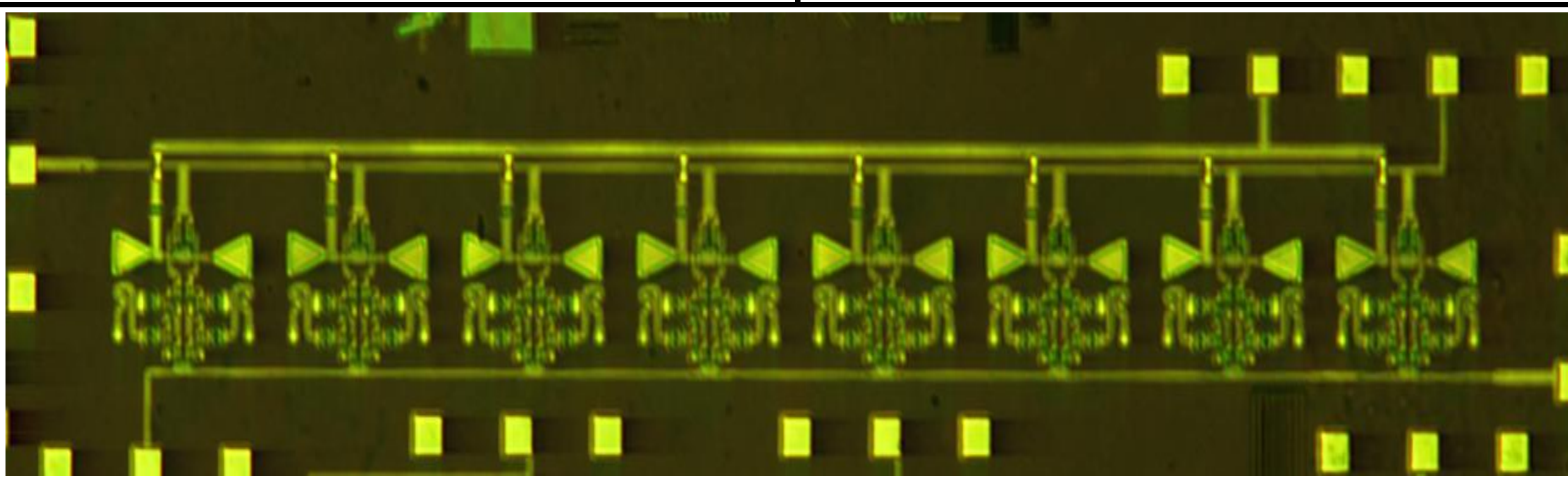
PK Sundararajan





TWA with internal ft-doubler cells



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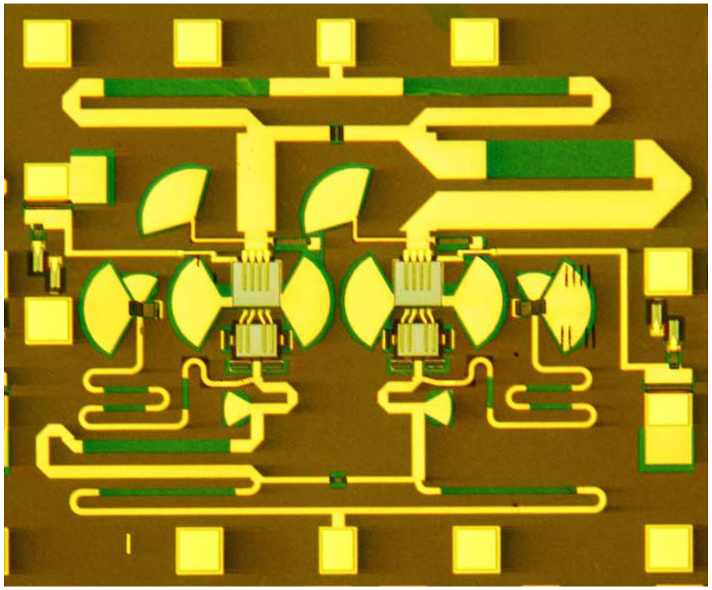
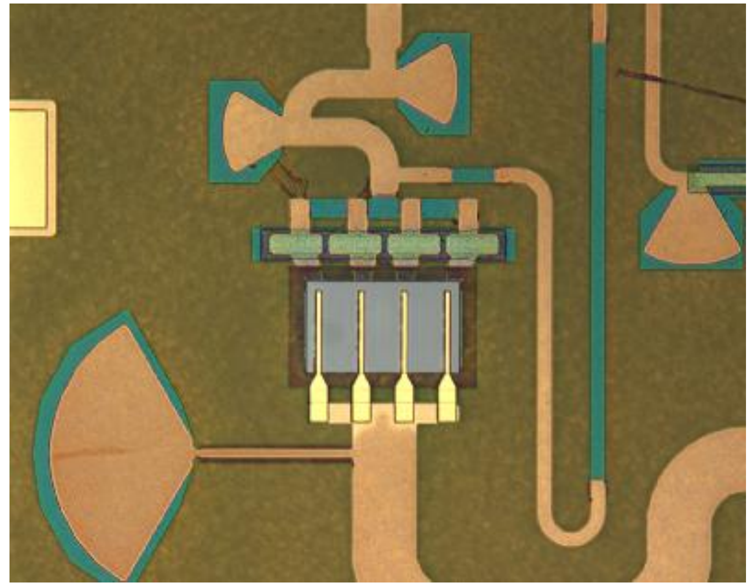
James Guthrie

InP-HBT W-band Amplifiers

ARO
Caltech



Balanced Amplifier: 10.7dBm at 78GHz

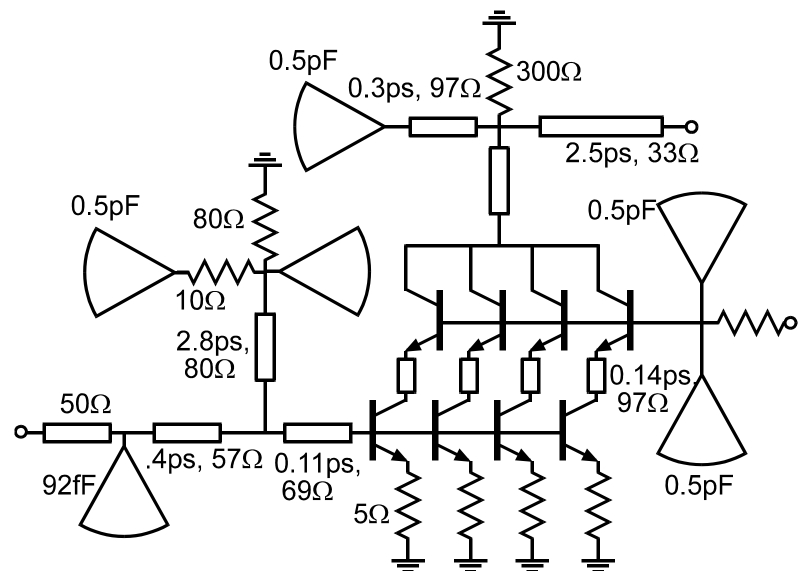


Common-Base Amplifier: 9.7dBm at 82.5 GHz

(transferred-substrate HBT)

InGaAs-collector:
→ V_{br}=1.5 V → ***low power***

InP-collector:
→ V_{br}~5 V
→ *higher powers expected*



66 GHz HBT master-slave flip-flop

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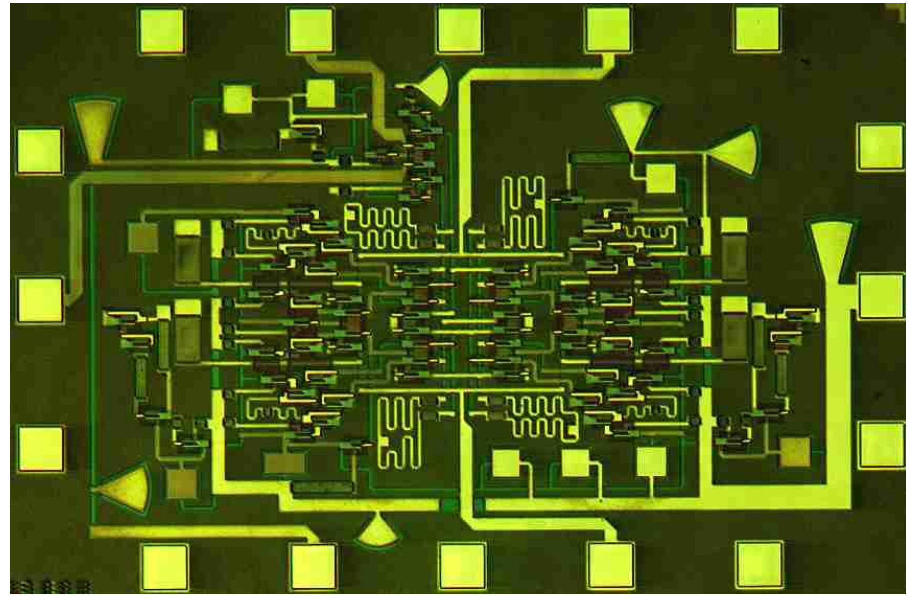
Michelle Lee

Objectives: 100 + GHz logic

Approach: transferred-substrate HBTs, microwave / digital design

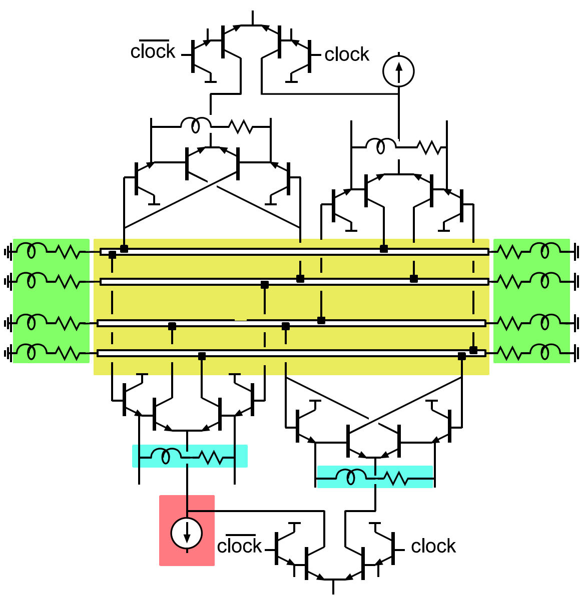
Simulations: 95 GHz clock rate in SPICE

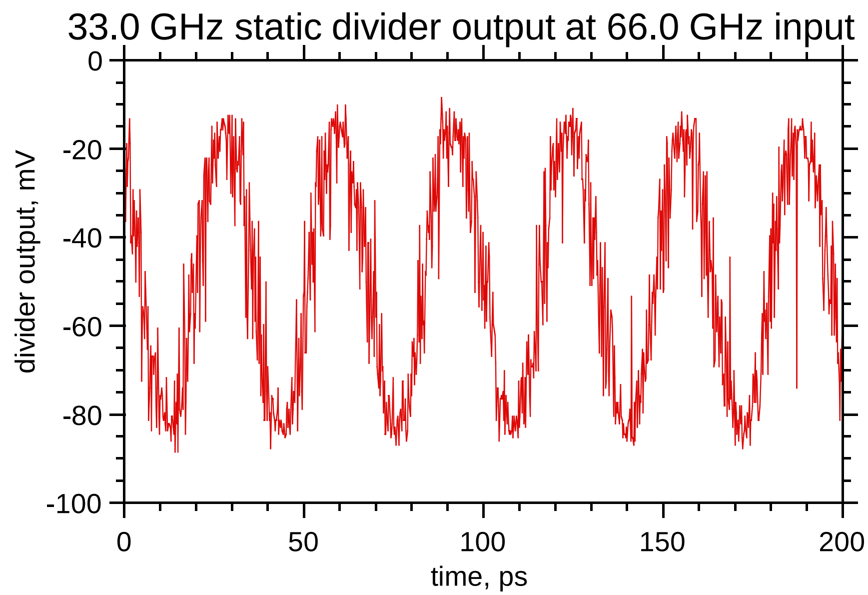
Accomplishments:
operation to 66 GHz



Design features:

- transmission-line bus short signal path
- inductive load
- emitter-follower damping
- keep-alive bias currents





3500-HBT 20 GHz Sine ~~ROM~~ ***WOM***

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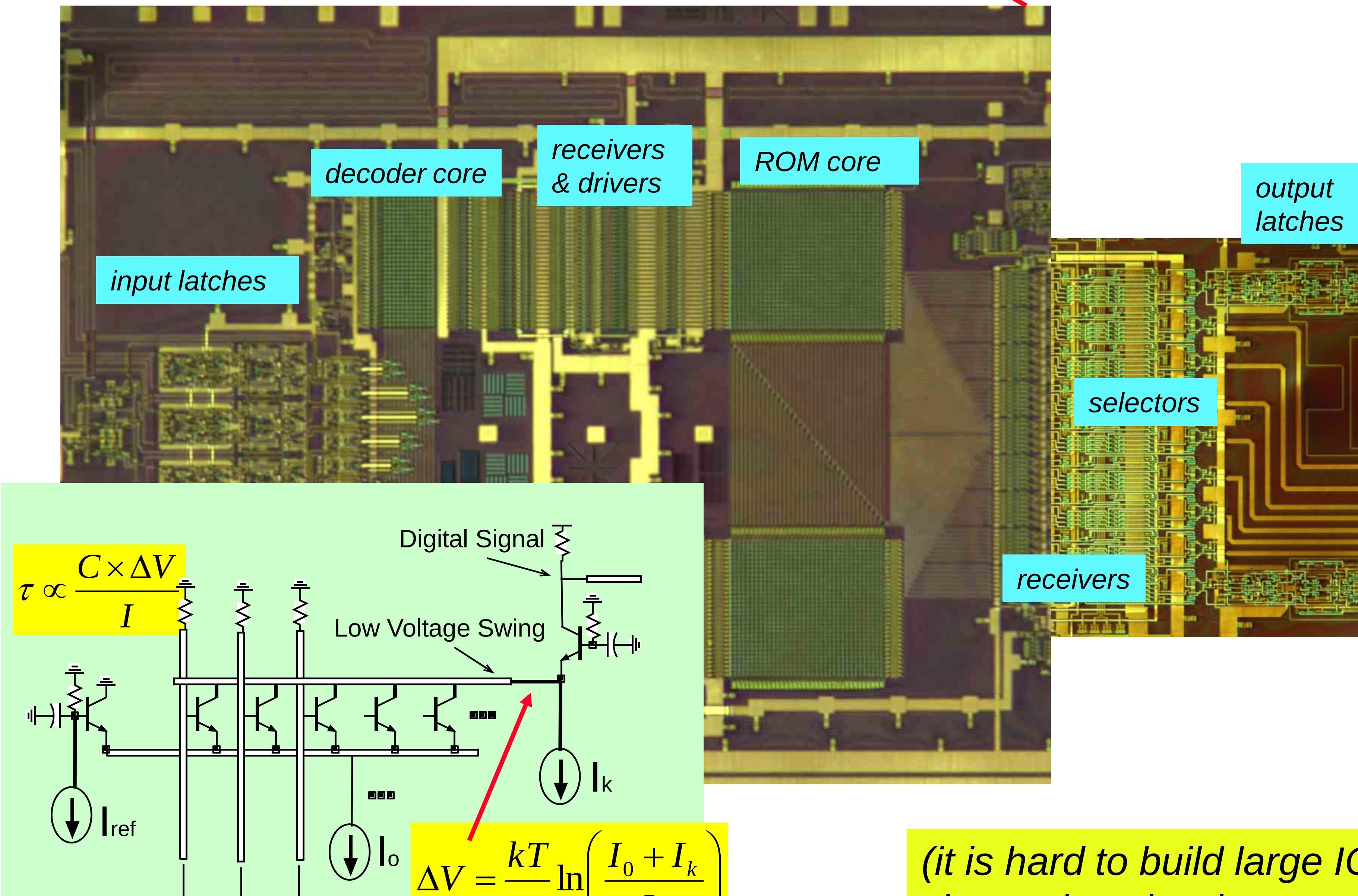
Yoram Betser



$$\tau \propto \frac{C \times \Delta V}{I}$$

$$\Delta V = \frac{kT}{q} \ln\left(\frac{I_0 + I_k}{I_o}\right)$$

(it is hard to build large ICs in a university cleanroom)

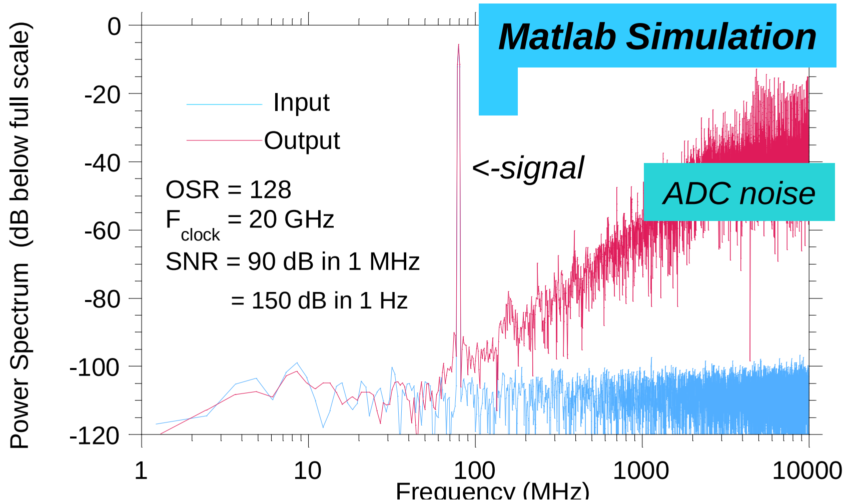
UCSB

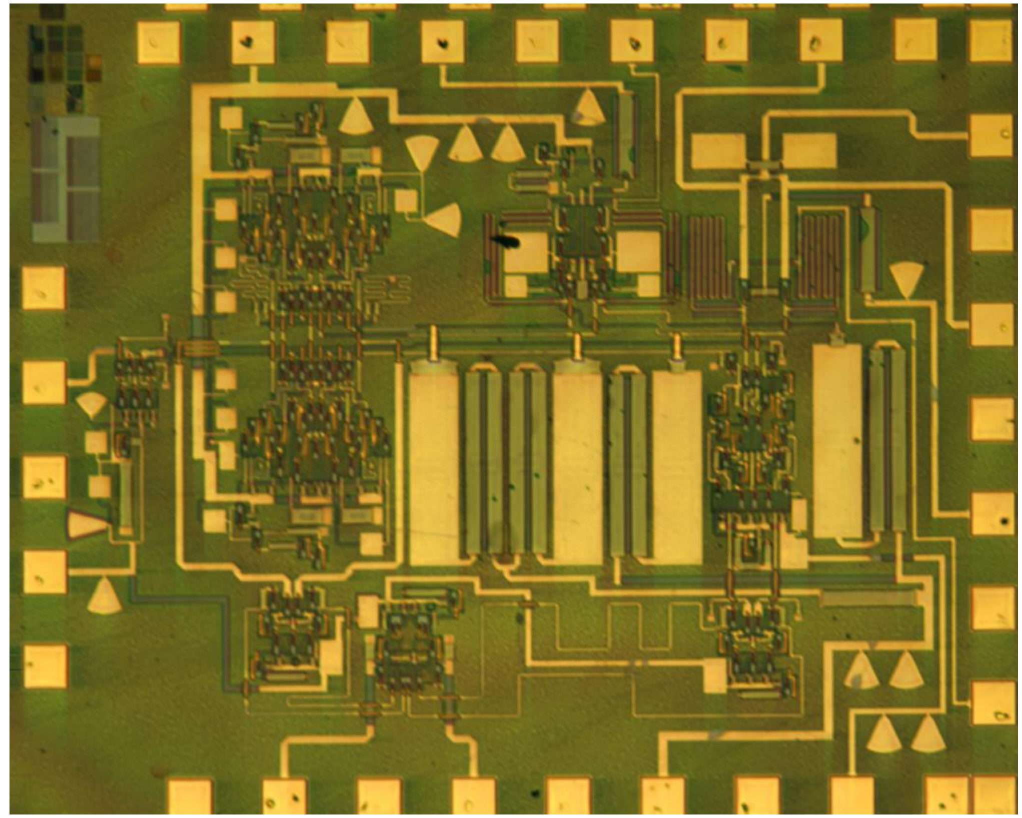
Shrinivasan Jaganathan

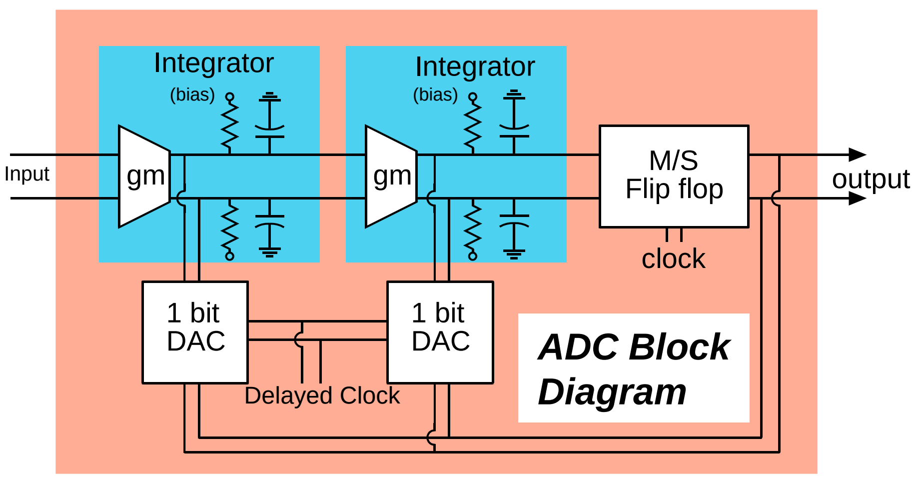
Delta-Sigma ADC

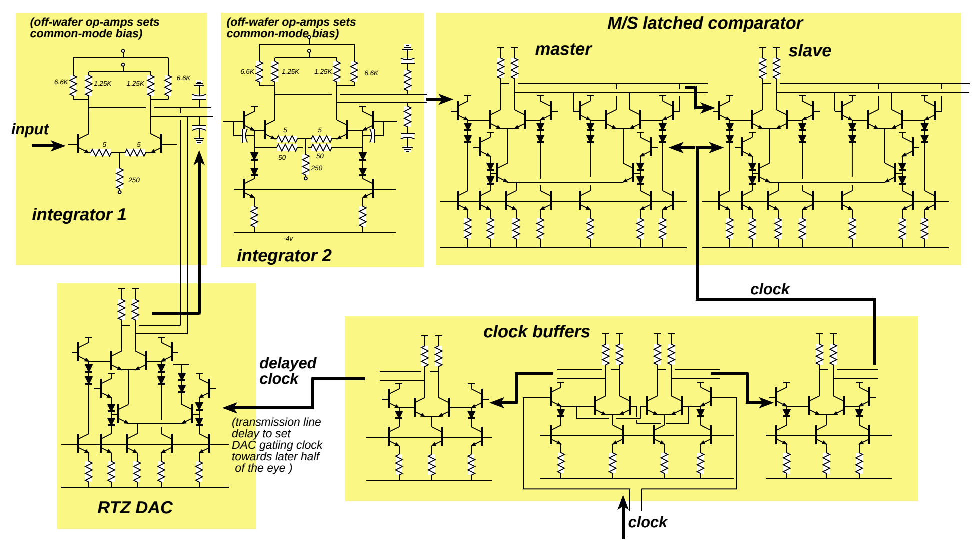
18 GHz clock rate   150 HBTs

6.2 ENOB for a 1 GHz signal
(2 GS/s equivalent Nyquist)



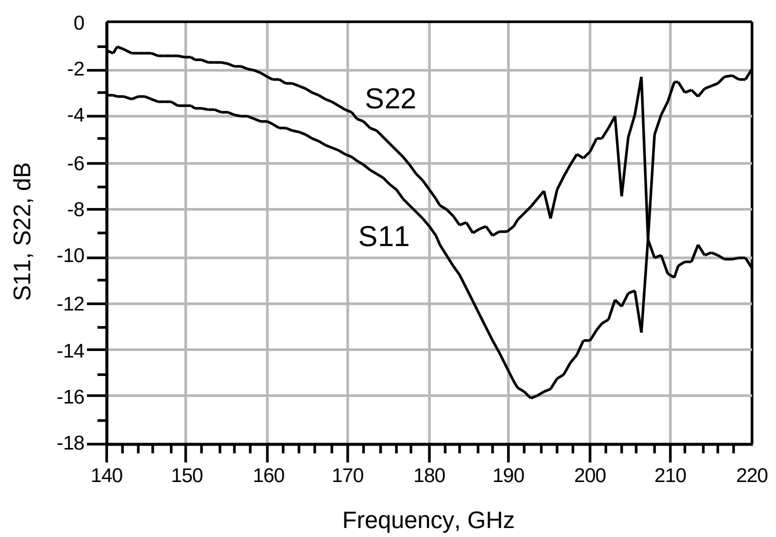


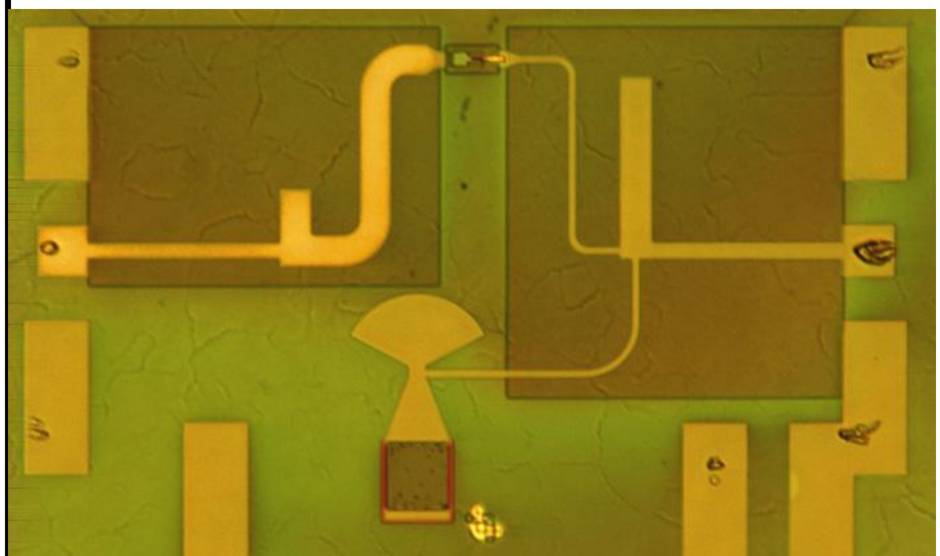


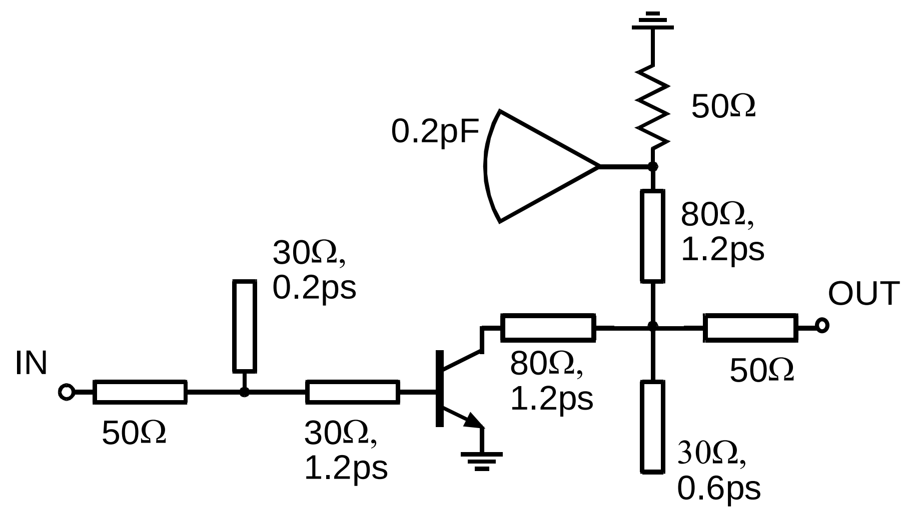


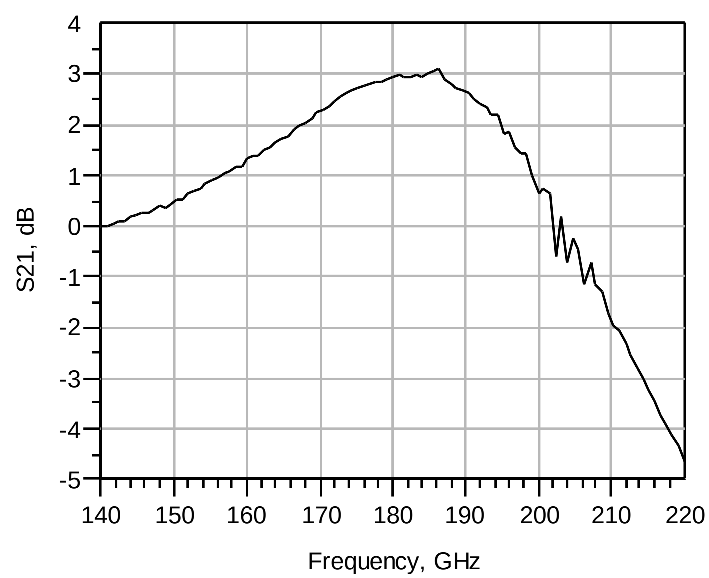
AFOSR 185 GHz HBT Amplifier UCSB

Miguel Urteaga









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19 GHz 2-bit adder

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Thomas Mathew