2001 International Conference on Indium Phosphide and Related Materials
Conference Proceedings
13th IPRM 14-18, May 2001 Nara, Japan

InP/InGaAs/InP DOUBLE HETEROJUNCTION BIPOLAR TRANSISTORS WITH 300 GHz F_{max}

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ABSTRACT

We report InP/InGaAs/InP Double Heterojunction Transistors(DHBTs) with high breakdown voltages in a substrate transfer process. A device with a 400 Å thick graded base, a 500 Å chirped superlattice base-collector grade and a 2500Å thick InP collector exhibits f_τ = 165 GHz and f_{max} = 300 GHz with breakdown voltage $BV_{CEO} = 6V$ at a current density, $J_e = 1 \cdot 10^5 A/cm^2$. A device with a 400 Å thick graded base, a 500 Å chirped superlattice base-collector grade and a 1500Å thick InP collector exhibits f_τ = 215 GHz and f_{max} = 210 GHz with breakdown voltage $BV_{CEO} = 4V$ at a current density, $J_e = 1 \cdot 10^5 A/cm^2$.

INTRODUCTION

Advances in device technology for heterojunction bipolar transistors (HBTs) are necessary to further improve the performance of associated high speed analogue and digital circuitry. The substrate transfer process has yielded InP based single heterojunction bipolar transistors (SHBTs) with outstanding cutoff frequencies [1]. However, SHBTs have low breakdown voltage and high output conductance limiting their use in high voltage and precision analog circuits. Higher breakdown voltages can be acheived by using a wide bandgap material such as InP as the collector. Efforts in this direction have resulted in impressive high frequency performance [2, 3]. Here, we report DHBTs fabricated in the substrate transfer process, a process that allows HBTs to be fabricated with narrow emitter/base and collector/base junctions on opposing sides of the base epitaxial layer.

LAYER STRUCTURE AND FABRICATION

The wafers were grown on Fe-doped semi-insulating (100) InP substrates at IQE, Inc. The layer structure is as shown in Table . The conduction band edge discontinuity (ΔE_c) at the base-collector heterointerface is removed by providing a linear bandgap variation for the interficial region [4] by using a chirped super lattice (CSL). Delta-doped layers are used at the ends of the base-collector grade to create a dipole that cancels the band offset. 0

Material	Doping(cm^{-3})	Thickness(nm)
nInGaAs	$1 \cdot 10^{19}$	100
nInGaAlAs	$1 \cdot 10^{19}$	20
nInP	$1 \cdot 10^{19}$	90
nInP	$8 \cdot 10^{17}$	30
nInGaAlAs	$8 \cdot 10^{17}$	23.3
nInGaAlAs	$2 \cdot 10^{18}$	6.6
pInGaAs	$4 \cdot 10^{19}$	40
nInAlGaAs	$1 \cdot 10^{16}$	48
nInP	$2 \cdot 10^{18}$	2
nInP	$1 \cdot 10^{16}$	250
nInGaAs	$1 \cdot 10^{19}$	75
nInAlAs	*UID*	250

The period of the superlattice for the base-collector grade is 1.5nm. From a material growth perspective, the InP/InGaAs CSL is much more difficult to grow than the InAlAs/InGaAs CSL due to the interficial strain that builds up as a result of the inter-mixing of group-V elements at the interface.

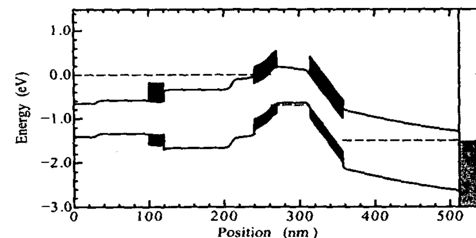

Fig. 1: Band diagram, under bias, of a typical device

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So, all-arsenide(InAlAs/InGaAs) CSLs have been used to grade all the heterointerfaces.

The emitter and base layers are grown at a lower temperature to reduce Beryllium outdiffusion during and after the growth of the base. Base grading is accomplished by increasing the temperature of the gallium cell after each 50 Å step of base growth to give a progressively wider bandgap $In_xGa_{1-x}As$ composition. The composition of InGaAs in the base-emitter grade is the same as that at the bsae emitter edge. The base layer and the base-emitter grade are therefore strained. The band diagram for a typical device with this layer structure is shown in Fig. 1.

After the emitters are defined, selective wet etch processes are used to define the base-emitter junction and the base mesa [5]. The active junction is then passivated and planarized using polyimide. The substrate transfer process commences with deposition of the PECVD Si_3N_4 insulator layer and the benzocyclobutene(BCB) transmission-line dielectric. Thermal and electrical vias are etched in the BCB. The wafer is electroplated to metalize the vias and to form the ground plane. Subsequently, the wafer is indium-bonded to a GaAs carrier substrate and the InP substrate removed in HCl. InGaAs stop-etch layers are used to prevent the substrate etch from removing the InP collector. Schottky collectors are then deposited, completing the process.

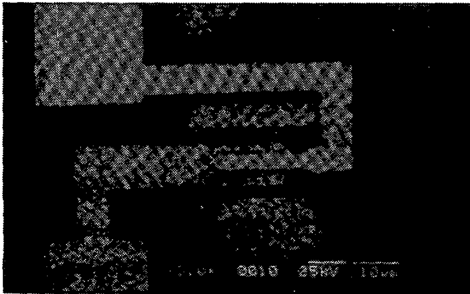

Fig. 2: Scanning Electron Micrograph of a completed transistor

A substrate transfer process of this nature allows HBTs to be fabricated with narrow emitter/base and collector/base junctions on opposing sides of the base epitaxial layer. Reducing the emitter and collector widths progressively reduces $R_{bb}C_{cb}$, resulting in a rapid increase in f_{max} with scaling. The layers can subsequently be thinned to obtain high values of both f_τ and f_{max}. Fig. 2 shows the Scanning Electron Micrograph of a completed transistor with a 1×8 μm^2 emitter contact and a 1.6 μm^2 collector contact.

RESULTS AND DISCUSSION

DC performance

Fig. 3 shows typical common-emitter characteristics for a 1×8 μm^2 emitter contact device with a 2000 Å collector depletion layer thickness at low current densities. The transistors demonstrate a common-emitter current gain $\beta = 40$ with a breakdown voltage, $BV_{CEO} > 6V$. The DC offset voltage is ~ 0.3 V and is due to the barrier in the schottky contact. Transistors fabricated with ohmic collectors exhibited a lower offset voltage of ~ 0.15 V. Transistors with a 3000 Å thick collector depletion layer thickness demonstrate similar current gain with a breakdown voltage, $BV_{CEO} > 9V$.

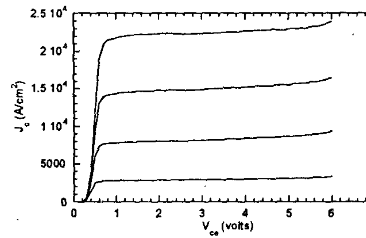

Fig. 3: $I_c - V_{ce}$ characteristics at low current densities, I_B is in steps of $15mA$

FIg. 4 shows the DC I-V characteristics at higher current densities. The maximum power density, before device failure , is found to be $4 \cdot 10^5 W/cm^2$. For devices with 3000 Å collector depletion layer thickness, the maximum power density before device failure is found to be $6 \cdot 10^5 W/cm^2$.

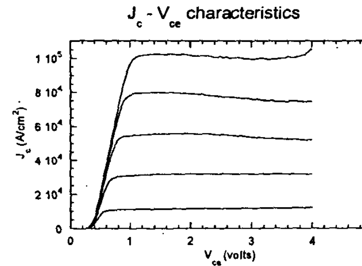

Fig. 4: $I_c - V_{ce}$ characteristics at high current densitites, I_B is in steps of $50mA$

Microwave performance

The devices were characterised by measuring the S-parameters on wafer using a 75-110 GHz network analyzer. The current gain(h_{21}) and the power(U) gain are extrapolated at -20 dB/decade to obtain the two figures of merit, f_τ, the current gain cutoff frequency and f_{max}, the maximum frequency of oscillation.

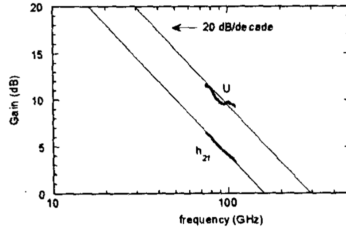

Fig. 5: RF gains for a DHBT with a 1×8 μm^2 emitter contact. This device has a 400 Å thick graded base and a 3000 Å thick collector depletion region.

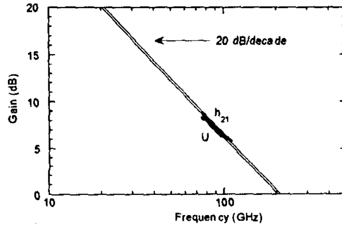

Fig. 6: RF gains for a DHBT with a 1×8 μm^2 emitter contact. This device has a 400 Å thick graded base and a 2000 Å thick collector depletion region.

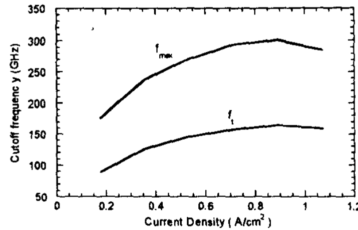

Fig. 7: Variation of f_τ and f_{max} with bias; $V_{CE} = 2.5V$

Fig. 5 shows h_{21} and U for one such device at a bias of $V_{CE} = 2.5V$ and $J_e = 9 \cdot 10^4 A/cm^2$. By extrapolating this data at -20dB/decade, the device is found to exhibit an $f_\tau = 165$ GHz and an $f_{max} = 300$ GHz. The device had a 3000 Å thick collector depletion layer. Devices with a 2000 Å thick collector depletion layer exhibit an $f_\tau = 215$ GHz and an $f_{max} = 210$ GHz.h_{21} and U for one such device at a bias of $V_{CE} = 1.5V$ and $J_e = 1 \cdot 10^5 A/cm^2$ are shown in Fig. 6. Fig. 7 and Fig. 8 show the variation of f_τ and f_{max} with J_E and V_{CE}.The V_{CE} is maintained at 2.5 V for the first plot and J_E is maintained at $6 \cdot 10^4 A/cm^2$ for the second plot. The drop in the cutoff frequencies at high current densities is due to the Kirk effect and at high V_{CE} is due to intervalley scattering in the collector.

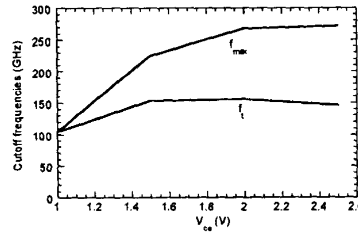

Fig. 8: Variation of f_τ and f_{max} with bias; $J_e = 6 \cdot 10^4 A/cm^2$

CONCLUSIONS

InP/InGaAs/InP DHBTs have been demonstrated in a substrate transfer process. A peak f_{max} of 300 GHz was obtained for a device with 1×8 μm^2 emitter contact dimensions, a 400 Å thick graded base and a 3000Å thick collector depletion region. The breakdown voltage, BV_{CEO} was found to be $\sim 6V$ at a current density, $J_e = 1 \cdot 10^5 A/cm^2$.A device with a a 400 Å thick graded base and a 2000Å thick collector depletion region exhibits an $f_\tau = 215$ GHz and $f_{max} = 211$ GHz. The breakdown voltage, BV_{CEO} was found to be $\sim 4V$ at a current density, $J_e = 1 \cdot 10^5 A/cm^2$. With further scaling, higher values of f_τ and f_{max} should be possible. The Kirk threshold density is found to be low and can be improved by increasing the collector doping. Experiments in this regard are in progress.

Acknowledgments: This work was supported by ONR under grant N00014-01-1-0066. The guidance of Dr. S. Jaganathan, now at GTran Inc., is gratefully acknowledged.

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