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2-BIT ADDER CARRY AND SUM LOGIC CIRCUITS CLOCKING AT 19 GHZ CLOCK FREQUENCY IN TRANSFERRED SUBSTRATE HBT TECHNOLOGY

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Abstract

We report carry and sum circuits for a 2-bit adder. The 2-bit adders are designed to be part of a pipelined 2N-bit adder-accumulator. The ICs clock at a maximum of 19 GHz and were fabricated in InAlAs/InGaAs transferred substrate HBT technology. To obtain high clock rates in a design with multiple gate delays, we have employed a novel merged AND-OR logic structure using 4-level series-gated current-steering logic. Further, this logic is merged with the synchronizing latch circuit so as to minimize the overall gate delay. The 2-bit carry circuit has 250 transistors, a maximum clock frequency of 19 GHz, and dissipates 1.2 W. The sum logic circuit of a full adder was realized as a 4-level series-gated ECL XOR gate. This circuit has a maximum clocking frequency of 24 GHz, has 150 transistors and dissipates 750 mW.

I. Introduction

Direct digital frequency synthesizers (DDFS) offer several advantages over phase locked loop (PLL) based synthesizers in commercial frequency hopped communication systems, radars, and radar jamming applications [1,2]. The advantages include precise frequency control, fast and phase continuous frequency switching, and excellent temperature and aging stability [1,2]. The block diagram of a DDFS system is shown in fig. 1. A digital signal processor (DSP) outputs a digital phase increment word $\Delta\phi(t)$, which is added to the existing phase value $\phi(t)$ in the accumulator. The adder-accumulator (phase accumulator) outputs the digital phase word $\phi(t+\Delta t)$ which addresses a sine ROM. The output of the sine ROM is the digital word representing $\sin \phi(t+\Delta t)$. The D/A converter converts the digital word corresponding to $\sin \phi(t+\Delta t)$ to its analog form.

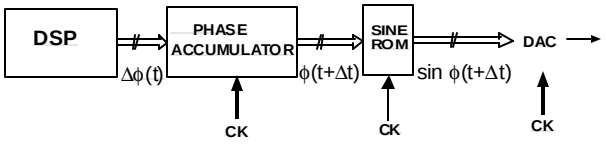

Fig. 1: Simplified block diagram of a DDFS system.

The frequency tuning range of DDFS systems is from dc to ~ ($f_{ck\ max}$ /3), where $f_{ck\ max}$ is the maximum clock frequency of operation [3]. The frequency resolution is given by $\Delta f = f_{ck}/ 2^N$, where N is the phase accumulator digital word width [3]. This work focuses on increasing the maximum clocking rate of the adder-accumulator. Fast sine ROM and DAC's are other significant DDFS design challenges.

II. Adder-accumulator architecture

The carry and sum logic circuit discussed in this paper form the building blocks of a 2N-bit pipelined adder-accumulator. A 8-bit pipelined adder-accumulator architecture is shown in fig. 2. Pipelining the inputs to the adder allows one to trade latency for maximum clocking frequency. Latency is defined as the time delay between a change at the input end and the resulting change in the output. The inputs of the adder-accumulator are delayed in increments of the clock period. Correspondingly, the outputs are also delayed to realign the outputs in time. The maximum clocking frequency of the 2-bit adder is limited by the carry propagation delay. The next section details the design of the carry and sum logic circuits.

III. 2-bit adder circuit design

The sum and carry logic realization for a full adder is shown in Fig. 3 [3]. A_0 and B_0 are the 2 adder inputs and C_{in} is the carry input to a full adder. The sum (S_0) logic can be realized using a 3-input XOR gate. The carry (C_{out}) generation requires an AND-OR logic

operation (fig. 3). Hence the carry logic circuit sees two gate propagation delays (i.e. $T_{pd\ carry} = 2\ T_{gate}$) whereas the sum logic circuit sees a single gate delay.

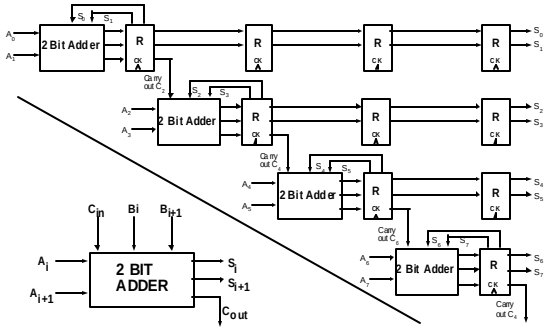

Fig. 2: Block diagram of an 8-bit pipelined adder

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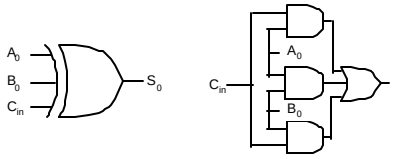

Fig. 3: Sum and carry logic realization in a full adder.

The full adder implementation is extended to realize the 2-bit adder block shown in fig. 4. Latches are needed at the outputs of the 2-bit adder for pipelining the carry bit and realigning the outputs in time. The latched sum output bits are fed back as input to the adder to perform the add and accumulate function. As is evident from fig. 4, the carry logic circuit is the critical delay path and limits the maximum clock frequency. Circuit simulations indicate that the maximum clock frequency for the carry logic circuit to be approximately 23 GHz.

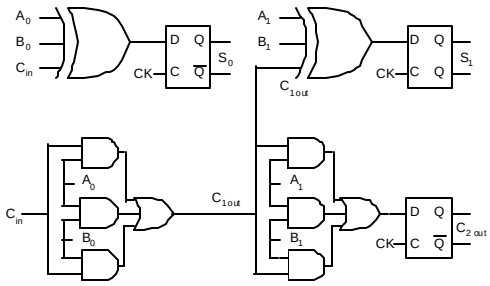

Fig. 4: Typical implementation of a 2-bit adder. In the case of an adder-accumulator, $B_i = S_i$.

The AND-OR logic required to generate the carry bit can be realized as a single 3-level series-gated ECL logic gate. This is shown in fig. 5. The carry logic realized using this AND-OR logic gate shows a 40% improvement in clocking speed as compared to the earlier approach. A further increase in clock speed can be achieved by merging the master-slave latch and the AND-OR logic gate, resulting in a 4-level series-gated structure shown in fig. 6. Simulations indicate that this approach provides a 40 GHz clock rate, which is a further 48% improvement. The block diagram of the 2-bit adder carry logic is shown in fig. 6. Fig. 7 shows the sum logic circuit realized by merging the 3-input XOR gate and the master-slave latch. The circuit diagrams are shown in fig.11 and fig.12.

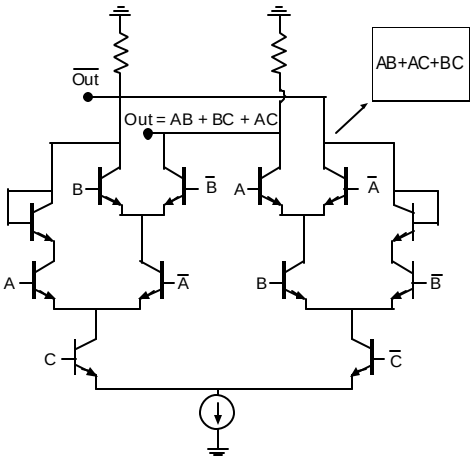

Fig. 5: Circuit diagram of the 3- level series-gated AND-OR gate that generates the carry output.

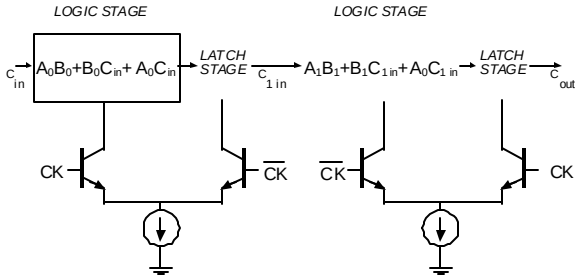

Fig. 6: Carry logic realized by merging the AND-OR gate with the synchronizing latch.

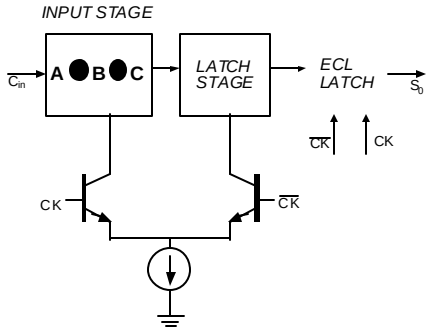

Fig. 7: Sum logic realized by merging the XOR gate with the master-slave latches.

IV. InAlAs/InGaAs transferred substrate HBT technology

Transferred substrate HBT technology has demonstrated excellent RF performance with peak f_t and f_{max} of about 300 GHz and 800 GHz respectively [4,5]. Circuits fabricated in this technology include small signal amplifiers, flip flops configured as frequency dividers, and oversampled A/D converters [6,7].

The process starts with process steps similar to that of mesa HBT processes. The process steps include emitter and base metallization, emitter/base mesa isolation, junction passivation and interconnect metallization. After front side processing, Benzocyclobutene (BCB) is spun on the wafer, and gold ground plane plating is carried out. The InP wafer is then inverted and bonded on to a GaAs carrier wafer and the InP substrate is then removed to contact the collector layer. The wafer cross section after bonding is shown in fig. 8. The presence of a continuous gold ground plane provides for a low dielectric constant microstrip wiring environment. The ability to lithographically define the collector contacts directly opposite to the emitter leads to significantly lower collector-base capacitance as compared to triple-mesa HBT processes.

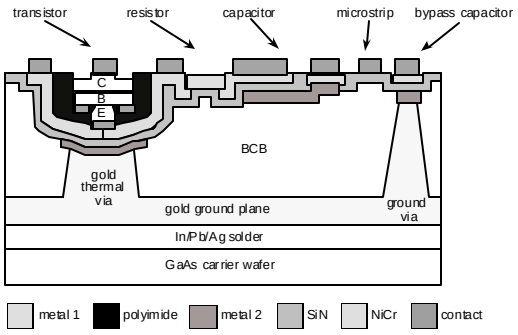

Fig. 8: Cross section of a transferred substrate HBT wafer after bonding.

V. Measurements and results

The chip photograph of the carry and sum logic circuits fabricated are shown in fig. 9 and fig. 10. HBTs with 3.0 x 1.0 μm^2 emitter and 4.0 x 2.0 μm^2 collectors were used. These transistors exhibited an f_t and f_{max} of 170 GHz and 180 GHz respectively at V_{ce} = 1.0 V and J_e = 1.0 mA/μm^2. DC measurements indicated a current gain β of approximately 5 to 6. These transistors can operate at a peak current density of 1.5 mA/μm^2 and a V_{ce} < 1.5V. The low current gain was due to problems associated with base band gap grading during the epitaxial growth.

The circuit diagram of the fabricated 2-bit adder carry logic circuit is shown in fig 11. Fig. 12 shows the sum logic circuit diagram. For testing purposes the circuits were configured as static frequency dividers. This involved setting the inputs to either logic high or logic low and feeding back the carry/sum outputs appropriately. This is indicated in fig. 11 and fig. 12, and was realized on chip using resistors and current sources. The clock input was applied to the circuits and the maximum clocking speed for a divide by two operation was determined. The carry logic circuit exhibited a maximum clocking rate of 19 GHz and the sum logic had a maximum clock rate of 24 GHz. The output waveforms measured on an oscilloscope are shown in fig. 13 and fig. 14.

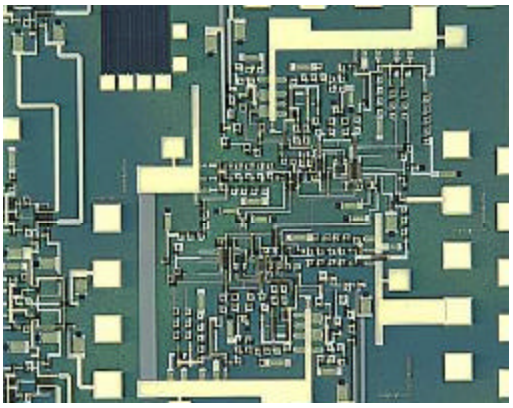

Fig. 9: Chip photograph of the carry logic circuit.

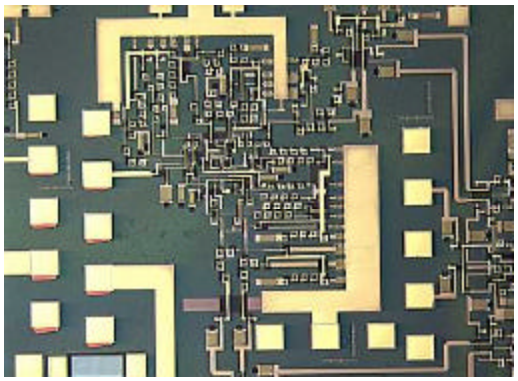

Fig. 10: Chip photograph of sum logic circuit.

VI. Conclusion

A new 3-level series-gated current-steering logic to realize the carry logic of a full adder was presented. The carry logic gate was then merged with the synchronizing latches to improve the clock rate in a pipelined adder-accumulator application. The 2-bit adder carry logic and sum circuits were fabricated in InAlAs/InGaAs transferred substrate HBT technology and had maximum clocking frequencies of 19 GHz and 24 GHz respectively. It is likely that the low current gains (β ~5-6) led to reduced frequency of operation. Simulations indicate that clock frequencies of 40 GHz should be possible.

VII. Acknowledgement

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VIII. Bibliography and references

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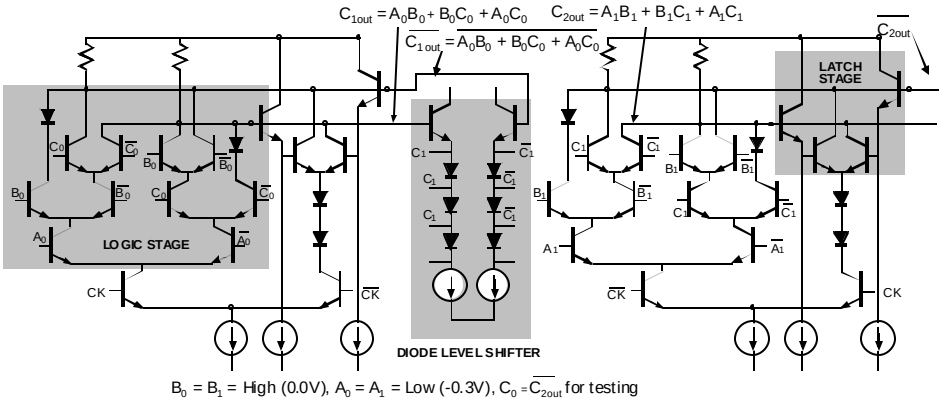

Fig. 11: 2-bit adder carry logic circuit.

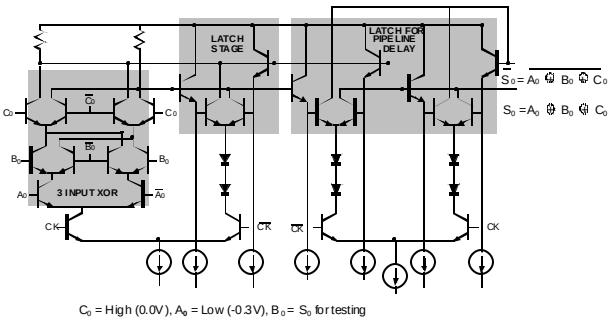

Fig . 12: Sum logic circuit with latches at the output

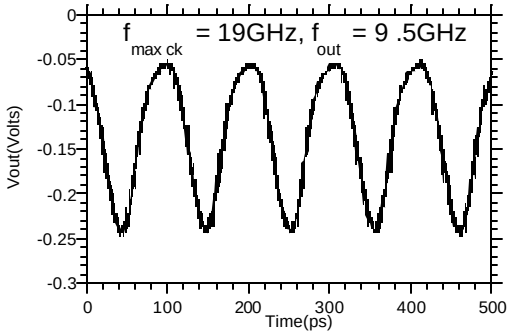

Fig. 13: Output waveform of the carry logic circuit for a 19 GHz clock input.

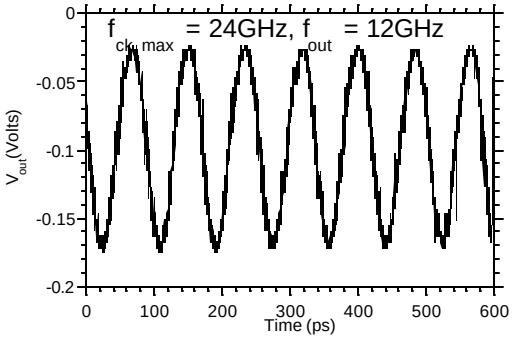

Fig.14: Output waveform of the sum logic circuit for a 24 GHz clock input.