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560 GHz f_t, f_{max} InGaAs/InP DHBT in a novel dry-etched emitter process

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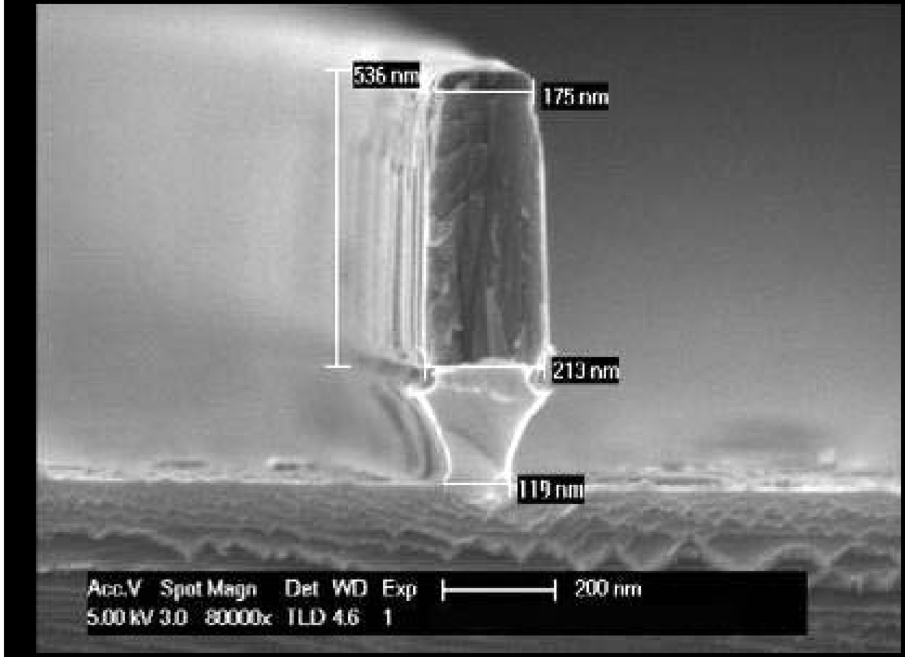
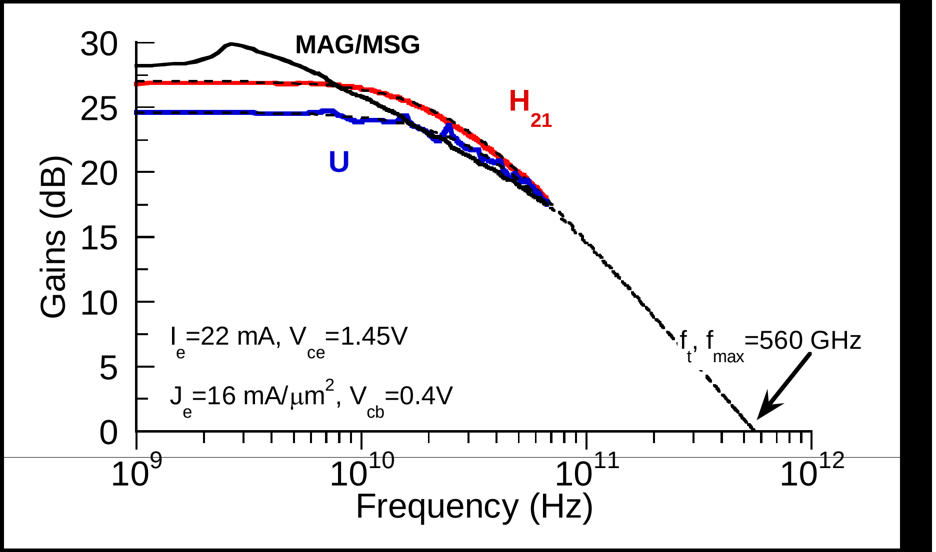
Latest UCSB DHBT w/ refractory emitter metal

New refractory metal emitter technology

250 nm emitter width





Scalable below 128 nm width

First RF results

Simultaneously 560 GHz f_t & f_{max}

BVceo = 3.3V

Standard figures of merit / Effects of Scaling

Small signal current gain cut-off frequency (from H_{21})

$$\frac{1}{2\pi f_{\tau}} = \boxed{\tau_{b} + \tau_{c}} + \frac{nk_{B}T}{qI_{c}}\left(C_{je} + \boxed{C_{cb}}\right) + \left(R_{ex} + R_{c}\right)\boxed{C_{cb}}$$

Thinning epitaxial layers (*vertical scaling*) reduces base and collector transit times… But increases capacitances

Power gain cut-off frequency (from U)

$$f_{\max} \cong \sqrt{\frac{f_{\tau}}{8\pi R_{bb,eff} C_{cb,eff}}}$$

Reduce R_{bb} and $C_{cb,}$ through *lateral* scaling

Charging time for digital logic

$$\tau \propto \frac{C_{cb}}{I_{c}} \Delta V$$

More efficient heat transfer

$$\Delta T \cong \frac{J_{e} W_{e} V_{ce}}{\pi K_{InP}} \ln\left(\frac{L_{e}}{W_{e}}\right) + \cdots$$

What parameters are needed for THz HBTs?

emitter	500	250	**125** nm width	✓
	16	9	**4** $\Omega\cdot\mu m^2$ access ρ	✓
base	300	150	**75** width,	✓
	20	10	**5** $\Omega\cdot\mu m^2$ contact ρ	✓
collector	150	100	**75** nm thick,	✓
	5	10	**20** $mA/\mu m^2$ current density	✓
	5	3.5	**3** V, breakdown	✓
f_τ	400	500	**700** GHz	
f_{max}	500	700	**1000** GHz	
power amplifiers	250	350	**500** GHz	
digital clock rate (static dividers)	160	230	**330** GHz	

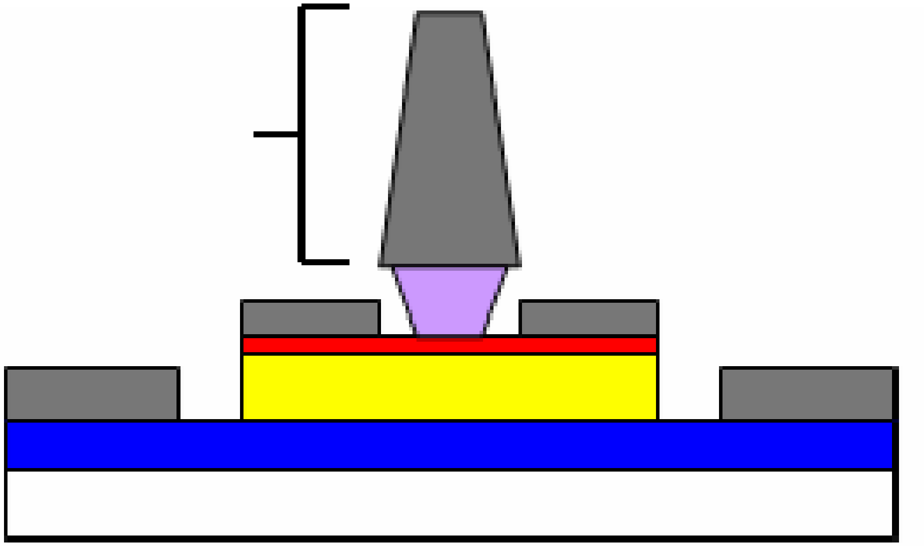
ρ_c<1 $\Omega\mu m^2$ U. Singisetti DRC 2007

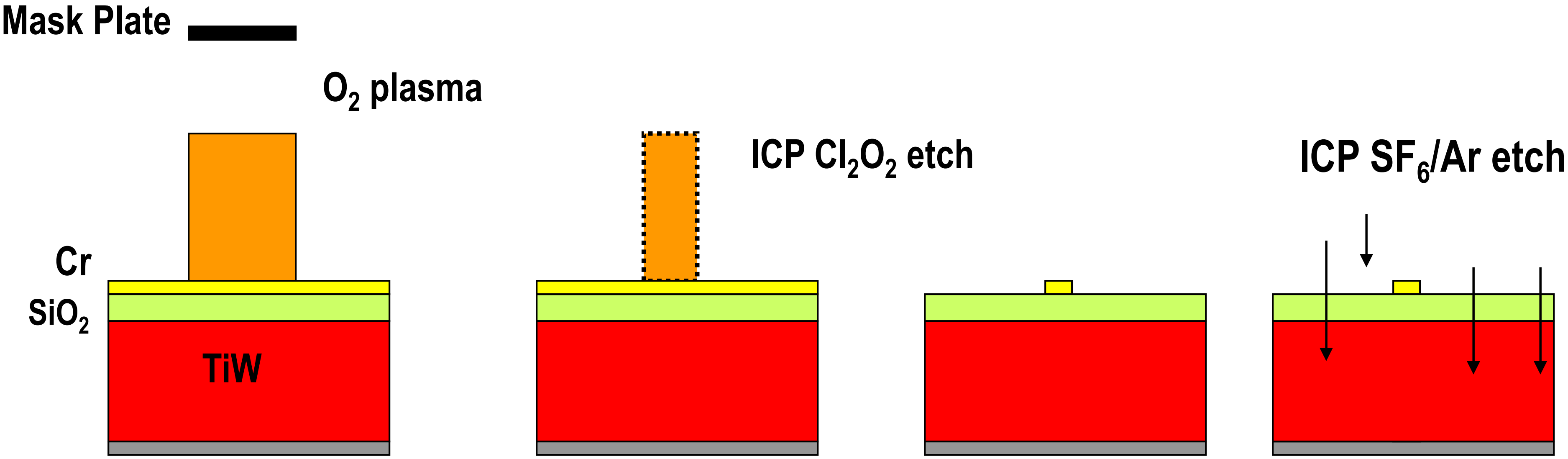
Ohmic contacts and epitaxial scaling good for 64nm HBT node!

Develop technology suitable for aggressive lateral scaling

TiW emitter dry etch formation

- ***Lift-off no good at <300 nm!***
- ***Dry etching – very high aspect ratio***
- ***Optical Lithography***

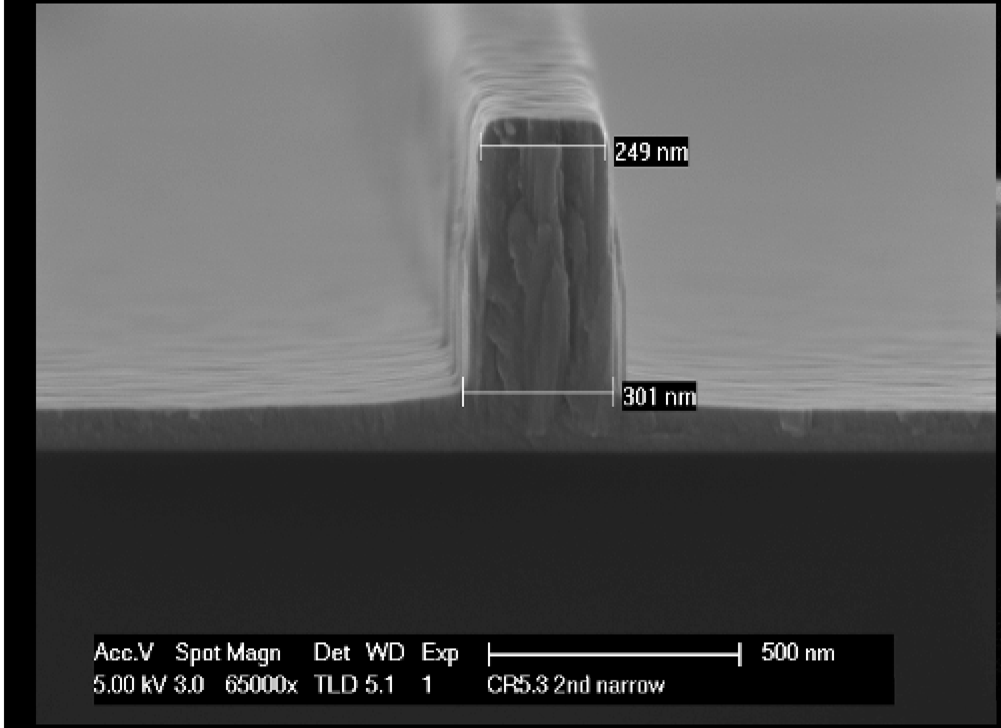


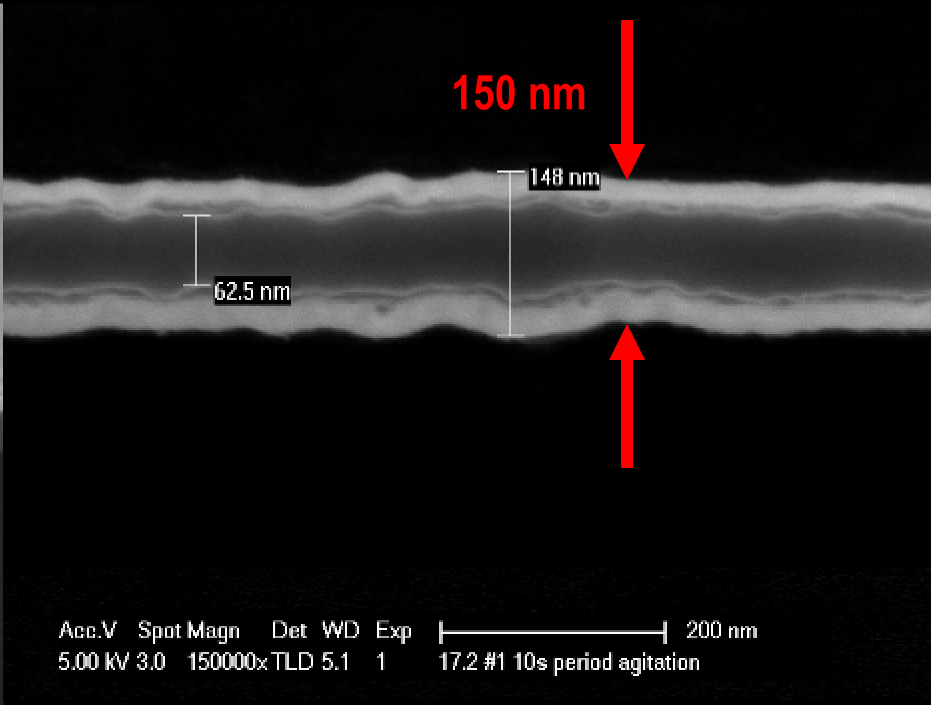


- Refractory $Ti_{0.1}W_{0.9}$ is thermally stable
- $\rho_c < 1\Omega/$Om^2 possible – no degradation of contact resistance for anneals up to 400C

TiW dry etching results

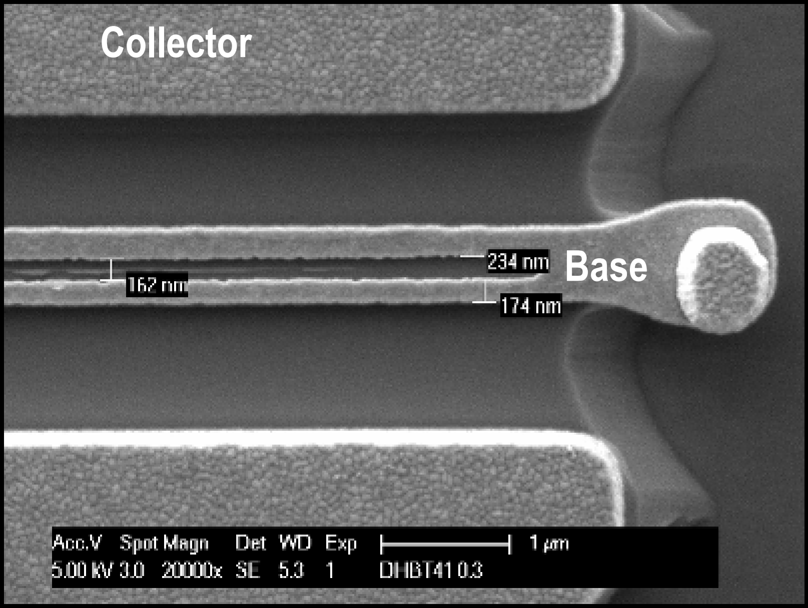
- 250-300 nm emitters routinely formed
- Demonstrated scalability down to 150 nm
- ~ 50-100 nm tapering during etch sets scaling limit

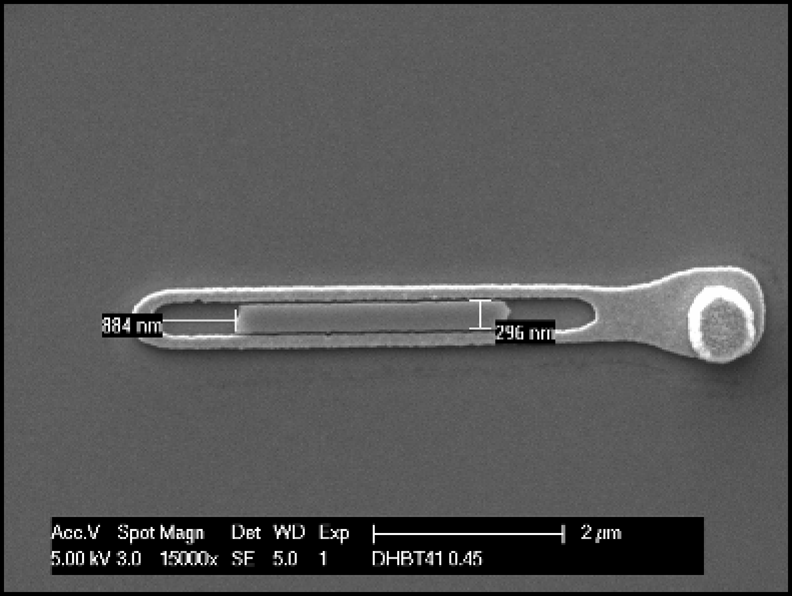


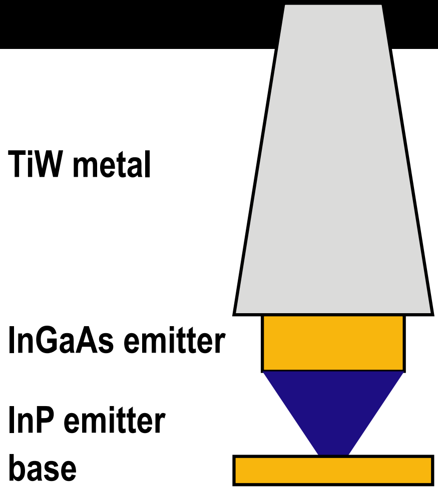


- Emitter metal height ~ 500-600 nm

Wet etch does not scale



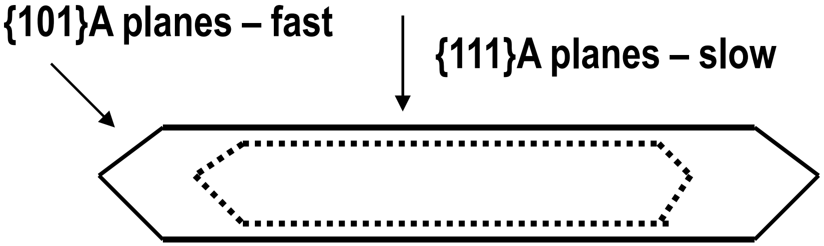




Minimum emitter width ~ 150 nm!

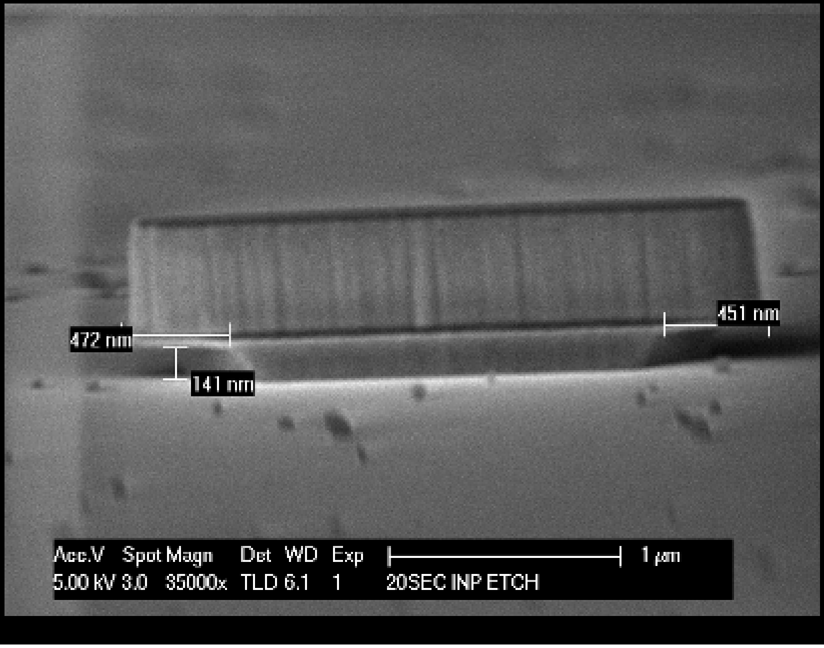
InGaAs etch ~ 30-40n

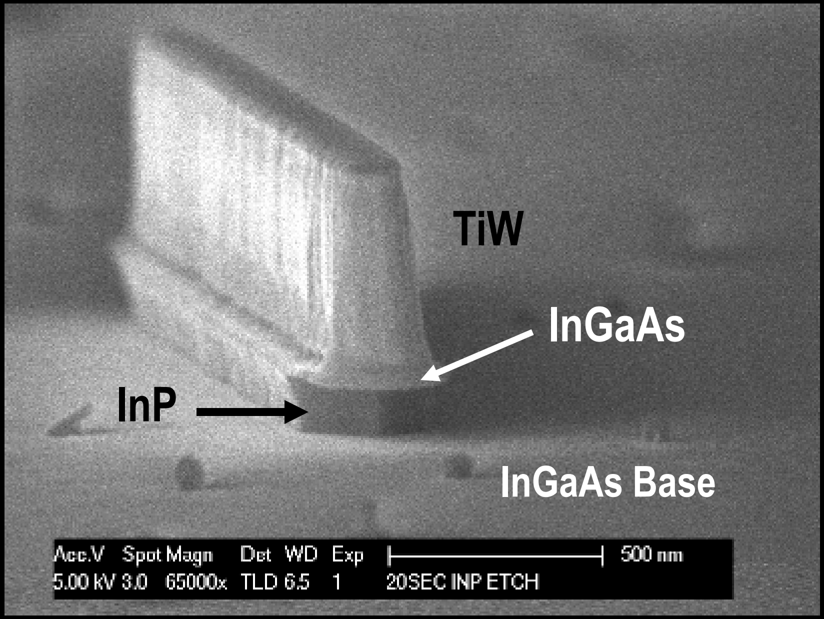
InP etch ~ 40 nm



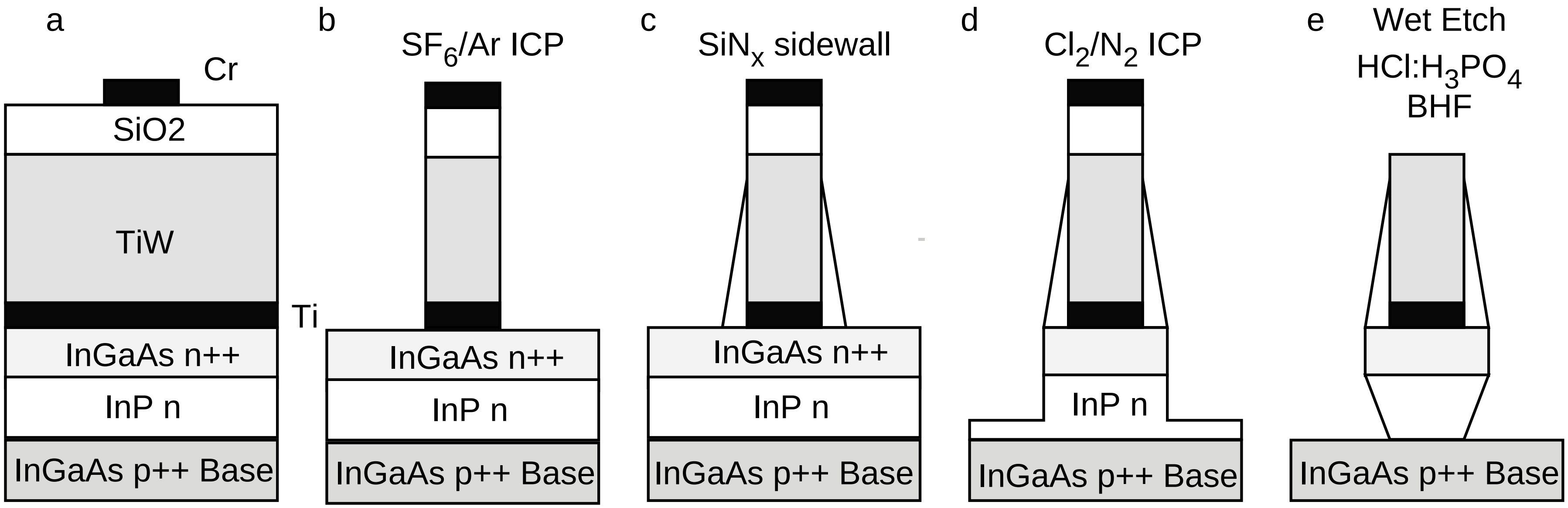
Hybrid dry/wet etch

- Anisotropic dry etch InGaAs, part of InP emitter, Cl_2N_2
- Formidable problem – $InCl_x$ formation
- Extensive UCSB know how on dry etching
- Solution – low power ICP etch @ 200C, low Cl_2 concentration
- Short InP wet etch

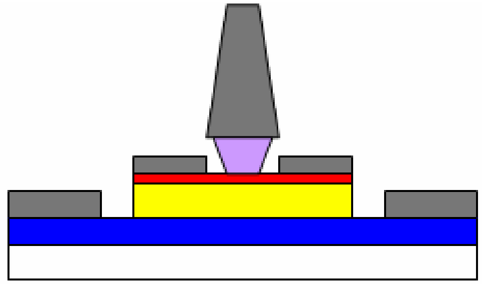




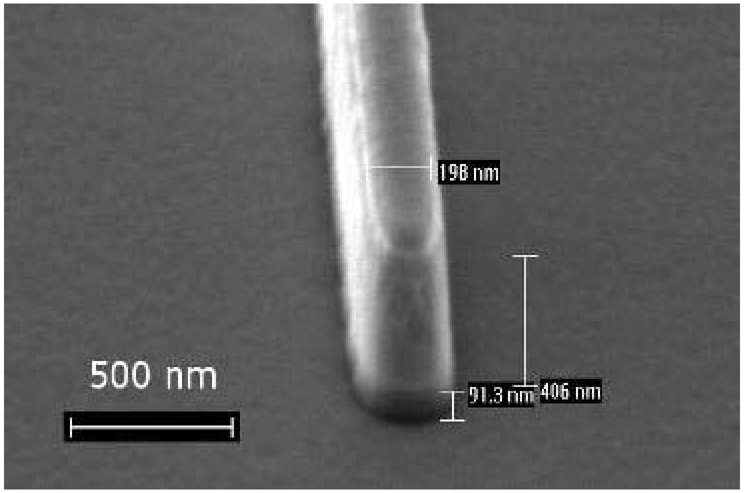
Current UCSB TiW emitter process



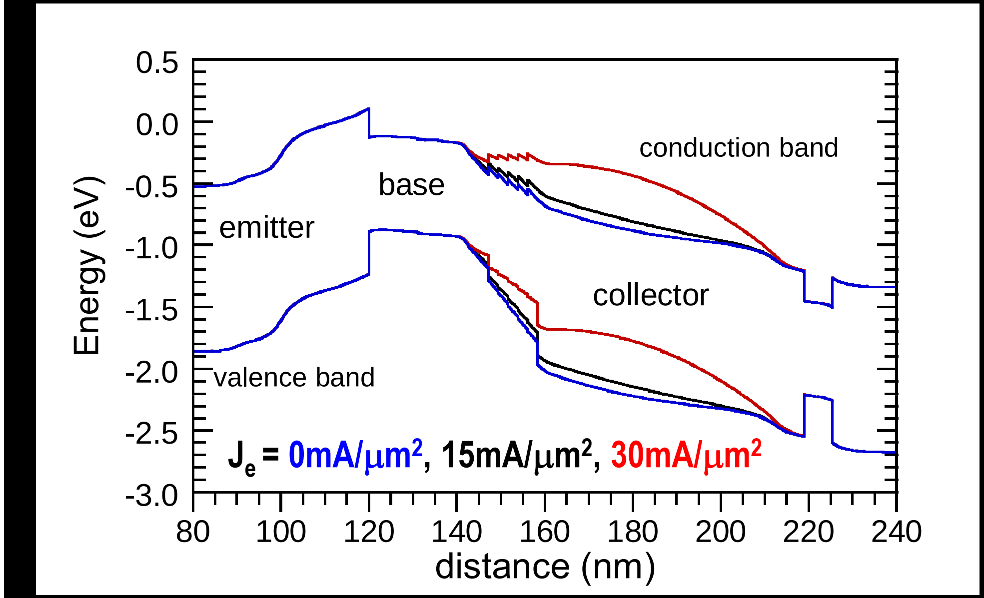
- 5 nm Ti layer for improved adhesion
- 25 nm SiN$_x$ sidewalls protects Ti/TiW during Cl$_2$ and BHF etch, improves adhesion
- Standard triple mesa
- BCB pasivation



Emitter prior to InP wet etch



Layer structure -- 70 nm collector DHBT



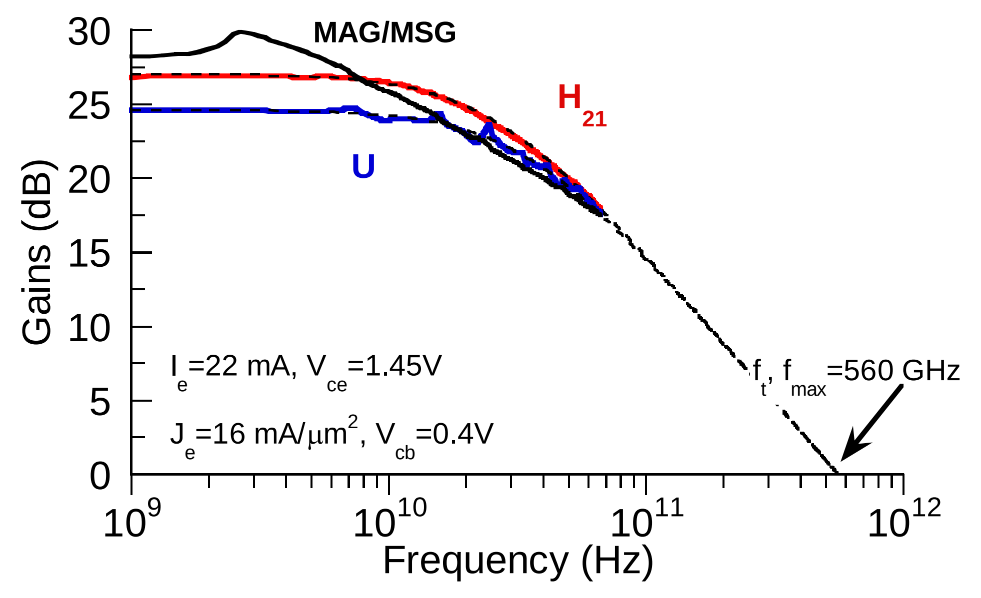
V_{be} = 1.0 V, V_{cb} = 0.0 V

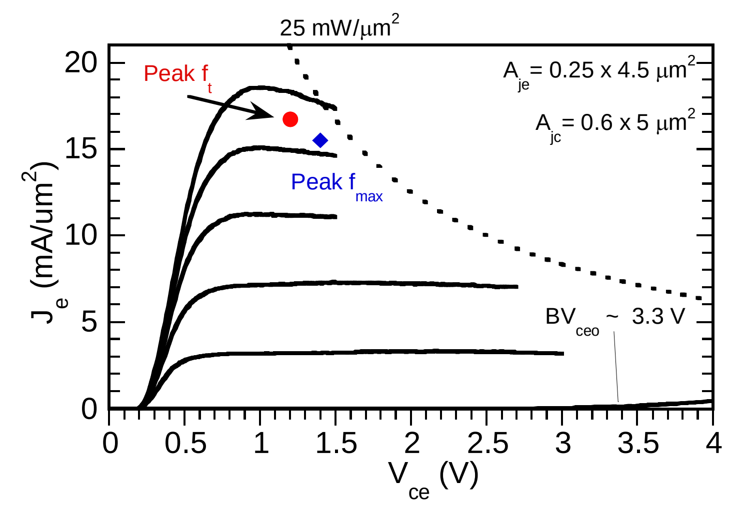
Thickness (nm)	Material	Doping cm^{-3}	Description
30	$In_{0.53}Ga_{0.47}As$	$5\cdot10^{19}$: Si	Emitter cap
10	$In_{0.53}Ga_{0.47}As$	$4\cdot10^{19}$: Si	Emitter
60	InP	$3\cdot10^{19}$: Si	Emitter
10	InP	$1.2\cdot10^{19}$: Si	Emitter
20	InP	$1.0\cdot10^{18}$: Si	Emitter
22	**InGaAs**	**$5\text{-}9\cdot10^{19}$: C**	**Base**
5.0	**$In_{0.53}Ga_{0.47}$ As**	**$2\cdot10^{17}$: Si**	**Setback**
11	**InGaAs / InAlAs**	**$2\cdot10^{17}$: Si**	**B-C Grade**
3	**InP**	**$6.2\cdot10^{18}$: Si**	**Pulse doping**
51	**InP**	**$2\cdot10^{17}$: Si**	**Collector**
5	InP	$1\cdot10^{19}$: Si	Sub Collector
5	$In_{0.53}Ga_{0.47}$ As	$2\cdot10^{19}$: Si	Sub Collector
300	InP	$2\cdot10^{19}$: Si	Sub Collector
Substrate	SI : InP		

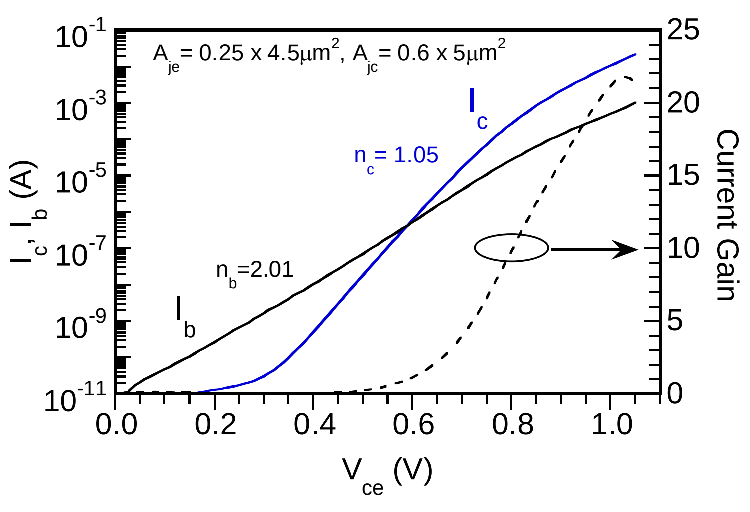
Objective:

- Thin collector and base for decreased electron transit time
- Collector doping designed for high Kirk threshold, designed for 128 nm node
- Setback and grade thinned for improved breakdown

RF & DC data –70 nm collector, 22 nm base InP Type-I DHBT







Emitter width ~ 250 nm

First reported device with f_t, f_{max} > 500 GHz

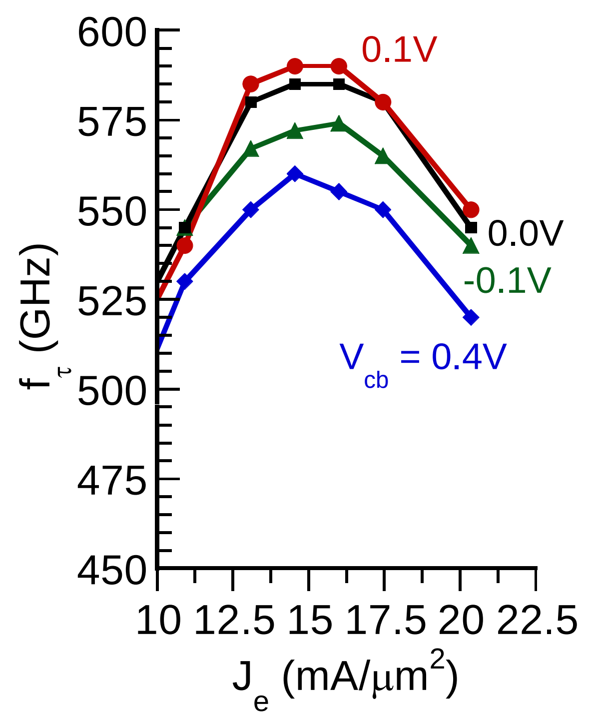
BV_{CEO} ~ 3.3 V, BV_{CBO} = 3.9 V ($J_{e,c}$ = 15kA/cm^2)

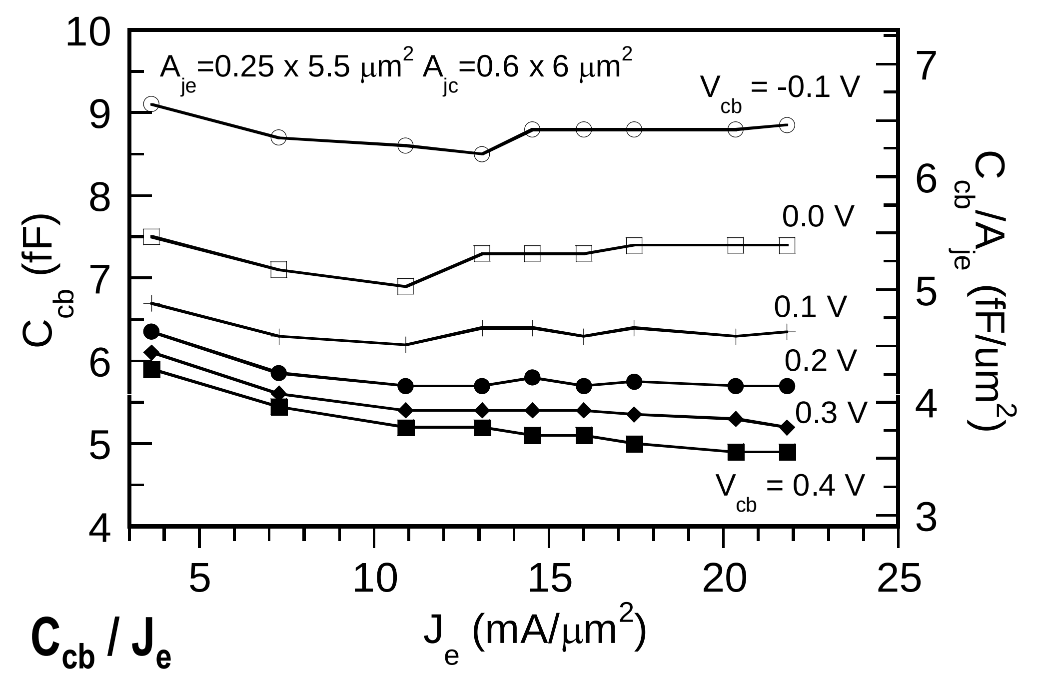
Emitter contact (from RF extraction), $R_{cont} < 5\ \Omega\cdot\mu m^2$

Base: R_{sheet} = 780 Ω/sq, R_{cont} ~ 15 $\Omega\cdot\mu m^2$

Collector: R_{sheet} = 11.1 Ω/sq, R_{cont} ~ 10.1 $\Omega\cdot\mu m^2$

RF data –70 nm collector, 22 nm base InP Type-I DHBT



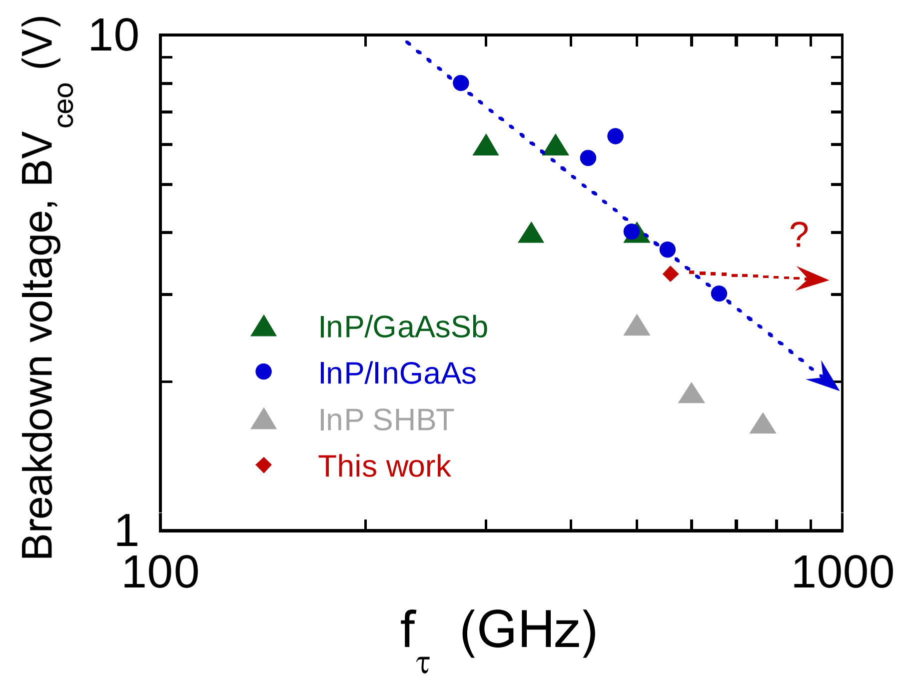


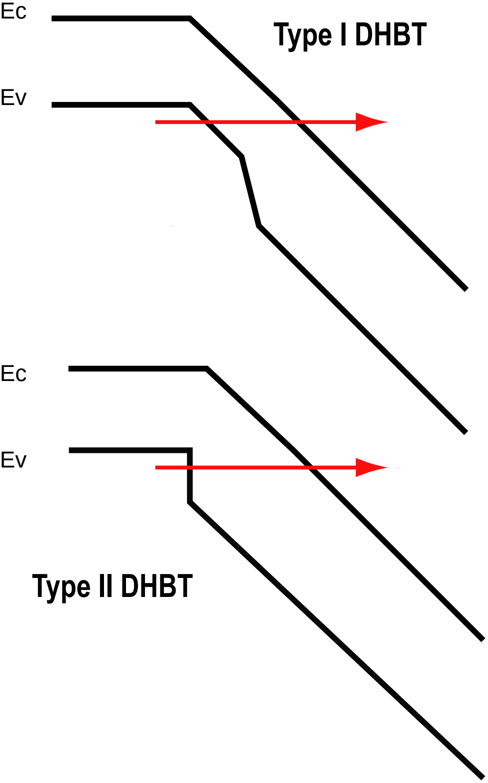
- No detectable increase in C_{cb} for high J_e
- Indicates that Kirk threshold is not reached
- Device performance limited by self heating?
- Further scaling needed for better thermal performance!

$$-\frac{\partial C_{cb}}{\partial I_c} = \frac{\partial}{\partial I_c}\left(\frac{\partial Q_{b+c}}{\partial V_{cb}}\right) = \frac{\partial}{\partial V_{cb}}\left(\frac{\partial Q_{b+c}}{\partial I_c}\right) = \frac{\partial \tau_f}{\partial V_{cb}}$$

→ *Kirk effect increases C_{cb}*
...even in DHBTs

Breakdown performance of InP HBTs



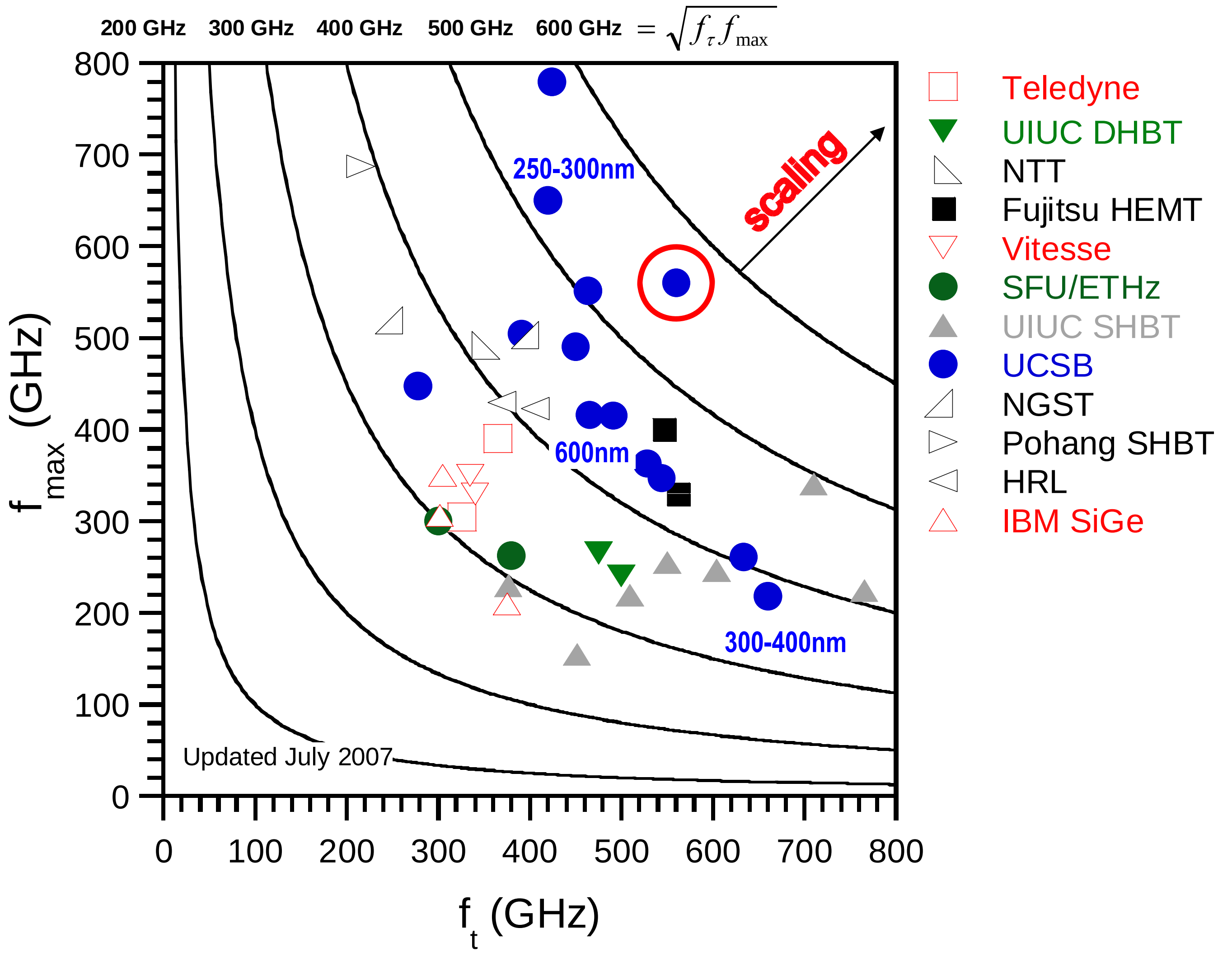


Type I DHBT and Type II DHBT – similar BV_{ceo}

Type II DHBTs has low f_{max} due to base resistance

SHBT have substantially lower breakdown

Current status of fast transistors



popular metrics :

f_τ or $f_{\max}$ alone

$(f_\tau + f_{\max})/2$

$\sqrt{f_\tau f_{\max}}$

$(1/f_\tau + 1/f_{\max})^{-1}$

much better metrics :

power amplifiers:

PAE, associated gain,

mW/μm

low noise amplifiers:

$F_{\min}$, associated gain,

digital:

f_{clock}, hence

$(C_{cb}\Delta V / I_c)$,

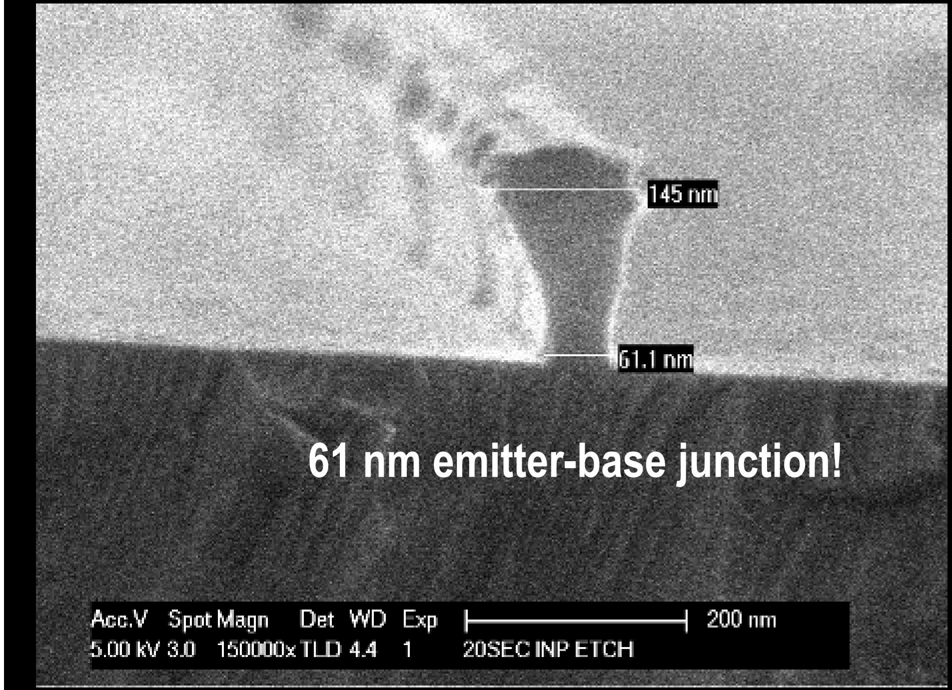
$(R_{ex} I_c / \Delta V)$,

$(R_{bb} I_c / \Delta V)$,

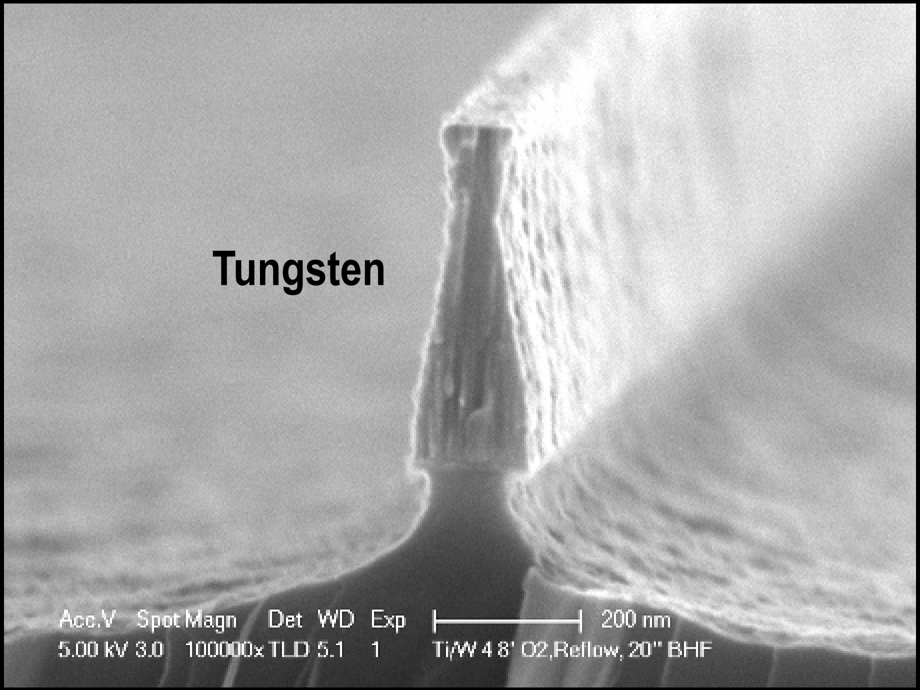
$(\tau_b + \tau_c)$

Emitter Process will scale to 128 nm & below

- Emitter-base junction has been scaled down to 64 nm
- Pure W emitter- no tapering



61 nm emitter-base junction!



Emitter metal peeled off during cross section cleave..

Conclusion

- HBTs @ 128 nm node→ 700 GHz ft, xx GHz fmax feasble
  challenges: contact resistivity, robust deep submicron processes
- Dry etch based DHBT emitter process → sub 100 nm junctions feasible
- First RF results: 250nm junctions: simultaneous f_t,f_{max} ~ 560 GHz
- 125 nm devices should come soon !
- … THz before next DRC?

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