Indium Phosphide and Related Materials Conference 2007

Sub-300nm InGaAs/InP Type-I DHBTs with a 150nm collector, 30nm base demonstrating 755GHz f_{max} and 416GHz f_{τ}

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Standard figures of merit / Effects of Scaling

Small signal current gain cut-off frequency (from H_{21})

$$\frac{1}{2\pi f_\tau} = \boxed{\tau_b + \tau_c} + \frac{nk_BT}{qI_c}\left(C_{je} + \boxed{C_{cb}}\right) + \left(R_{ex} + R_c\right)\boxed{C_{cb}}$$

Thinning epitaxial layers (*vertical scaling*) reduces base and collector transit times... But increases capacitances

Power gain cut-off frequency (from U)

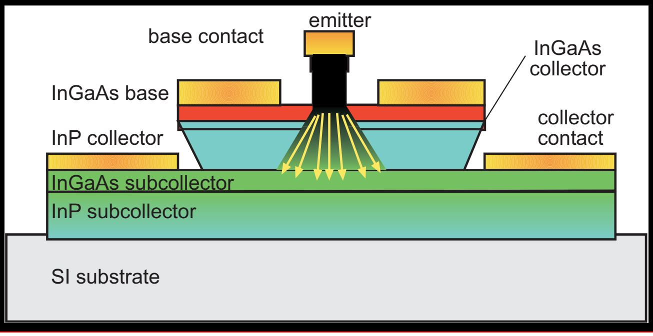
$$f_{\max} \cong \sqrt{\frac{f_\tau}{8\pi R_{bb,eff} C_{cb,eff}}}$$

Reduce R_{bb} and $C_{cb,}$ through *lateral* scaling

Charging time for digital logic

$$\tau \propto \frac{C_{cb}}{I_c}\Delta V$$

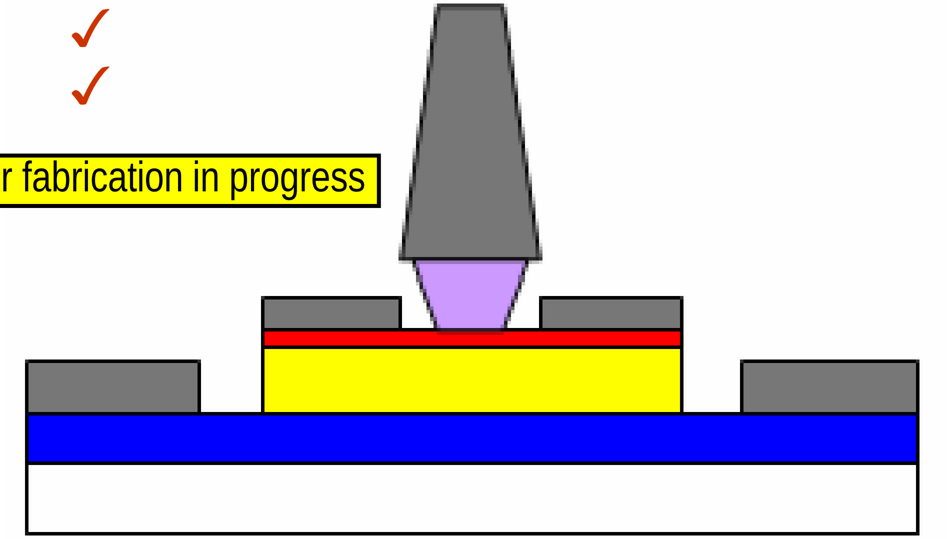
Higher J_{kirk}, dimished self-heating due to current increased current spreading



2006: 250 nm Scaling Generation, 1.414:1 faster

emitter	500	250 nm width		✓
	16	$9\ \Omega\cdot\mu m^2$ access ρ		✓
base	300	150 width,		✓
	20	$10\ \Omega\cdot\mu m^2$ contact ρ		✓
collector	150	100 nm thick,		✓
	5	$10\ mA/\mu m^2$ current density		✓
	5	3.5 V, breakdown		✓
f_τ	400	500 GHz	(416 GHz)	✓
f_{max}	500	700 GHz	(755 GHz)	✓
power amplifiers	250	350 GHz		
digital clock rate (static dividers)	160	230 GHz		

Designs and / or fabrication in progress



Temperature Rise: Transistor, Substrate, Package

cylindrical heat flow near junction

spherical flow for $r > L_e$

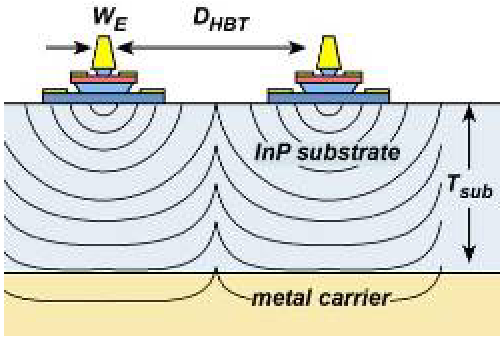
planar flow for $r > D_{HBT}/2$

$$\Delta T_{\text{substrate}} \cong \frac{P}{\pi K_{InP} L_E}\ln\left(\frac{L_e}{W_e}\right) + \frac{P}{\pi K_{InP}}\left(\frac{1}{L_E}-\frac{1}{D}\right) + \frac{P}{K_{InP}}\cdot\left(\frac{T_{sub}-D/2}{D^2}\right)$$

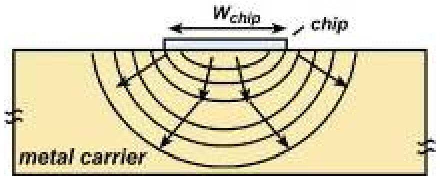
increases logarithmically

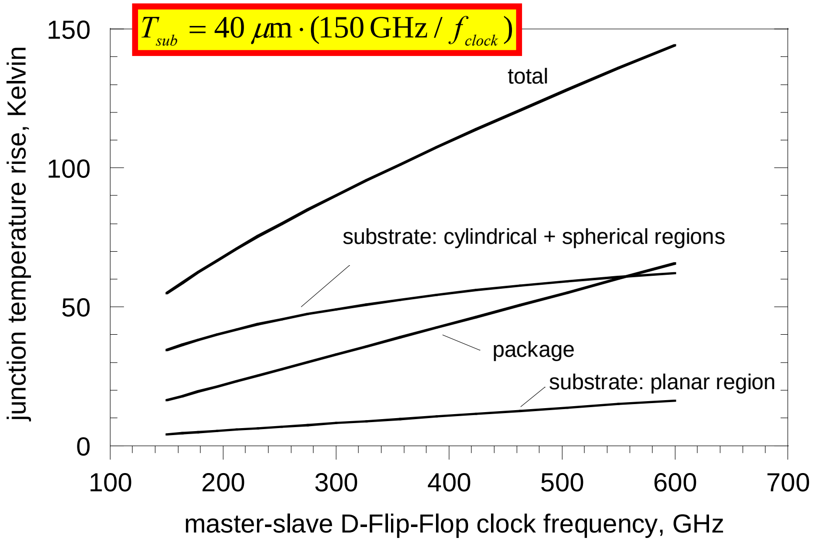
insignificant variation

increases quadratically if T_{sub} is constant

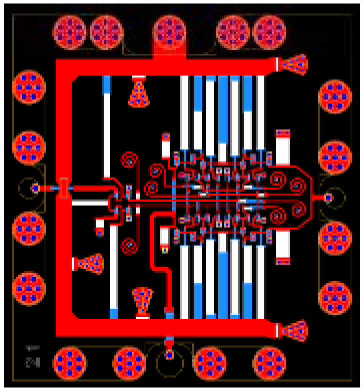


$$\Delta T_{package} \cong \left(\frac{1}{\pi}+\frac{1}{2}\right)\frac{P_{chip}}{K_{Cu} W_{chip}}$$



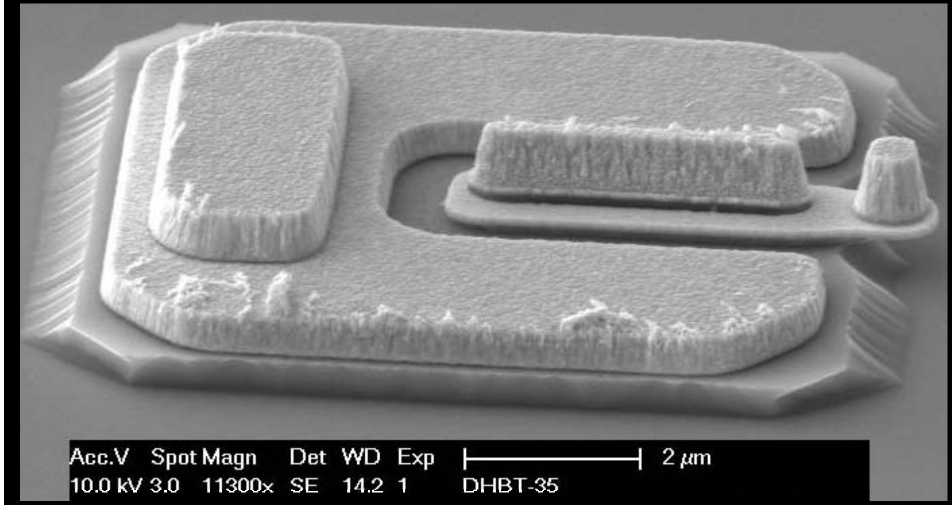


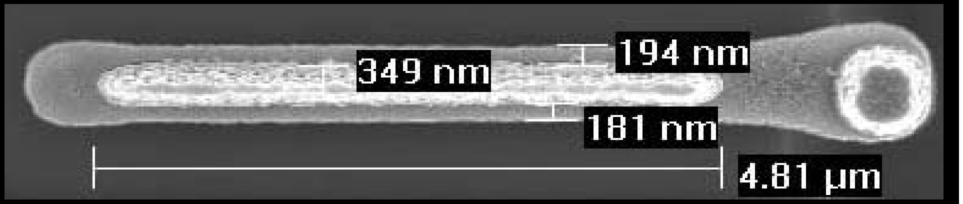
$T_{sub} = 40\,\mu\text{m}\cdot(150\,\text{GHz}/f_{clock})$

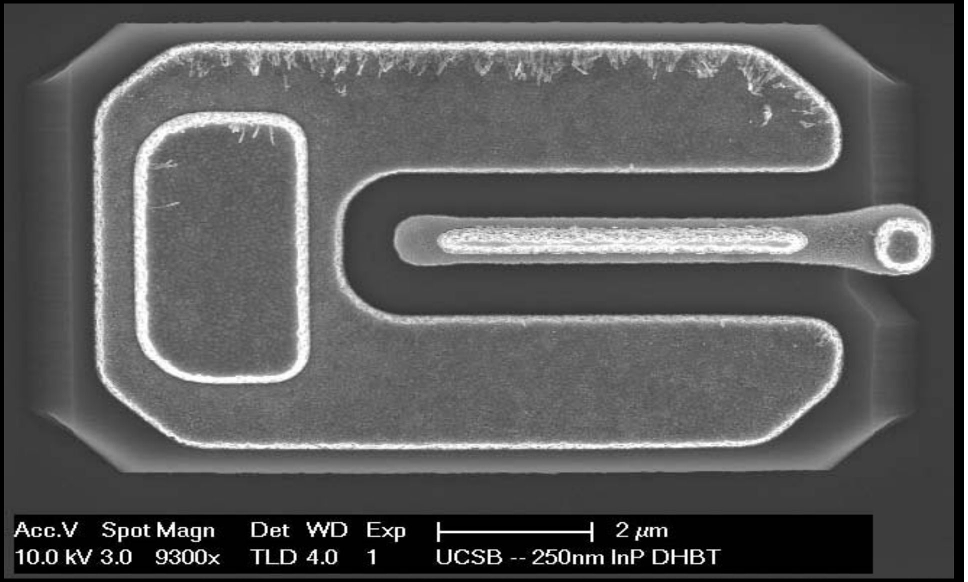


Wiring lenghts, clock rates, power densities, etc. scaled from demonstrated 150 GHz digital ICs

250 nm scaling generation DHBTs







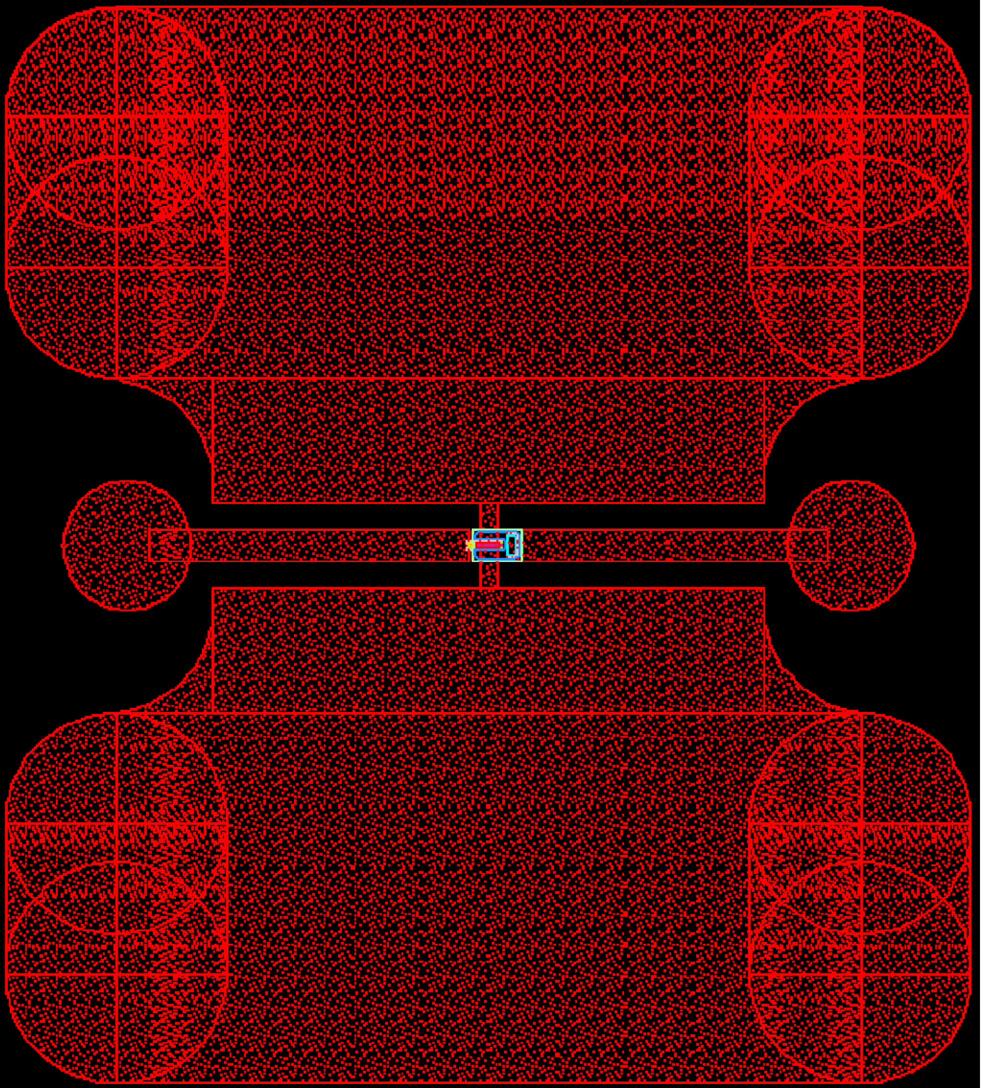
- All features realized by I-line lithography
- Emitter contact resistance $\rho_{c,\,ex}$ is ~ 5 $\Omega\cdot\mu m^2$
- Base ρ_c is < 2 $\Omega\cdot\mu m^2$ as deposited…
  - Increases to ~ 6-7 $\Omega\cdot\mu m^2$ after 60 min, 250°C BCB
- Recall, 1/8 µm scaling generation needs $\leq 5\ \Omega\cdot\mu m^2$ emitter ρ_c

Test-fixture surrounding the DUT

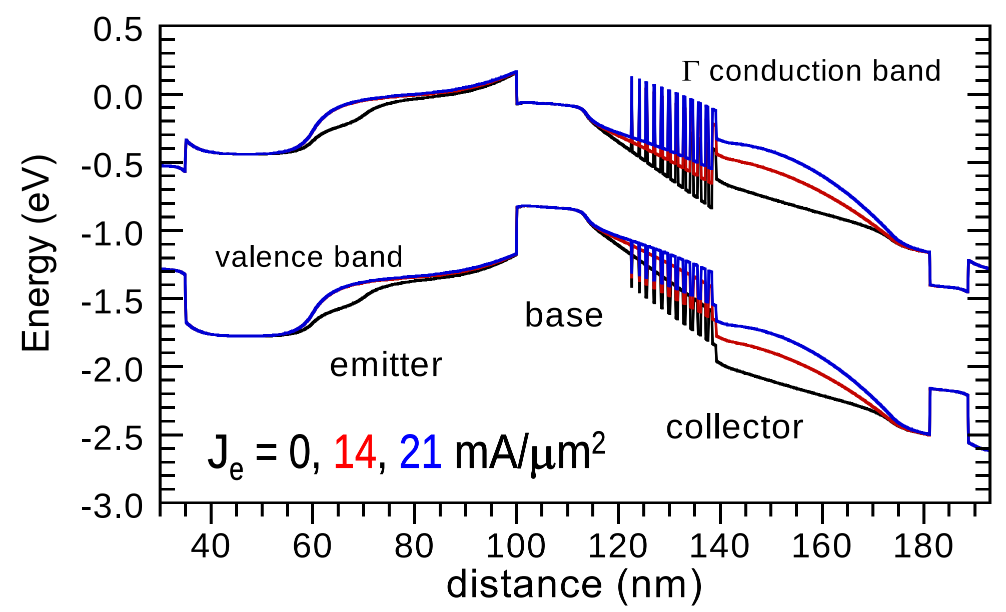
Details behind 2-port device measurement:

1. Shielded probes
   – Cascade Infinity in this case
2. Microwave absorber under DUT
   -- The substrate is ~ 635μm thick
   -- First parasitic mode excited ~ 26 GHz
3. Signal feed line is 75μm per side
4. Probe-pad is circular, Radius = 15μm
5. Structure resides on ~ 1.8μm BCB (ε_r = 2.7), on thick InP substrate (ε_r ~13)

OK for manual probing, not automated



Layer structure -- 60 nm collector DHBT



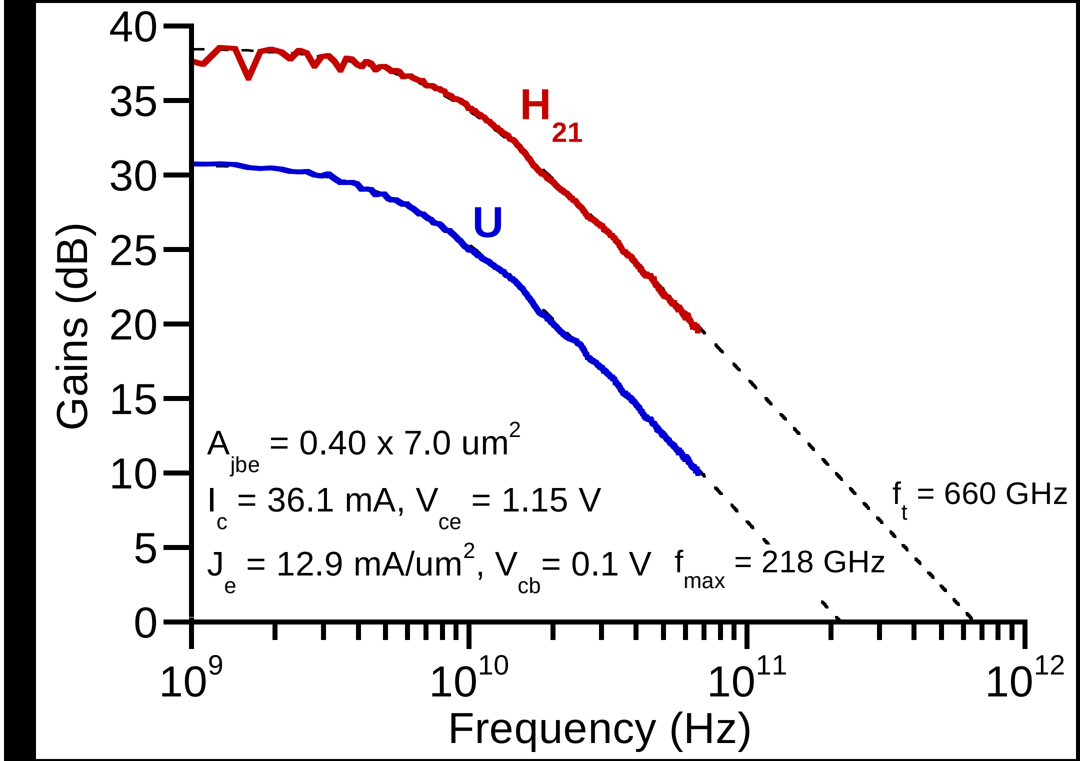
V_{be} = 0.95 V, V_{cb} = 0.0 V

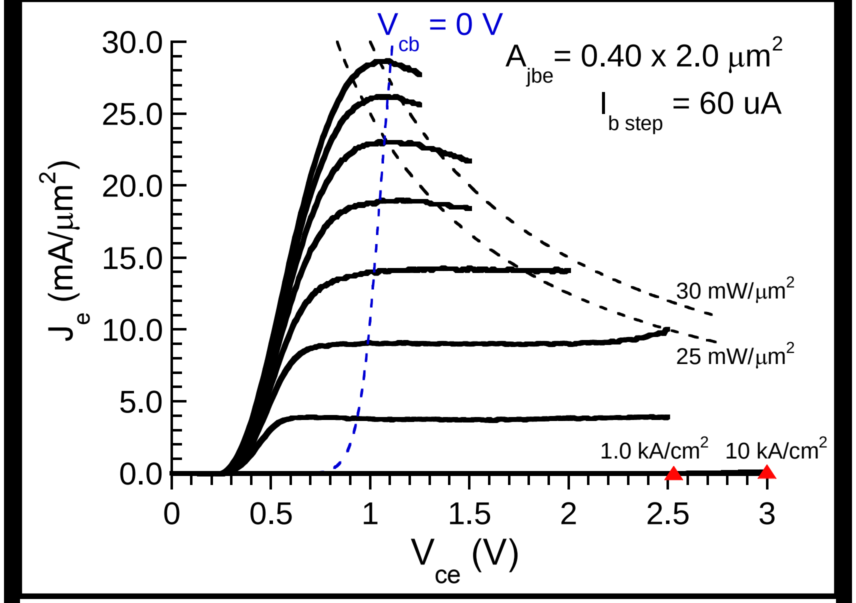
Objective:

- Thin collector and base for decreased electron transit time
- High f_τ device with moderate f_{max}
- Investigate J_{max} before current blocking in the base-collector grade
- What is the HBT breakdown at this collector scaling node?

Thickness (nm)	Material	Doping cm^{-3}	Description
10	$In_{0.85}Ga_{0.15}As$	$5\cdot10^{19}$: Si	Emitter cap
15	$In_xGa_{1-x}As$	$> 4\cdot10^{19}$: Si	Emitter cap grading
10	$In_{0.53}Ga_{0.47}As$	$4\cdot10^{19}$: Si	Emitter
85	InP	$3\cdot10^{19}$: Si	Emitter
10	InP	$1.2\cdot10^{18}$: Si	Emitter
30	InP	$1.0\cdot10^{18}$: Si	Emitter
14	InGaAs	$10\text{-}7\cdot10^{19}$: C	Base
7.5	$In_{0.53}Ga_{0.47}$ As	$7.5\cdot10^{16}$: Si	Setback
18	InGaAs / InAlAs	$7.5\cdot10^{16}$: Si	B-C Grade
3	InP	$3.75\cdot10^{18}$: Si	Pulse doping
31.5	InP	$7.5\cdot10^{16}$: Si	Collector
7.5	InP	$1\cdot10^{19}$: Si	Sub Collector
7.5	$In_{0.53}Ga_{0.47}$ As	$2\cdot10^{19}$: Si	Sub Collector
300	InP	$2\cdot10^{19}$: Si	Sub Collector
Substrate	SI : InP		

DC data – 60 nm collector, 14 nm base InP Type-I DHBT



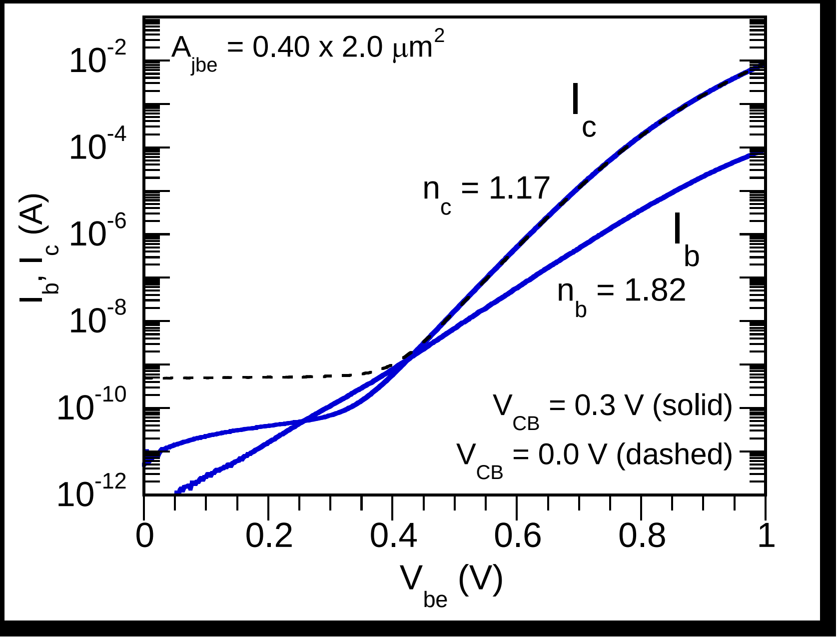


BV_{CEO} = 3.01 V, BV_{CBO} = 3.76 V ($J_{e,c}$ = 10kA/cm^2)

Emitter contact (from RF extraction), R_{cont} ~ 6.2 Ω·μm^2

Base: R_{sheet} = 1470 Ω/sq, R_{cont} ~ 70 Ω·μm^2

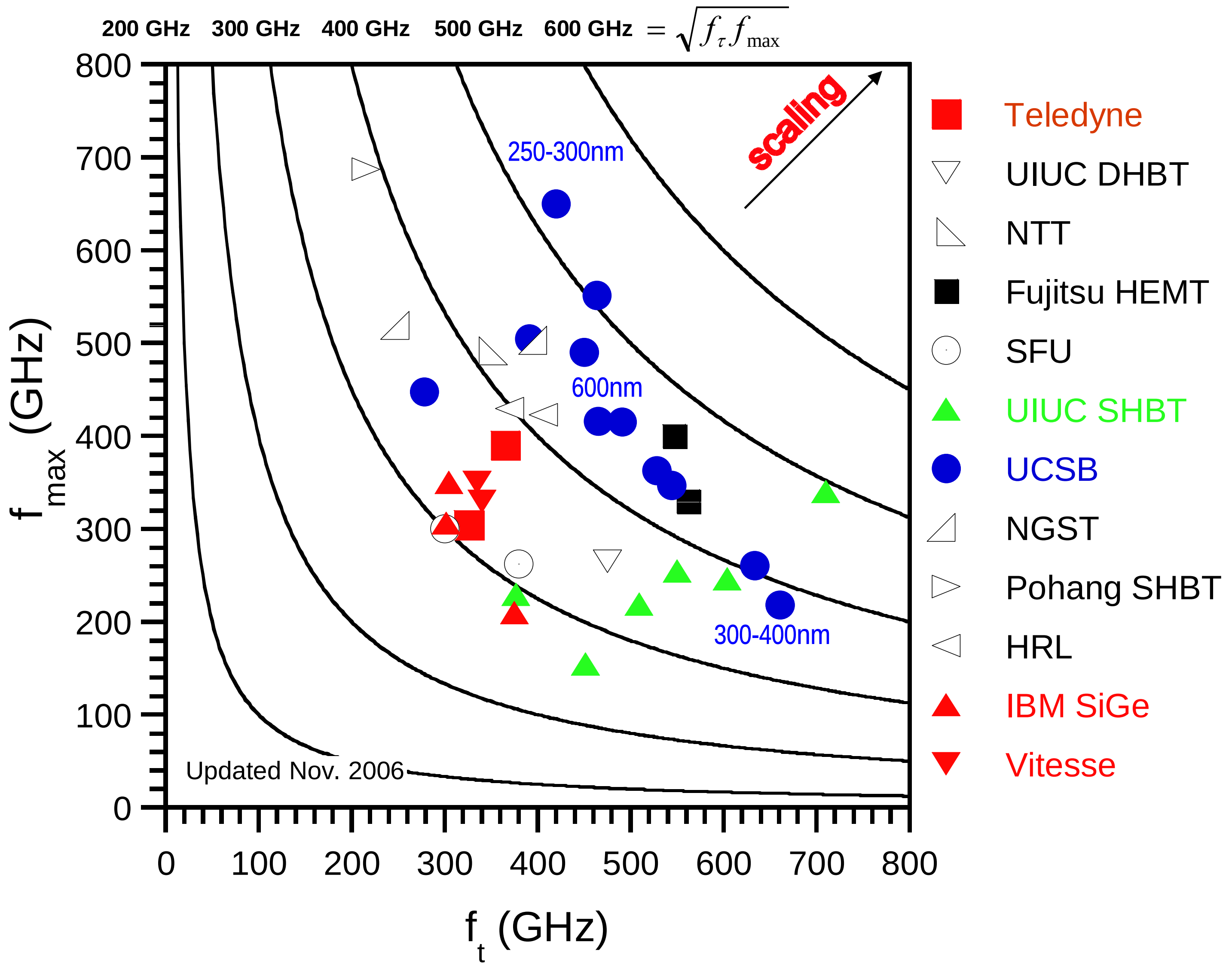
Collector: R_{sheet} = 12.1 Ω/sq, R_{cont} ~ 4.7 Ω·μm^2



NOTE:

660GHz f_τ validated by 1/slope of 1/Imag(H_{21}) vs freq

Fast transistors – late 2006



popular metrics :

f_τ or $f_{\max}$ alone

$(f_\tau + f_{\max})/2$

$\sqrt{f_\tau f_{\max}}$

$(1/f_\tau + 1/f_{\max})^{-1}$

much better metrics :

<u>power amplifiers</u>:

PAE, associated gain,

mW/μm

<u>low noise amplifiers</u>:

$F_{\min}$, associated gain,

<u>digital</u>:

f_{clock}, hence

$(C_{cb}\Delta V / I_c)$,

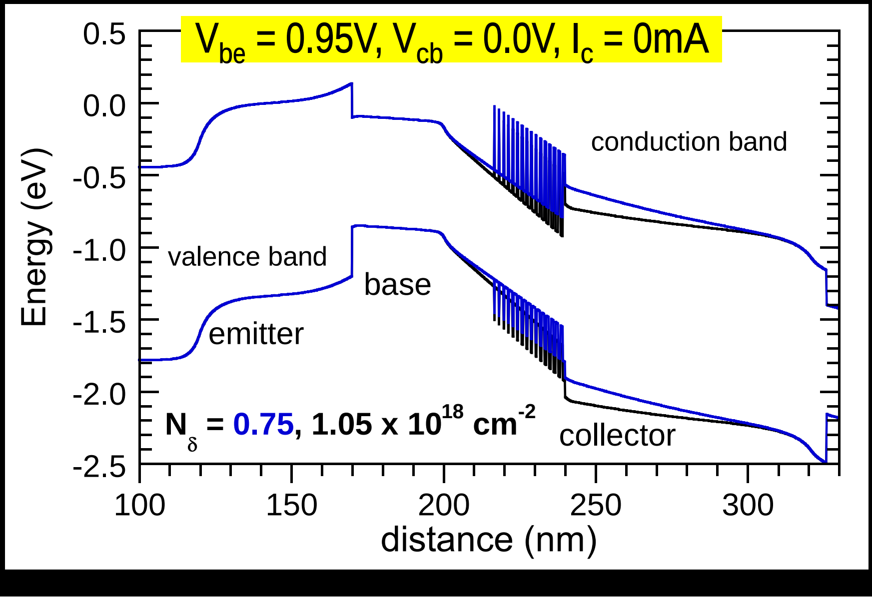
$(R_{ex} I_c / \Delta V)$,

$(R_{bb} I_c / \Delta V)$,

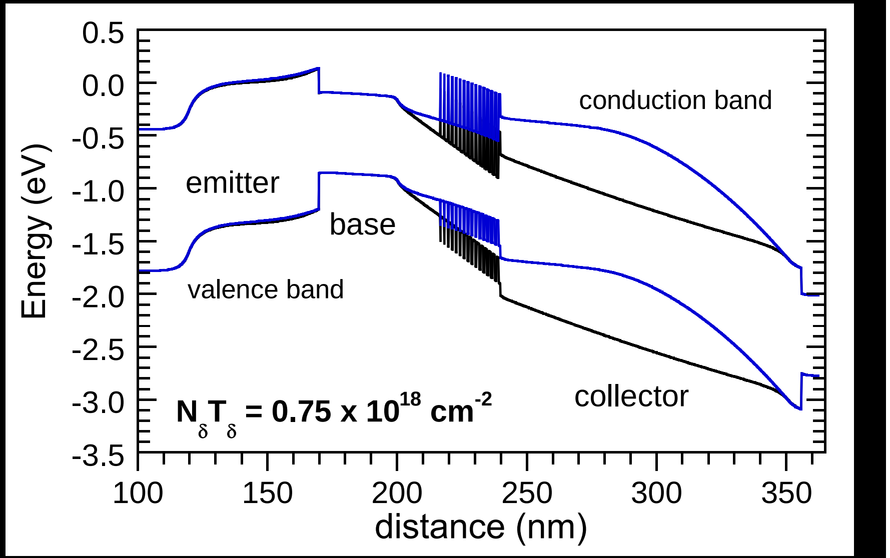
$(\tau_b + \tau_c)$

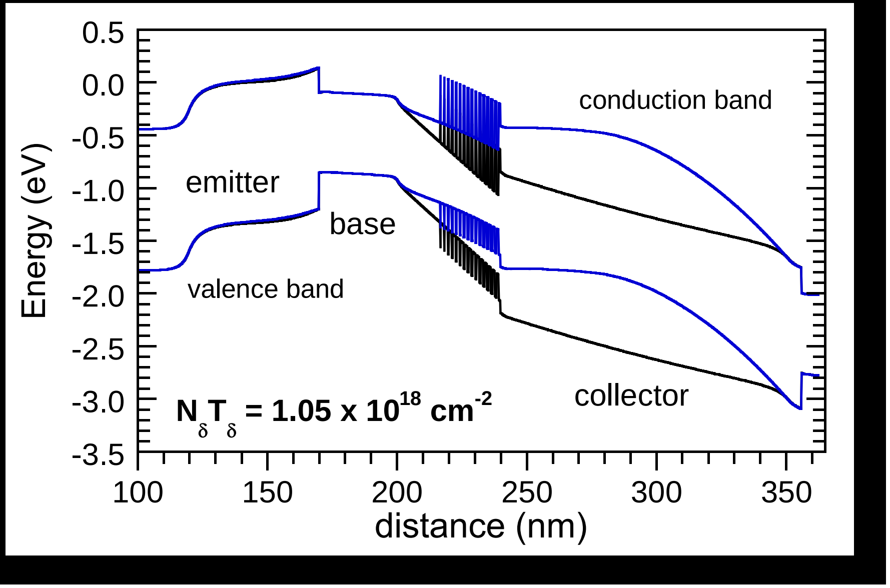
Band diagram – UCSB 150 nm collector DHBT revised

Thickness (nm)	Material	Doping cm^{-3}	Description
30	InGaAs	$7\text{-}4 \cdot 10^{19}$: C	Base
15	$In_{0.53}Ga_{0.47}As$	$3.5 \cdot 10^{16}$: Si	Setback
24	InGaAs / InAlAs	$3.5 \cdot 10^{16}$: Si	B-C Grade
3	InP	$3.5 \cdot 10^{18}$: Si	Pulse doping
108	InP	$3.5 \cdot 10^{16}$: Si	Collector
5	InP	$1 \cdot 10^{19}$: Si	Sub Collector
6.5	$In_{0.53}Ga_{0.47}As$	$2 \cdot 10^{19}$: Si	Sub Collector
300	InP	$2 \cdot 10^{19}$: Si	Sub Collector
Substrate	SI : InP		

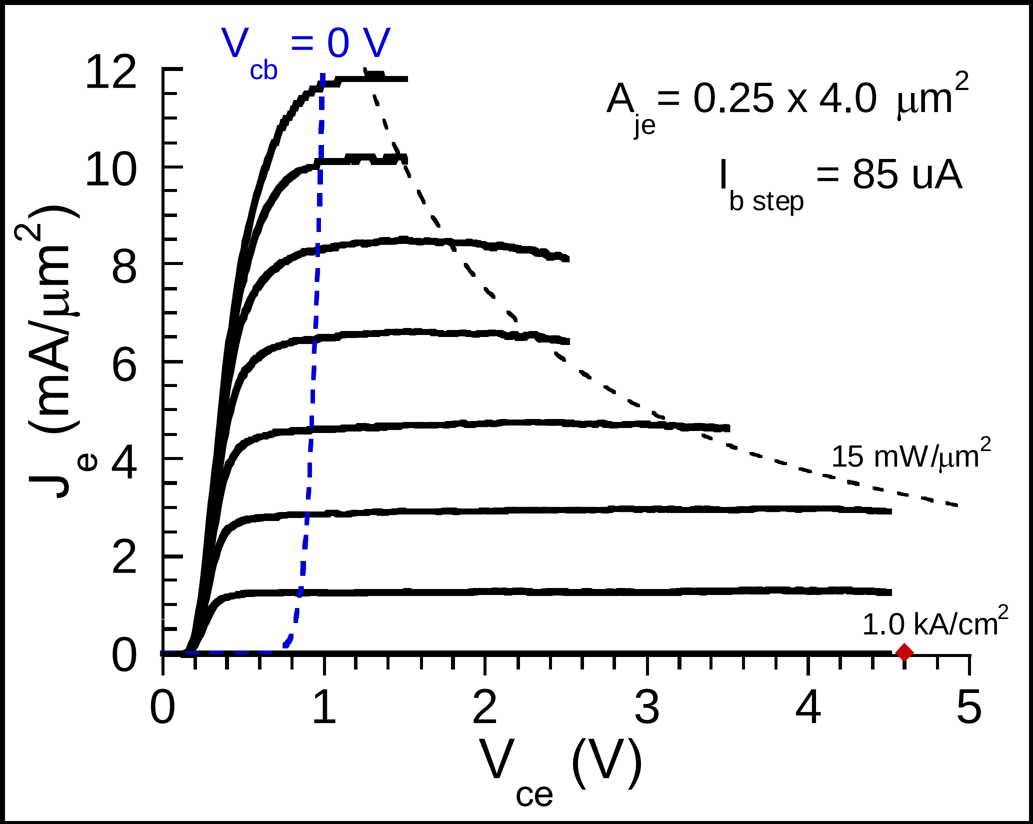


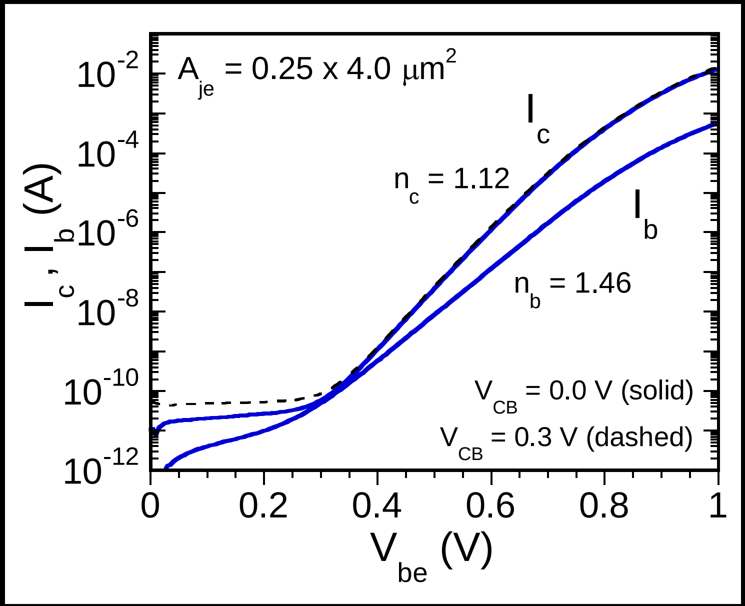
V_{be} = 0.95V, V_{cb} = 0.6V, J_e = 0, 10 mA/μm^2

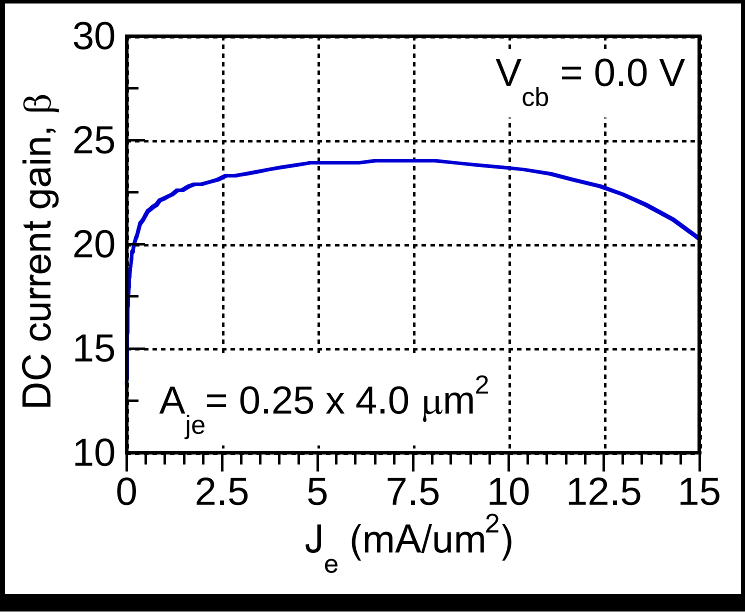




DC data – 150nm collector, 30nm base InP Type-I DHBT







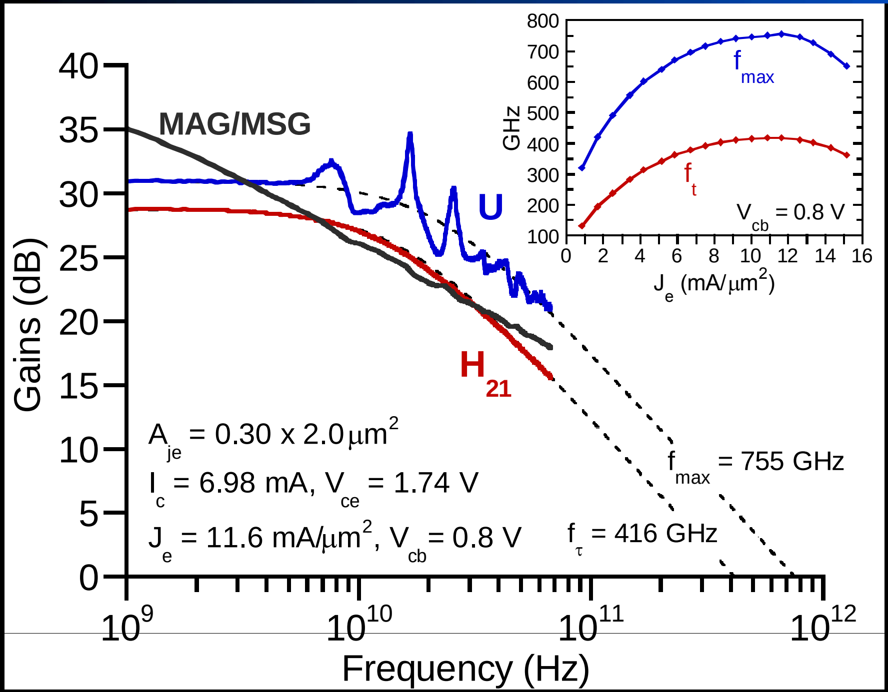
BV_{CEO} = 5.64 V, BV_{CBO} = 6.65 V ($J_{e,c}$ = 10 kA/cm^2)

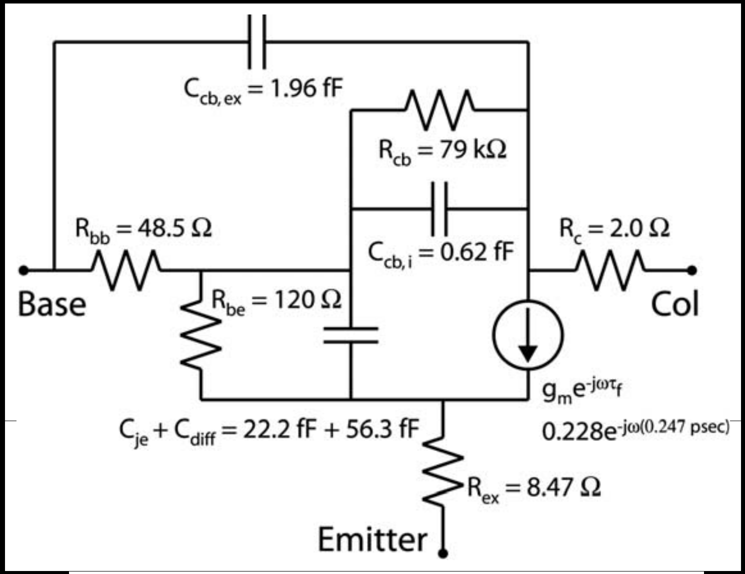
Emitter contact (from RF extraction), R_{cont} ~ 5.1 Ω·μm^2

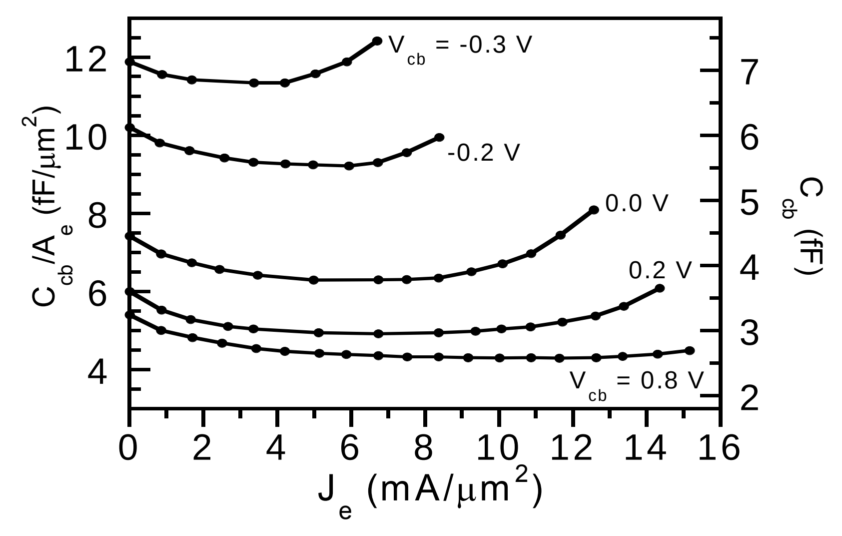
Base: R_{sheet} = 603 Ω/sq, R_{cont} ~ 6.29 Ω·μm^2

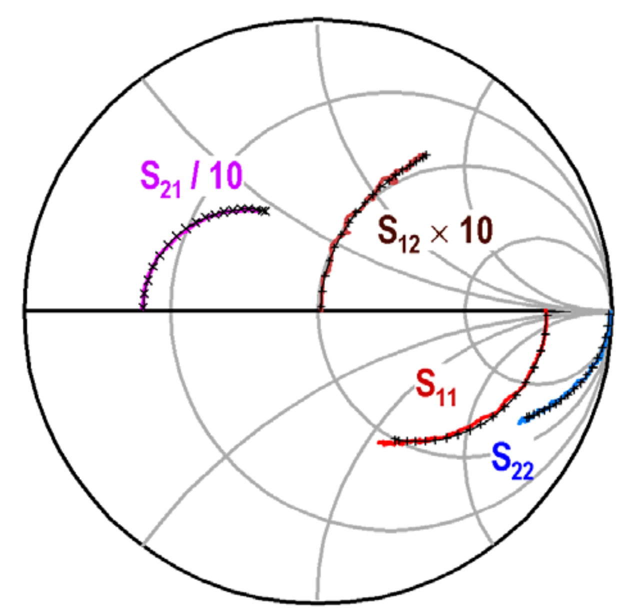
Collector: R_{sheet} = 12.2 Ω/sq, R_{cont} ~ 6.37 Ω·μm^2

Measured microwave data – 755 GHz f_{max}



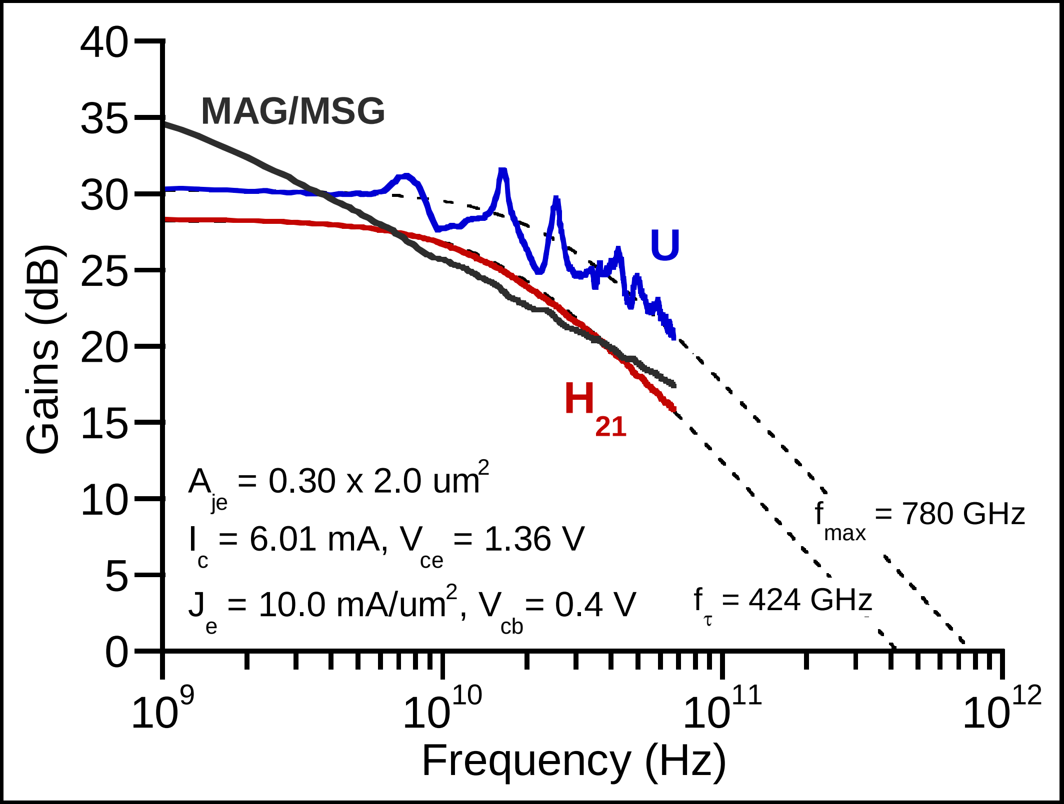






Frequency span: 100 MHz to 67 GHz

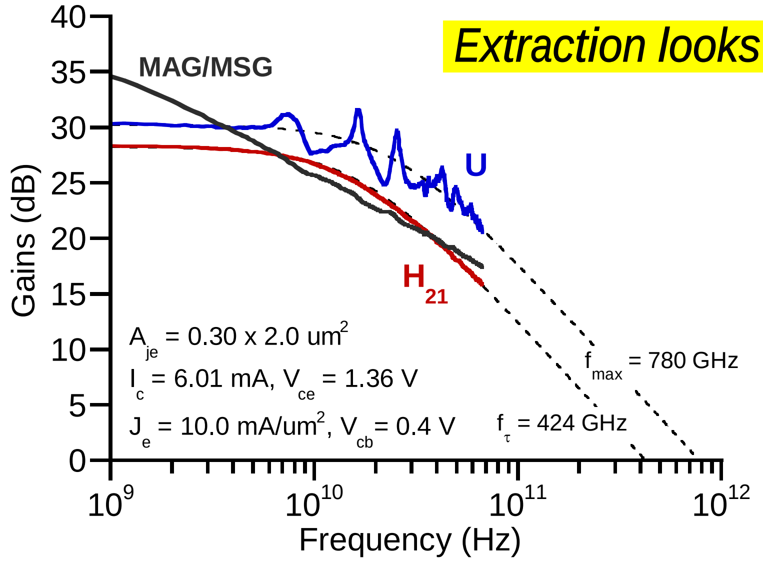
Surprise finding…higher f_{max} HBT bias found



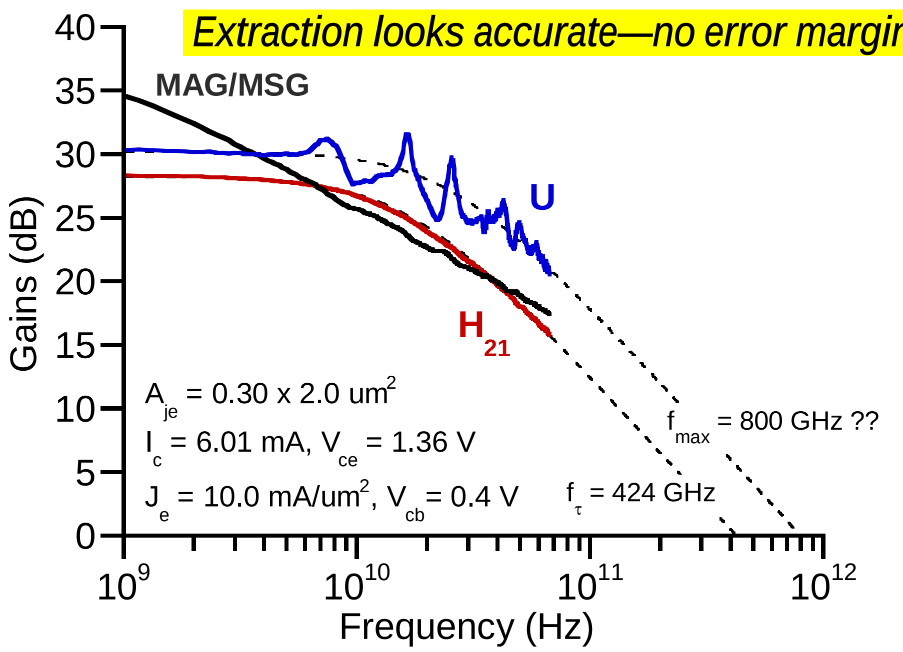
- Record f_{max} for a transistor
- Record bandwidth for any device…at room temperature
  - Previous high is f_τ = 755GHz from UIUC InP SHBTs → f_τ = 845GHz when cooled to -55°C
- Record high $f_\tau \times BV_{ceo}$ = 2391 GHz·V -- exceeding previous Type-II InP DHBT
  - Similar values have been demonstrated by UCSB InP Type-I DHBT at 120nm collector node

Reasonableness of f_{max} determination at 780GHz

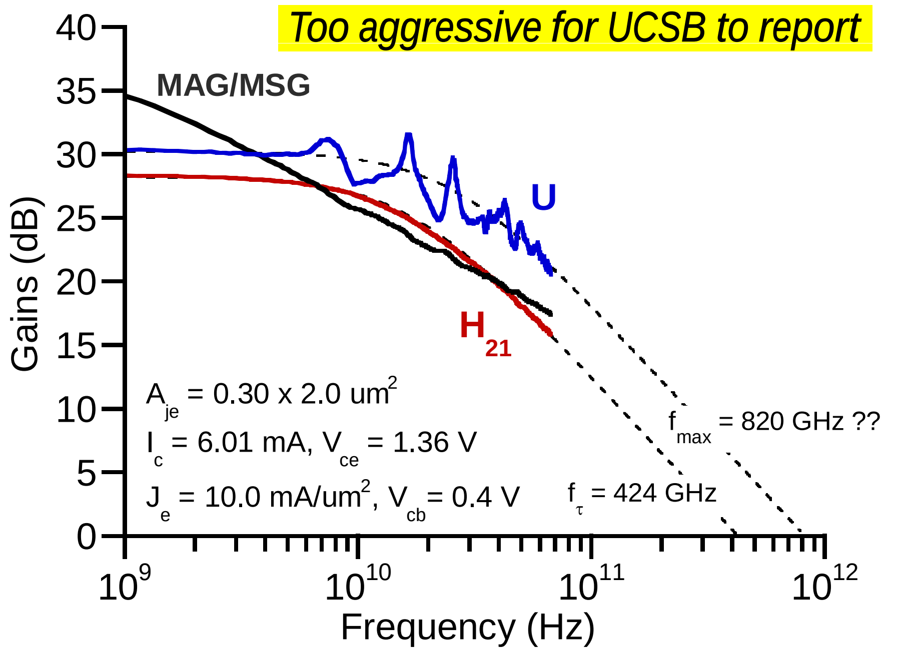
Extraction looks accurate—confident reporting



Extraction looks accurate—no error margin

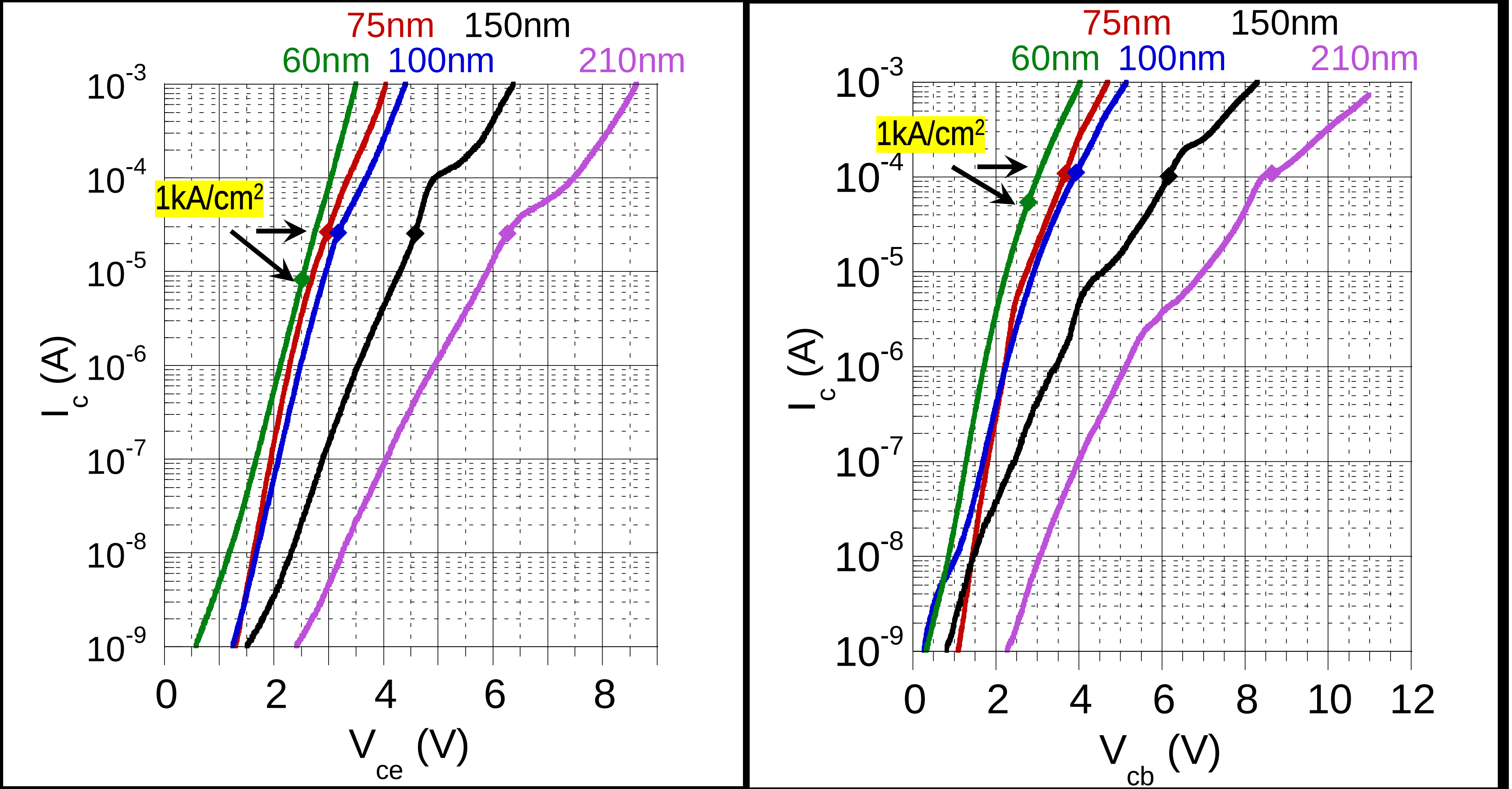


Too aggressive for UCSB to report



Common emitter and base breakdown of UCSB InP Type-I DHBTs

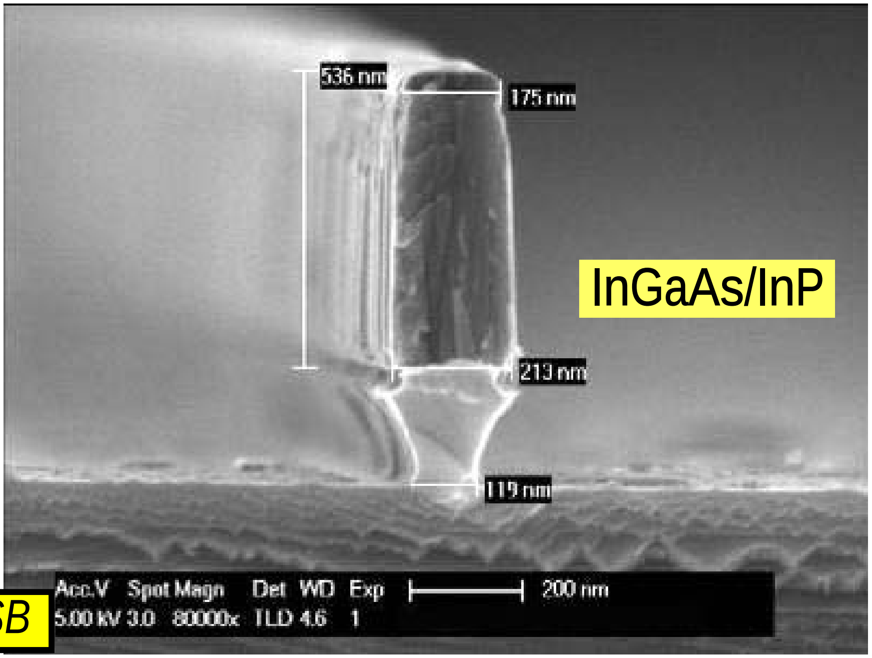
Collector thicknesses, T_c



Published data shows similar BV_{ceo},BV_{cbo} for type-I and type-II DHBTs…
and is much higher than InP SHBTs at any scaling generation at same J_e, J_c

2007: 125 nm Scaling Generation → almost-THz HBT

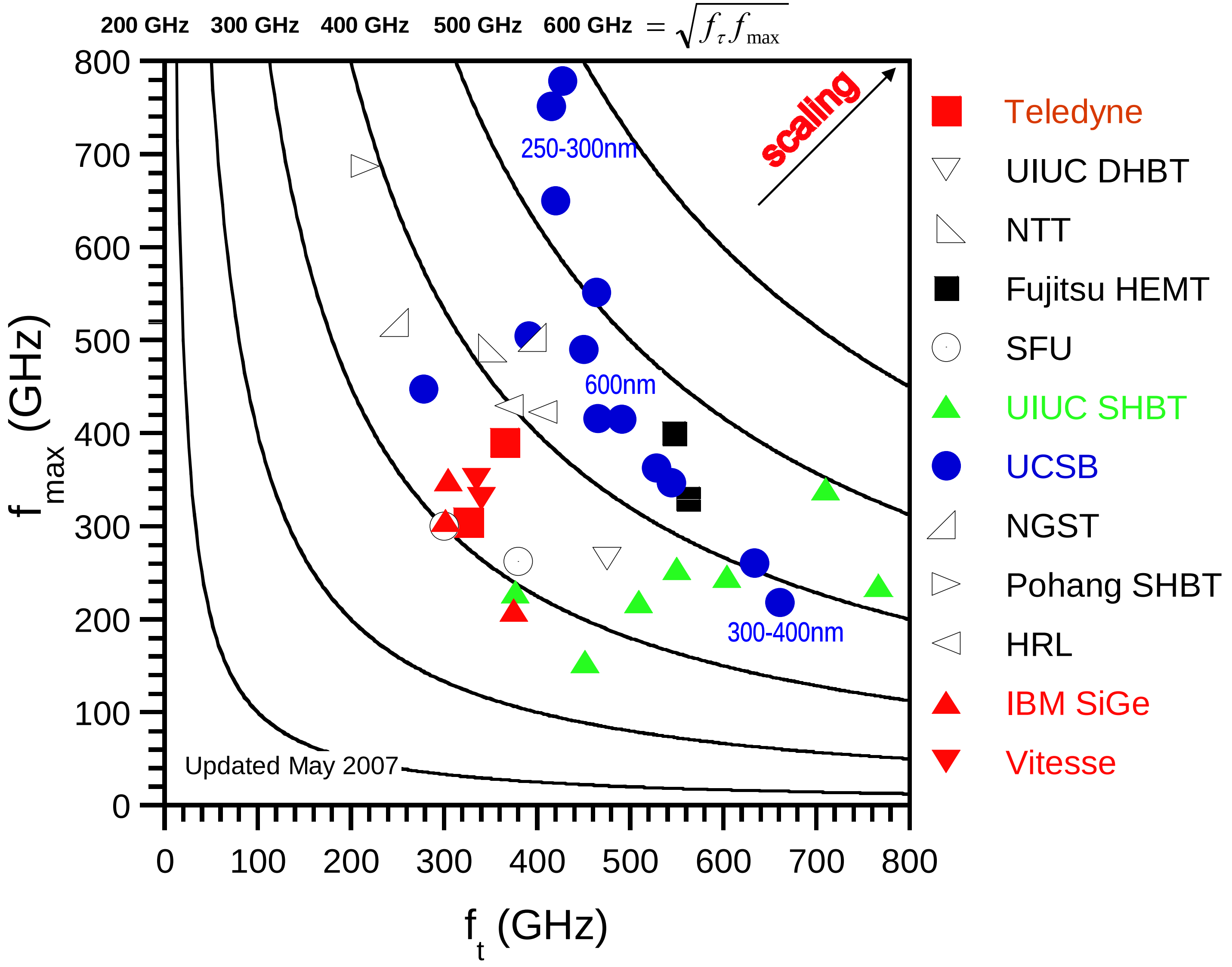
emitter	500	250	125 nm width	✓
	16	9	$4\ \Omega\cdot\mu m^2$ access ρ	✓
base	300	150	75 width,	✓
	20	10	$5\ \Omega\cdot\mu m^2$ contact ρ	✓
collector	150	100	75 nm thick,	✓
	5	10	$20\ mA/\mu m^2$ current density	✓
	5	3.5	3 V, breakdown	✓
f_τ	400	500	700 GHz	
f_{max}	500	700	1000 GHz	
power amplifiers	250	350	500 GHz	
digital clock rate (static dividers)	160	230	330 GHz	



InGaAs/InP

*Emitter formation design: **Erik Lind**, Post-Doc, UCSB*

InP HBTs today



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PAE, associated gain,

mW/μm

low noise amplifiers:

$F_{\min}$, associated gain,

digital:

f_{clock}, hence

$(C_{cb}\Delta V / I_c)$,

$(R_{ex} I_c / \Delta V)$,

$(R_{bb} I_c / \Delta V)$,

$(\tau_b + \tau_c)$

Conclusion

- 250nm InP DHBTs have demonstrate record bandwidth of 780GHz
- Type-I InP DHBTs are scalable down to 60nm collectors w/ 2× higher breakdown voltages – *with usable high-voltage, high current operation*
- Record $f_\tau \times BV_{ceo}$ = 2390GHz·V demonstrated for same collector thickness as Type-II GaAsSb InP DHBTs
- With little time to spare, UCSB aggressively pursuing 125nm devices and is close…
  - All potential device physic limitations satisfied…just need to make it

This work was supported DARPA under the TFAST program N66001-02-C-8080, DARPA SWIFT program, and by the ONR N0001-40-4-10071