Ultra Low Resistance Ohmic Contacts to InGaAs/InP

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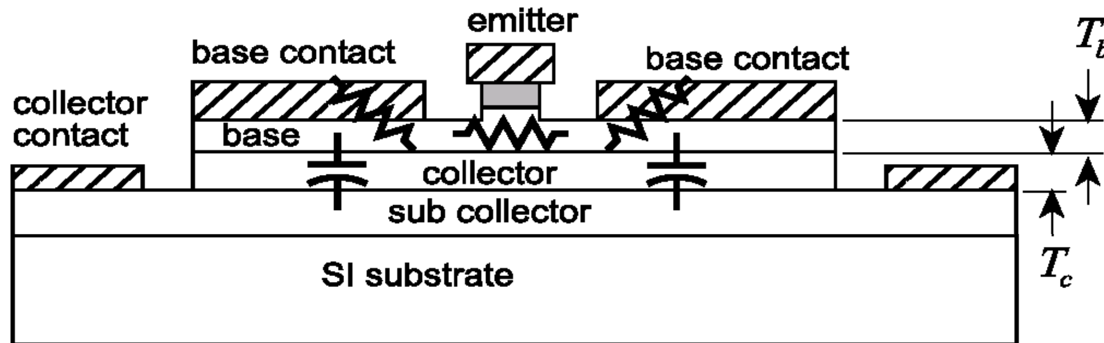
Outline

- **Motivation**
- **Previous Work**
- **Approach**
- **Results**
- **Conclusion**

Device bandwidth scaling laws



$$\frac{1}{2\pi f_\tau} = \tau_{base} + \tau_{collector} + C_{je}\frac{kT}{qI_E} + C_{bc}\frac{kT}{qI_E} + R_{ex}C_{bc} + R_{coll}C_{bc}$$

$$f_{\max} = \sqrt{\frac{f_\tau}{8 \cdot \pi \cdot (R_{bb} \cdot C_{cb})_{eff}}}$$

Goal: Double transistor bandwidth → Reduce transit delay, Reduce RC delay → Vertical Scaling

Increased Capacitance → Lateral Scaling → Keep R constant → Reduce ρ_c

$$R_{ex} = \frac{\rho_c}{A}$$ → ρ_c has to scale as inverse square of lateral scaling

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*M.J.W. Rodwell, IEEE Trans. Electron. Dev., 2001

Device bandwidth scaling roadmap – THz transistor

Emitter Resistance key to THz transistor

Emitter resistance effectively contributes > 50 % in bipolar logic gate delay*

Contact resistance serious barrier to THz technology

$2\ \Omega \cdot \mu m^2$ contact resistivity required for simultaneous THz f_t and f_{max}

Parameter	scaling law	Gen. 2 (500 nm)	Gen. 3 (250 nm)	Gen. 4 (125 nm)	Gen 5 (62.5nm)
MS-DFF speed	γ^1	150 GHz	240 GHz	330 GHz	480 GHz
Amplifier center frequency	γ^1	245 GHz	430 GHz	660 GHz	1.0 THz
Emitter Width	$1/\gamma^2$	500 nm	250 nm	125 nm	62.5 nm
Resistivity	$1/\gamma^2$	16 Ω-μm^2	8 Ω-μm^2	4 Ω-μm^2	2 Ω-μm^2
Base Thickness	$1/\gamma^{1/2}$	300Å	250 Å	212 Å	180 Å
Contact width	$1/\gamma^2$	300 nm	175 nm	120 nm	60 nm
Doping	γ^0	7 10^{19} /cm^2	7 10^{19} /cm^2	7 10^{19} /cm^2	7 10^{19} /cm^2
Sheet resistance	$\gamma^{1/2}$	500 Ω	600 Ω	708 Ω	830 Ω
Contact ρ	$1/\gamma^2$	20 Ω-μm^2	10 Ω-μm^2	5 Ω-μm^2	2.5 Ω-μm^2
Collector Width	$1/\gamma^2$	1.2 μm	0.60 μm	0.36 μm	0.18 μm
Thickness	$1/\gamma$	1500 Å	1060 Å	750 Å	530 Å
Current Density	γ^2	4.5 mA/μm^2	9 mA/μm^2	18 mA/μm^2	36 mA/μm^2
$A_{collector}/A_{emitter}$	γ^0	2.4	2.4	2.9	2.8
f_τ	γ^1	370 GHz	520 GHz	730 GHz	1.0 THz
f_{max}	γ^1	490 GHz	850 GHz	1.30 THz	2.0 THz
$V_{BR,CEO}$		4.9 V	4.0 V	3.3 V	2.75 V
ΔT		39 K	50 K	61 K	72 K
I_E / L_E	γ^0	2.3 mA/μm	2.3 mA/μm	2.3 mA/μm	2.3 mA/μm
τ_f	$1/\gamma$	340 fs	240 fs	180 fs	130 fs
C_{cb} / I_c	$1/\gamma$	400 fs/V	280 fs/V	240 fs/V	170 fs/V
$C_{cb} \Delta V_{logic} / I_c$	$1/\gamma$	120 fs	85 fs	74 fs	52 fs
$R_{bb} /(\Delta V_{logic} / I_c)$	γ^0	0.76	0.47	0.34	0.26
$C_{je} (\Delta V_{logic} / I_C)$	$1/\gamma^{3/2}$	380 fs	180 fs	94 fs	50 fs
$R_{ex} /(\Delta V_{logic} / I_c)$	γ^0	0.24	0.24	0.24	0.24

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*M.J.W. Rodwell, IEEE Trans. Electron. Dev., 2001

Device bandwidth scaling-FETs

Source contact resistance must scale to the inverse square of device scaling

Source resistance reduces g_m and I_d

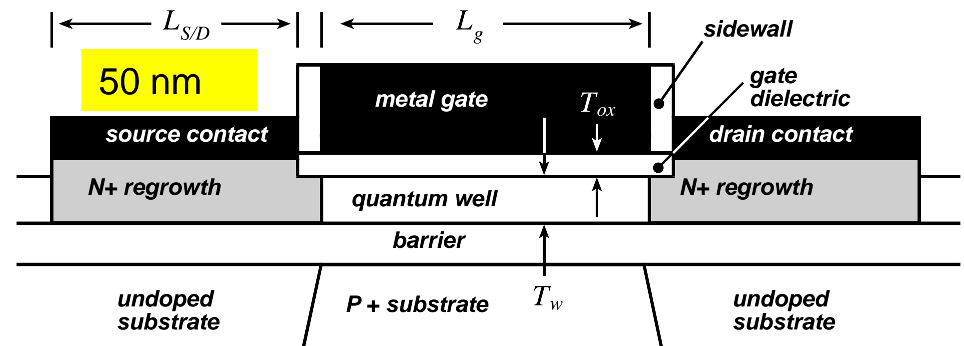
A 22 nm III-V MOSFET with 5 mA/µm I_d

↓

15 $\Omega \cdot \mu m$ source resistance will reduce I_d by 10%

↓

With 50 nm contact width this will require ρ_c of 1 $\Omega \cdot \mu m^2$



Low source resistance means better NF in FETs*

$$NF_{\min} \approx 1 + \sqrt{g_{mi}(R_s + R_g + R_i)\Gamma} \cdot \left(\frac{f}{f_\tau}\right)$$

*T Takahashi ,IPRM 07

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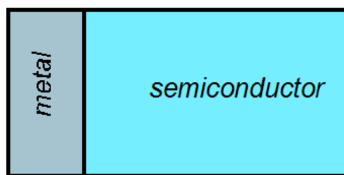
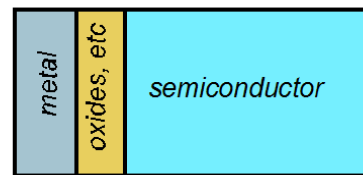
Conventional Contacts

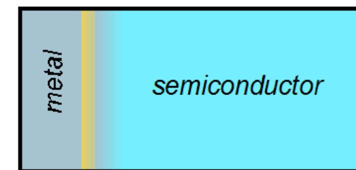
- Conventional contacts
  - complex metallization and annealing schemes
  - Surface oxides, contaminants
  - Fermi level pinning
  - metal-semiconductor reaction improves resistance

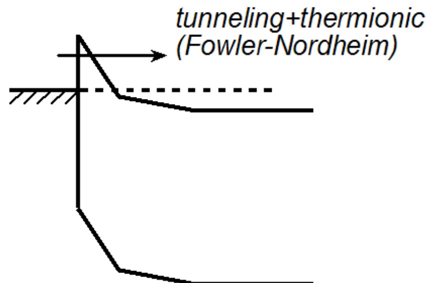
5 Ω- μm² ($5 \cdot 10^{-8}$ Ω- μm²) obtained on InGaAs, used on the latest HBT results

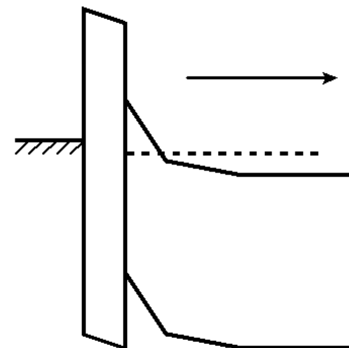
Further improvement difficult using this technique

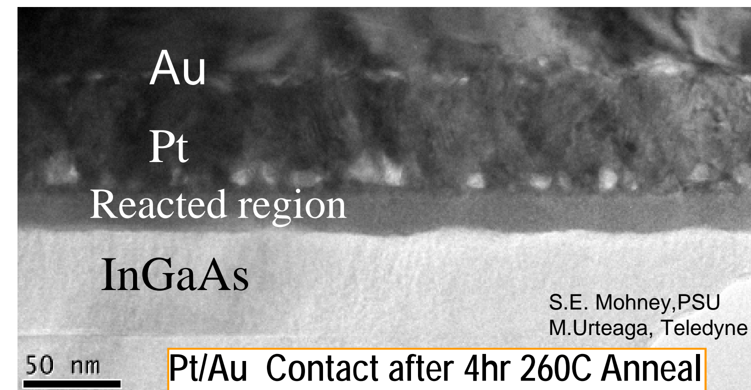












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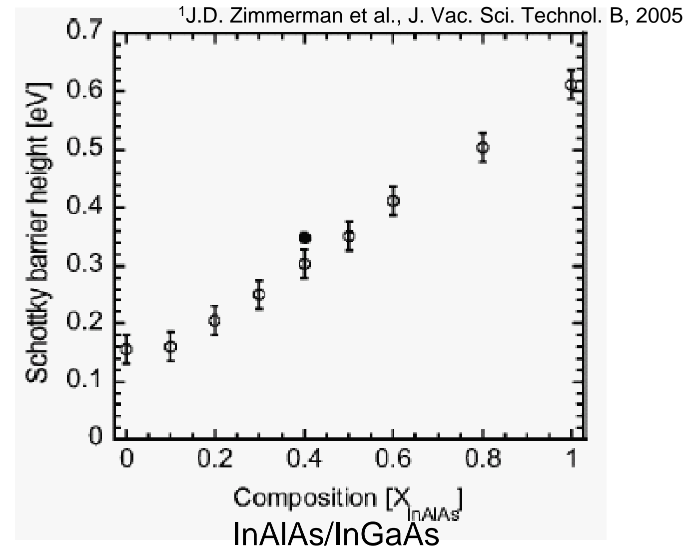
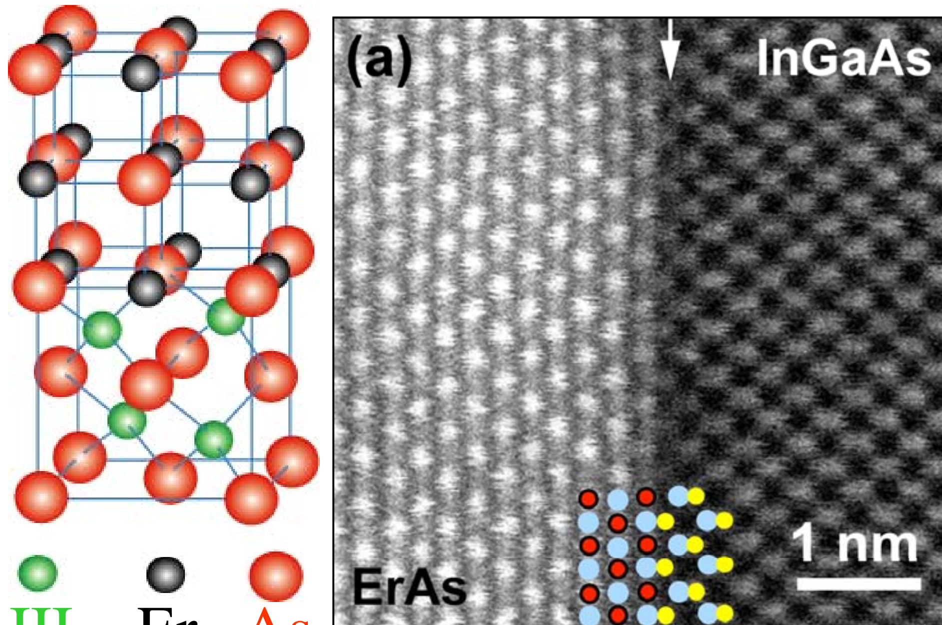
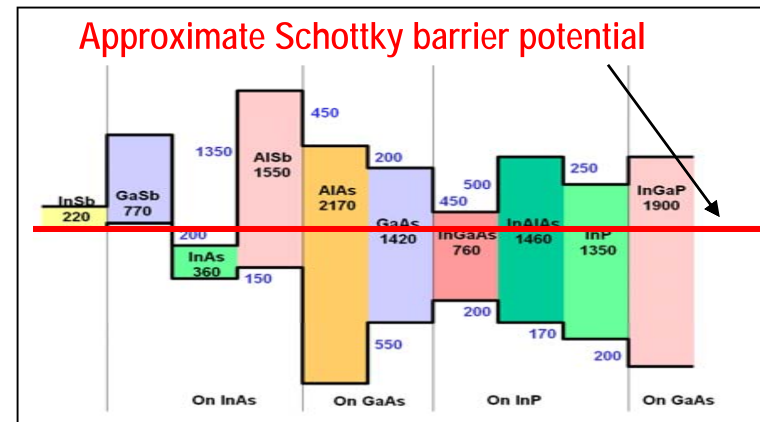
In-situ ErAs-InGaAs Contacts

- Epitaxial ErAs-InGaAs contact
  - Epitaxially formed, no surface defects, no fermi level pinning
  - *In-situ,* no surface oxides
  - thermodynamically stable
  - ErAs/InAs fermi level should be above conduction band





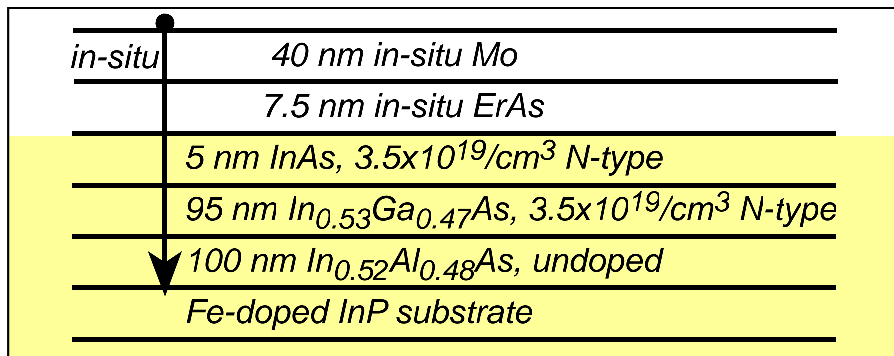
D. O. Klenov, Appl. Phys. Lett., 2005



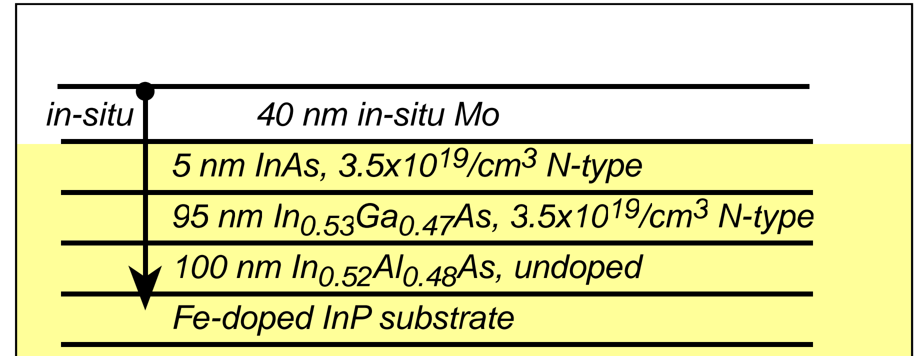
S.R. Bank, NAMBE , 2006

In-situ and *ex-situ* Contacts

- *In-situ* Mo Contact
  - *In-situ* deposition no oxide at metal-semiconductor interface
  - Fermi level pins inside conduction band of InAs

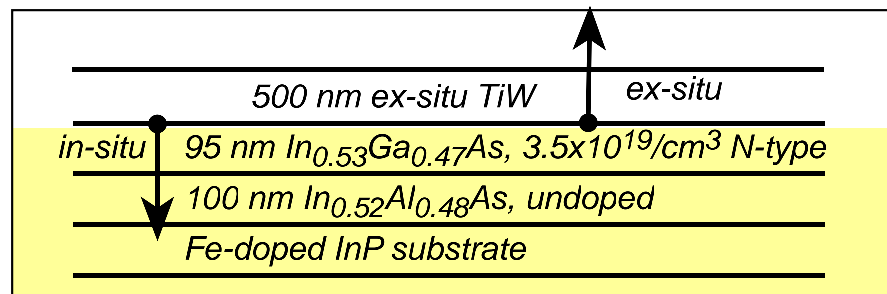


In-situ ErAs/InAs



In-situ Mo/InAs

- *Ex-situ* contacts
  - InGaAs surface oxidized by UV Ozone treatment
  - Strong NH4OH treatment before contact metal deposition



Ex-situ TiW/InGaAs

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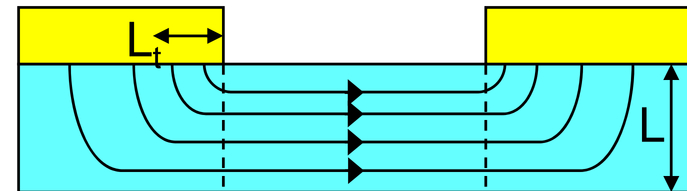
* S.Bhargava, Applied Physics Letters, 1997

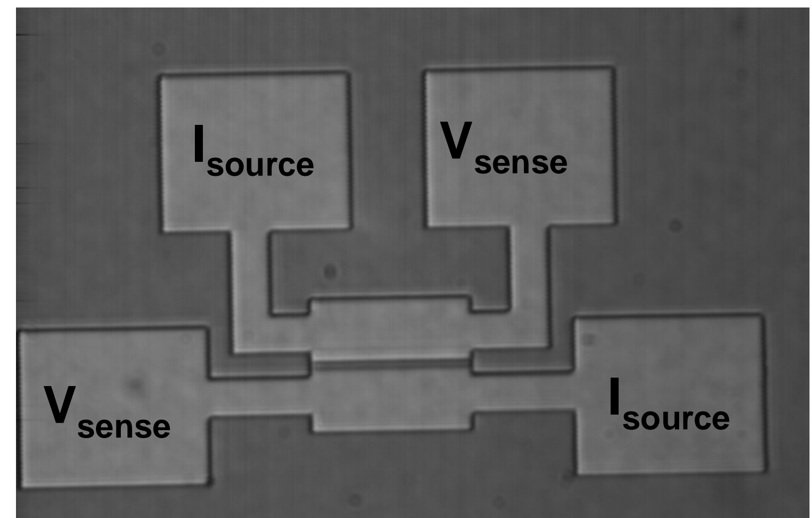
MBE growth and TLM fabrication

- MBE Growth
  - InGaAs:Si grown at 450 C
  - 3.5 E 19 active Si measured by Hall
  - ErAs grown at 450 C, 0.2 ML/s
  - Mo deposited in a electron beam evaporator connected to MBE under UHV
  - Mo cap on ErAs to prevent oxidation
  - Layer thickness chosen so as to satisfy 1-D condition in TLM



$L_t/L >> 1$

- TLM Fabrication
  - Samples processed into TLM structures by photolithography and liftoff
  - Mo and TiW dry etched in SF_6/Ar with Ni as etch mask, isolated by wet etch
  - Separate probe pads from contacts to minimize parasitic metal resistance



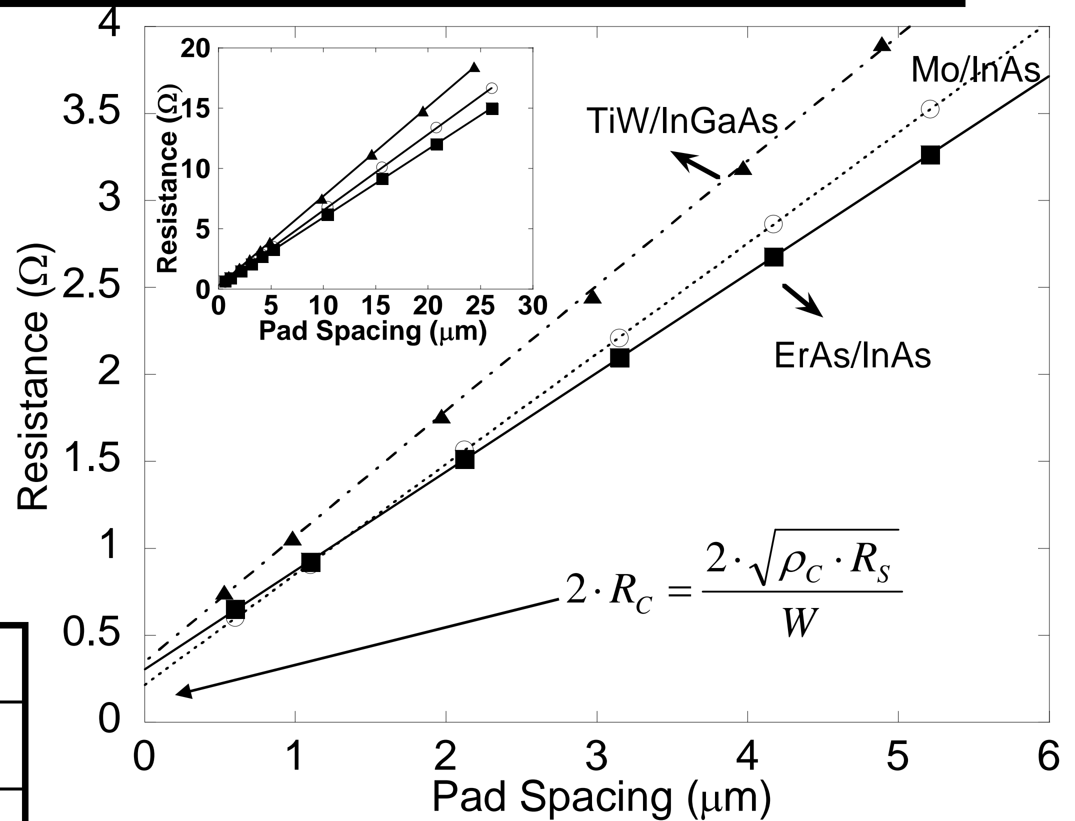
Contact Resistance

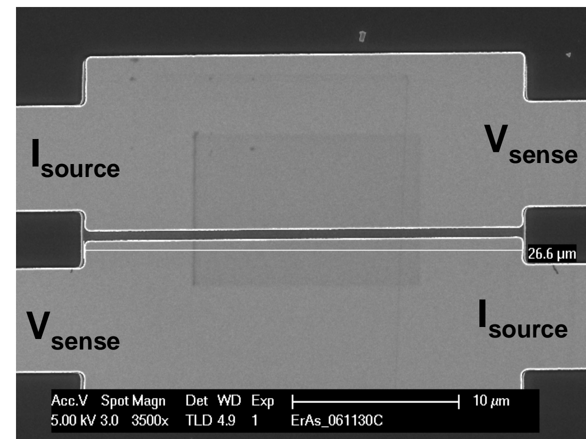
- Resistance measured by 4155 C parameter analyzer
- Pad spacing verified by SEM image
- Smallest gap, contact resistance 60 % of total resistance

- 15-18 Ohm sheet resistance for all three contacts

Contact	$\rho_c(\Omega - \mu m^2)$	L_t (nm)
ErAs/InAs	1.5	300
Mo/InAs	0.5	175
TiW/InGaAs	0.7	190

$$1\Omega \cdot \mu m^2 = 1 \cdot 10^{-8} \Omega \cdot cm^{-2}$$





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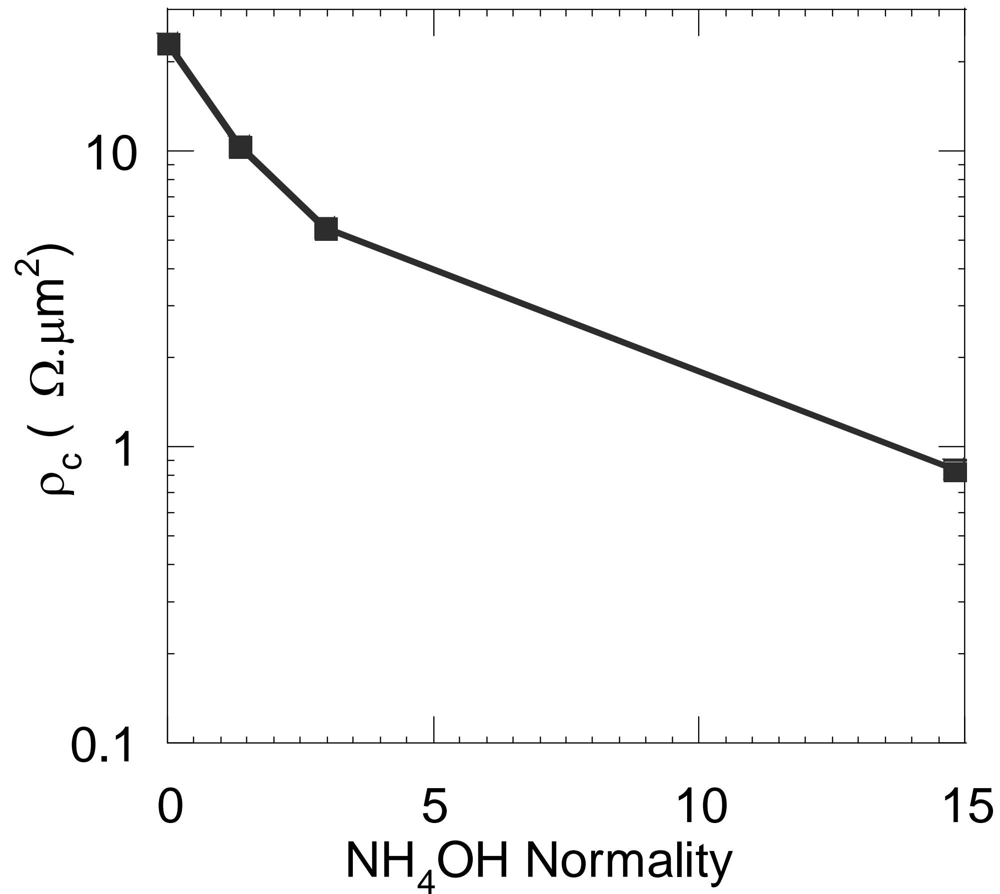
Ex-situ Contacts

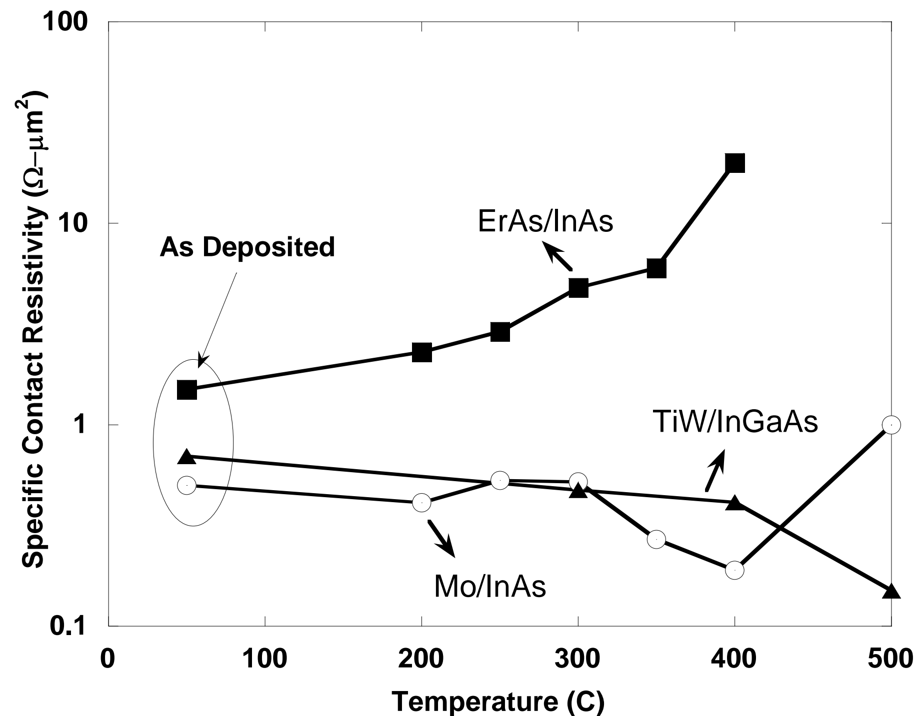
• Ex-situ contact depends on the concentration of NH_4OH*



* A.M. Crook, submitted to APL

Thermal Stability

- Contacts annealed under N_2 flow at different temperatures
- Contacts stays Ohmic after anneal
- In-situ Mo/InAs, ex-situ TiW/InGaAs contact resistivity < 1 Ω-μm^2 after anneal
- ErAs/InAs contact resistivity increases with anneal
- The increase could be due to lateral oxidation of ErAs



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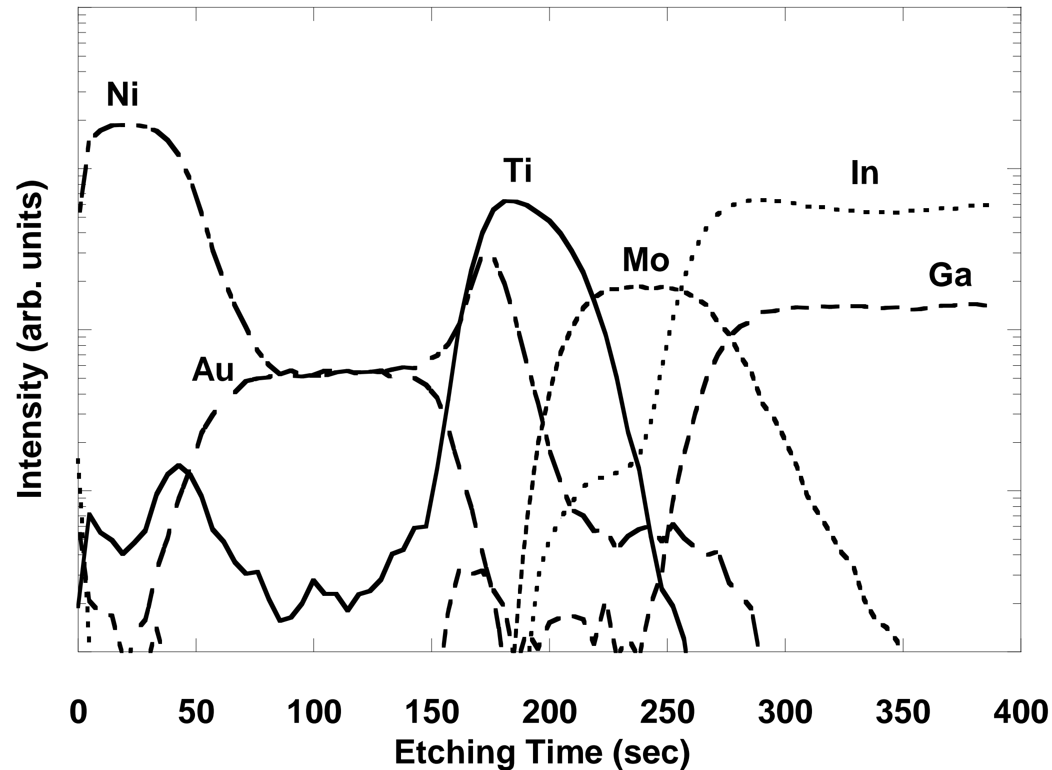
Thermal Stability

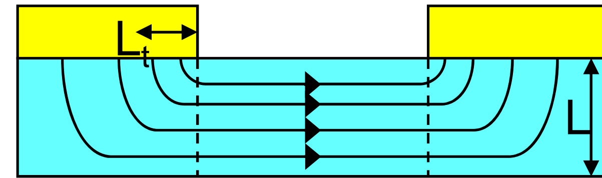
- SIMS depth profiling shows that Mo and TiW act as diffusion barrier to Ti and Au

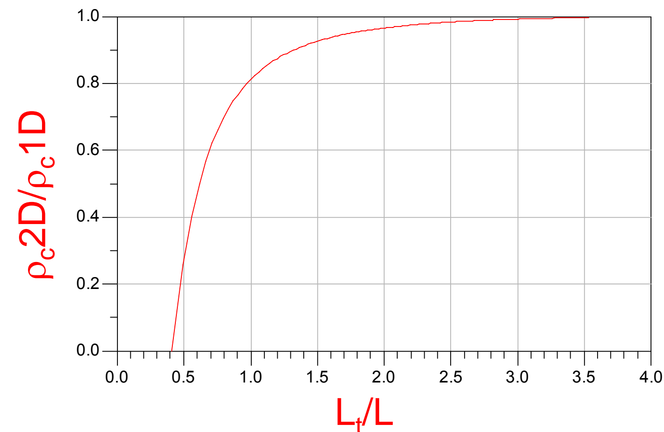


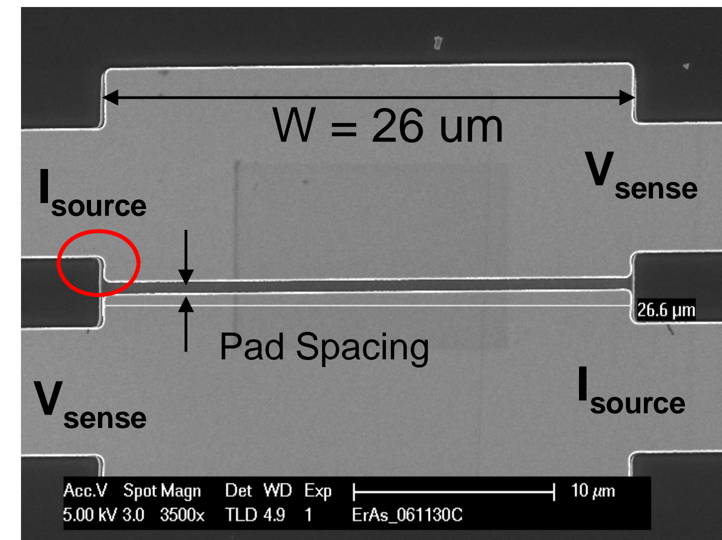
SIMS profile of contacts annealed at 400 C

Error Analysis

- 1-D Approximation
  - Large L_t/L,
  - 1-D case overestimates ρ_c
- Overlap resistance
  - Wide contact width reduces overlap resistance.
- 1-D case, Overlap resistance overestimates extracted ρ_c
- Errors
  - Pad spacing, minimized by SEM inspection
  - Resistance, minimized by using 4155C parameter analyzer
  - $\delta\rho_c/\rho_c^*$ is 60 % at 1 Ω-μm^2 , 75 % at 0.5 Ω-μm^2







*H.Ueng, IEEE TED,2001

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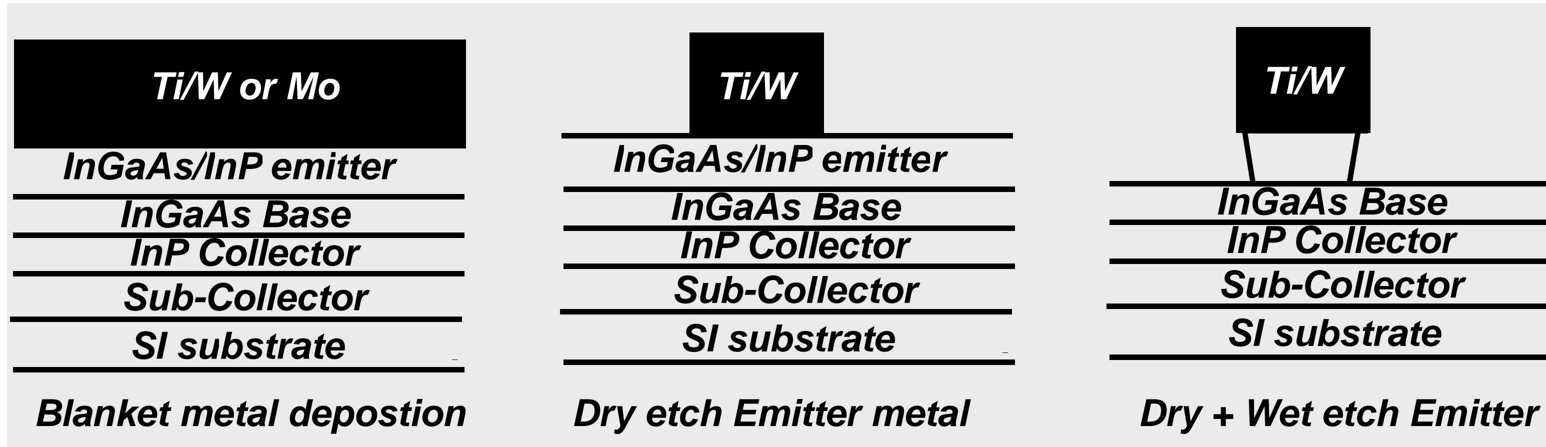
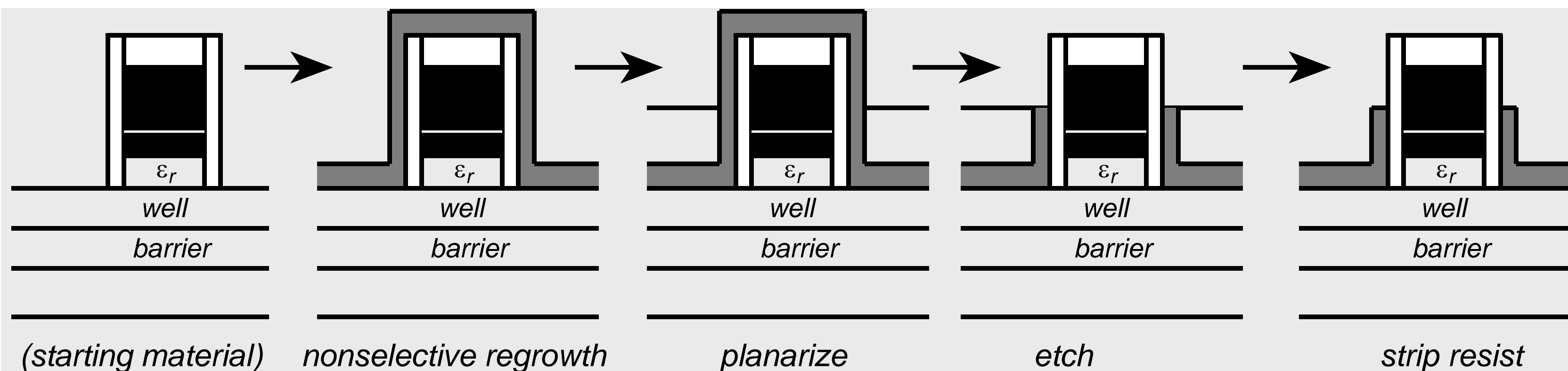
Integration into Device Processing

- HBT emitter contact*



*E.Lind, Late News,DRC 2007

- Source Contact in FETs



Conclusion

- Ultra Low Ohmic contacts to InGaAs/InP with $\rho_c < 1\ \Omega\text{-}\mu m^2$
- Contacts realized by both *in-situ* and *ex-situ*
- *In-situ* Mo/InAs and *ex-situ* TiW/InGaAs $\rho_c < 1\ \Omega\text{-}\mu m^2$ even after 500 C anneal
- *In-situ* ErAs/InAs contacts $\rho_c = 1.5\ \Omega\text{-}\mu m^2$, increases gradually with anneal

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